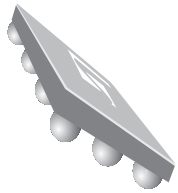
STHVDAC-253C7

Datasheet

BST capacitance controller, 350 µm pitch



Flip Chip 0.35 mm pitch
(12 bumps)

Features

- Dedicated controller to bias BST tunable capacitances
- Turbo and Glide Modes for optimal system performance
- Integrated boost converter with 3 programmable outputs (from 0 to 24 V)
- Low power consumption and high accuracy thanks to production trimming
- MIPI RFFE v2.0 serial interface 1,8 V with extended frequency range up to 52 MHz
- Synchronous reads support (*sRead*)
- 3 USID support in order to control 3 antennas with a single device
- GPIO for Register swap to support DPDT switching and USB cable plugged in
- Available in 350 microns pitch WLCSP for stand-alone or SiP module integration
- WLCSP package is not sensitive to moisture (MSL = 1)

Benefits

- RF tunable passive implementation in mobile phones to optimize the radiated performance

Applications

- Cellular Antenna tunable matching network in multi-band GSM/WCDMA/LTE handsets
- Compatible for open loop antenna tuner application

Product status link
STHVDAC-253C7

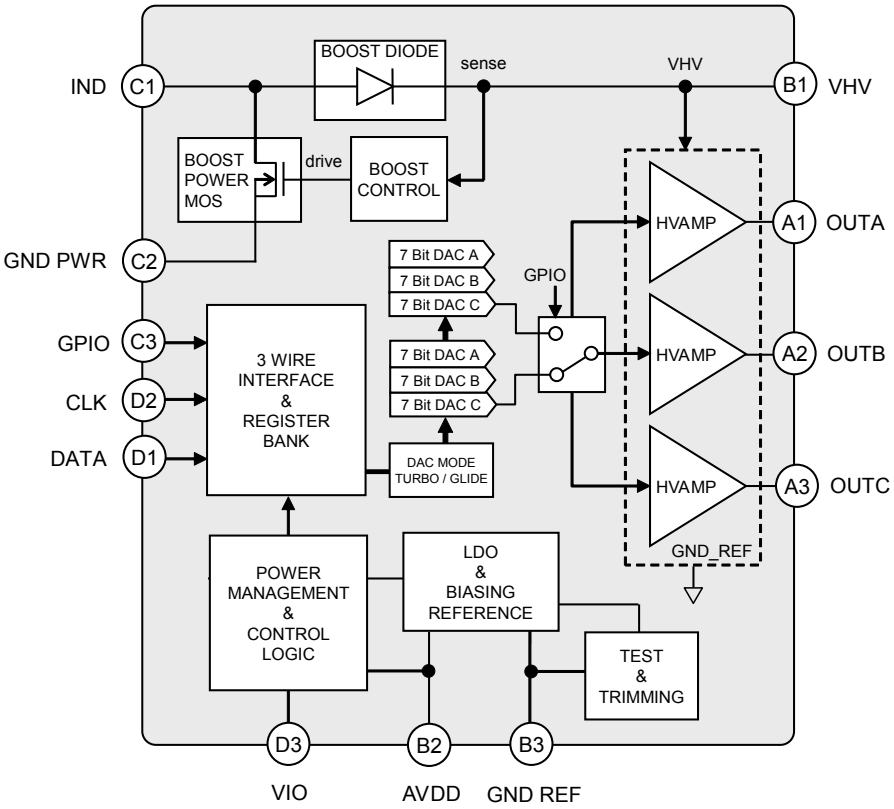
Description

The ST high voltage BST capacitance controller STHVDAC-253C7 is a high voltage Digital to Analog Converter (DAC), specifically designed to control and meet the wide tuning bias voltage requirement of the BST tunable capacitances.

It provides three independent high voltage outputs to control three different capacitances. It is fully controlled through an RFFE serial interface.

BST capacitances are tunable capacitances intended for use in mobile phone application, and dedicated to RF tunable application. They are controlled through a bias voltage ranging from 0 to 24 V. The implementation of BST tunable capacitance in mobile phones enables a significant improvement in terms of radiated performance, making the performance almost insensitive to external environment.

Figure 1. **HVDAC functional block diagram**

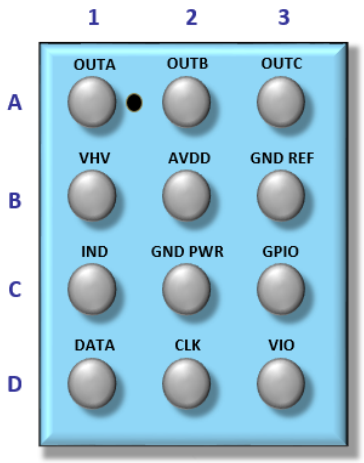


1 Signal description

Table 1. Pinout description

Pin number	Pin name	Description
A1	OUTA	High voltage output A
A2	OUTB	High voltage output B
A3	OUTC	High voltage output C
B1	VHV	Boost High voltage output
B2	AVDD	Analog supply
B3	GND_REF	Analog Ground
C1	IND	Boost inductance
C2	GND_PWR	Power ground
C3	GPIO	General purpose IO, connect to GND otherwise
D1	DATA	RFFE interface / serial DATA
D2	CLK	RFFE interface / serial clock
D3	VIO	Digital supply

Figure 2. Package footprint (bump side view)



2 Characteristics

Table 2. Absolute maximum ratings (limiting value)

Symbol	Parameter	Rating	Unit
AV_{dd}	Analog supply voltage	-0.3 to +5.5	V
$V_{I/O}$	Digital supply voltage	-0.3 to +2.0	V
V_{LOG}	Input voltage logic lines (DATA, CLK, GPIO)	-0.5 to $V_{I/O}$ + 0.5	V
$V_{ESD\ (HBM)}$	Human body model, JESD22-A114-B, All I/O	2	kV
$V_{ESD(CDM)}$	Charge device model, JESD22-C101, all I/O	> ± 125	V
T_{stg}	Storage temperature	-55 to +150	°C
T_j	Maximum junction temperature	125	°C

Table 3. Recommended operating conditions

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
T_{AMB_OP}	Operating ambient temperature	-30		+85	°C
AV_{dd}	Analog supply voltage	2.3		5	V
$V_{I/O}$	Digital supply voltage	1.65		1.95	V
VIH	Input voltage logic level High (DATA, CLK, GPIO)	0.7* $V_{I/O}$		$V_{I/O}$ + 0.3	V
VIL	Input voltage logic level Low (DATA, CLK, GPIO)	-0.3		0.3* $V_{I/O}$	V

Table 4. DC characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{LBOOST}	Boost inductor supply current L = 15 µH AVDD = 3.3 V	Low power mode or idle			0.3		µA
		I_{LBOOST_SS2}	Active mode, 1 output steady state 2 V		90		
			Active mode, 3 outputs steady state 2 V		225		
		I_{LBOOST_SS20}	Active mode, 1 output steady state 20 V		110		
			Active mode, 3 outputs steady state 20 V		280		
I_{AVDD}	AVDD supply current AVDD = 3.3 V	Low power mode or idle			1.5		µA
		I_{AVDD_SS2}	Active mode, 1 output steady state 2 V		270		
			Active mode, 3 outputs steady state 2 V		340		
		I_{AVDD_SS20}	Active mode, 1 output steady state 20 V		270		
			Active mode, 3 outputs steady state 20 V		340		
$I_{I/O}$	$V_{I/O}$ supply current	Low power mode or shutdown			1.4		µA
		Active mode: (3 outputs active) No activity on CLK, VI/O = 1.8 V FCLK = 13 MHz FCLK = 26 MHz			25 190 350		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{I/O}$	$V_{I/O}$ supply current	FCLK = 52 MHz		625		µA
I_{IH}	Input current logic level high	Any mode, DATA, CLK	-1		+1	µA
I_{IL}	Input current logic level low		-1		+1	µA
I_{GPIO}	GPIO leakage current	GPIO = 1.8 V (250 kΩ pull-down)		7.2		µA
V_{IORST}	V_{IO} low threshold	Reset to shutdown mode			0.5	V
V_{IOACT}	V_{IO} high threshold	Shutdown to active mode	1.55			V

Table 5. High voltage DAC output characteristics (Conditions : AV_{dd} from 2.3 to 5 V, $V_{I/O}$ from 1.65 to 1.95 V, T_{amb} from -30 °C to +85 °C, OUTA-C, unless otherwise specified)

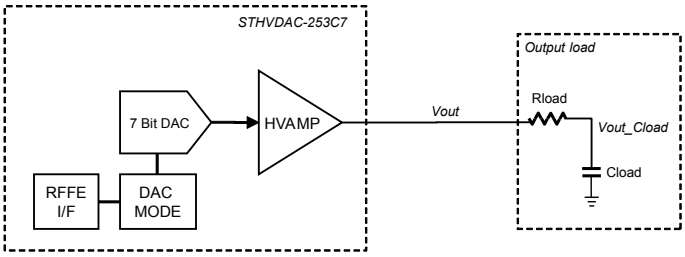
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Low power mode						
Zout	OUTA-OUTC output impedance		6			MΩ
Active mode						
VOH	OUTA-OUTC maximum output voltage	DAC = 7Fh, ILOAD < 1 µA	23.16	23.88	24.59	V
VOL	OUTA-OUTC minimum output voltage	DAC = 0Bh, ILOAD < 1 µA	2.00	2.07	2.13	V
Resolution	Voltage resolution / OUTA- OUTC	7 bits DAC, 0Bh to 7Fh range		188		mV
INL	Integral non−linearity least squared best fit	DAC A – DAC C from 0Bh to 7Fh	-1		+1	LSB
DNL	Differential non−linearity least squared best fit	DAC A – DAC C from 0Bh to 7Fh	-0.5		+0.5	LSB
Error	DACs error	DAC A – DAC C from 0Bh to 7Fh	-3%		+3%	%Vout
Isc	Over current protection	Any DAC output			50	mA

3 Theory of operation

3.1 HVDAC output voltages

The HVDAC outputs are directly controlled by programming the 7 bits DAC (DAC A to DAC C) through the RFFE interface. The DAC stages are driven from a reference voltage, generating an analog output voltage driving a high voltage amplifier supplied from the boost converter (Figure 2. HVDAC functional block diagram).The HVDAC output voltages are scaled from 0 to 24 V, with 127 steps of 188 mV. If DAC value is set to 00h, then the corresponding output is setup to be in high impedance state (6MΩ). STHVDAC-253C7 has been specifically designed to drive BST tunable capacitors, equivalent to RC output loads as shown in Figure 5. HVDAC output voltage in normal, turbo and glide modes.

Figure 3. HVDAC output load



Each DAC output can be operated either in normal, turbo or glide mode. The DAC mode is set by controlling turbo mode bit of each DAC register (MSB of registers 2, 3, 4), and Glide_enable bits (defined in registers 1).

DAC Operation in normal mode -- Glide_enable = 0b, Turbo_mode = 0b

- In normal mode, the DAC output directly switches from old to new output voltage after programming. The DAC output is controlled to ensure the output voltage (V_{out}, see Figure 4. HVDAC output load) reaches its final value within 10 µs typical after valid RFFE command. Typical timing diagram in normal mode is shown on Figure 5. HVDAC output voltage in normal, turbo and glide modes.

DAC Operation in Turbo mode -- Glide_enable = 0b, Turbo_mode = 1b

- A specific Turbo mode is implemented in the STHVDAC-253C7 to ensure a fast system settling time.

  In this mode, the DAC voltage outputs are optimized to minimize the settling time on the output capacitor load (Vout_Cload, see Figure 4. HVDAC output load). Once enabled, the output voltage on the output capacitor reaches its final value within 55 µs typical.

  In TURBO mode, STHVDAC-253C7 has been optimized to support up to 4 different output RC loads, as defined in Table 6. Supported output RC loads (turbo mode only). The RC loads can be selected for each output independently, by controlling PTIC_selection bits in registers 9 to 11.

  Typical timing diagram in Turbo Mode is shown on Figure 5. HVDAC output voltage in normal, turbo and glide modes.

DAC Operation in Glide mode -- Glide_enable = 1b, Turbo_mode = x

- Glide mode has been implemented to smooth DAC output voltage transition, and to minimize the impact of tunable capacitor changes on RF system performance (especially to meet 3GPP phase discontinuity requirements).

  In this mode, the DAC output voltage transitions from old to new voltage value, in a period of time equal to the glide_delay defined as :

  – Glide_delay = glide_step_delay * 256 (programmable from 512 µs up to 16.84 ms)

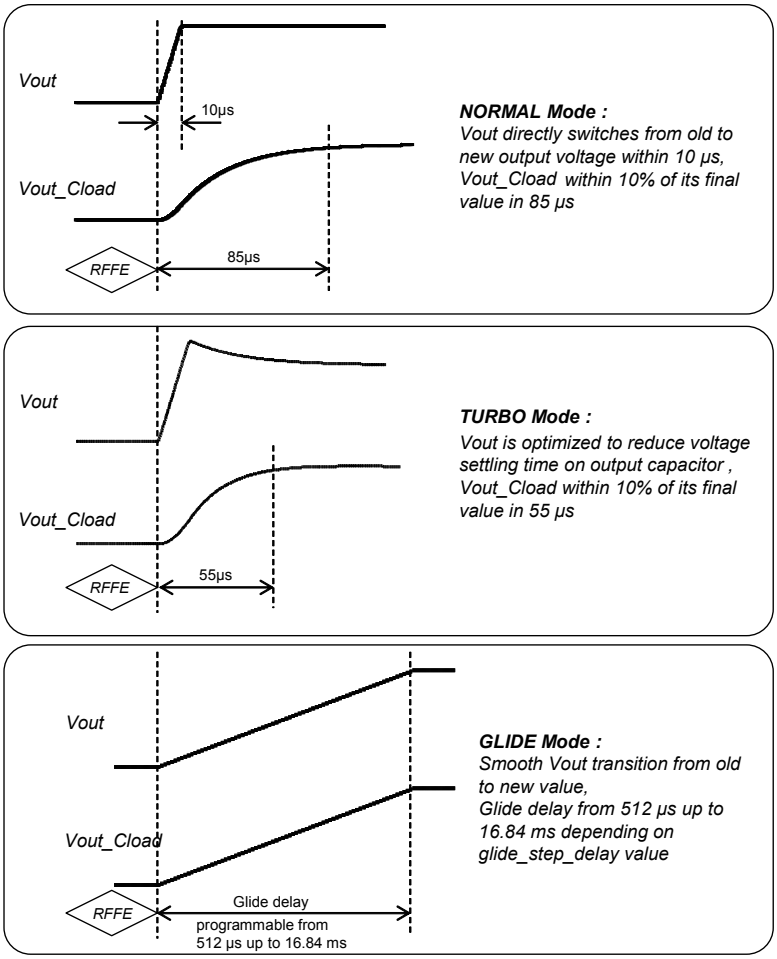
  – glide_step_delay defined in registers 1 as per Table 13. Glide step delay control – Reg#1.

  Typical timing diagram in glide mode is shown on Figure 5. HVDAC output voltage in normal, turbo and glide modes.

Table 6. Supported output RC loads (turbo mode only)

PTIC_selection bits		Rload	Cload
0	0	12 kΩ	2.7 nF
0	1	17 kΩ	
1	0	22 kΩ	
1	1	27 kΩ	

Figure 4. HVDAC output voltage in normal, turbo and glide modes



3.2 Device operating modes

The following operating modes are accessible through the serial interface:

1. **Shutdown mode**: The HVDAC is switched off, and all the blocks in the control ASIC are switched off. Power consumption is almost zero in this mode, the DAC outputs are in high Z state. The shutdown mode is set by driving $V_{I/O}$ to low level.
2. **Active mode**: The device is directly set into this mode after startup, or by driving PWR_mode bits to 00b in register #0 or #28.

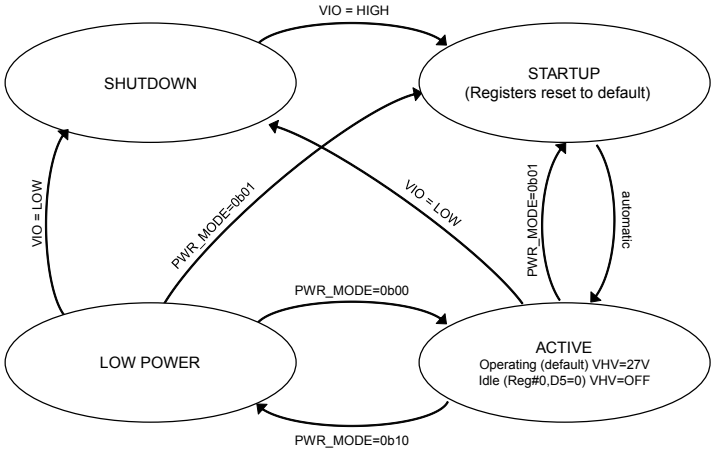
   Active mode is further controlled through reg0 bit D5:

   – D5 = 0b: idle mode: the device is switched off except the RFFE interface. Power consumption is almost zero in this mode, the DAC outputs are in high Z state. (same as low power mode)

   – D5 = 1b (default) : operating mode: The HVDAC is switched on and the DAC outputs are fully controlled through the RFFE serial interface. The DAC settings can be dynamically modified and the outputs will be adjusted according to the specified timing diagrams. Each DAC can be individually controlled and/or pulled down according to application requirements
3. **Low power mode**: The HVDAC is switched off except the RFFE interface. Power consumption is almost zero in this mode, the DAC outputs are in high Z state.

   The device is set into this mode by driving PWR_mode bits to 10b. All registers can be controlled and accessed in low power mode.

Figure 5. **HVDAC state diagram**



3.3 Device reset

Power-on reset is implemented on the $V_{I/O}$ supply input, ensuring the HVDAC will be reset to default mode once $V_{I/O}$ supply line rises above a given threshold (typically 0.5 V). This trigger will force all registers to their default value.

Device reset is also implemented as defined in the MIPI RFFE specification. Setting PWR_mode bits to 01b will force the device to reset all registers to their default value. A soft reset is implemented using register #26 MSB. Setting this bit will reset all registers to their default values, except PM_TRIG register (reg #28) and device USID (reg #31).

3.4 RFFE serial interface

The HVDAC is fully controlled through RFFE serial interface (DATA, VIO, CLOCK). This interface is further described in the next sections of this document and is made compliant to the MIPI alliance specification for RF front end control interface version 1.10 - 26 July 2011 (see Figure 13. Operation register WRITE command sequence and Figure 14. Operation register READ command sequence).

Sequence Start Condition (SSC) : One rising edge followed by falling edge on DATA while CLK remains at logic level low. This is used by the master to identify the start of a command frame.

Parity (P) : Each frame ends with a single parity bit. The parity bit is driven such in a way that the total number of bits in the frame that are driven to logic level one, including the parity bit, is odd.

Bus Park Cycle (BP): the slave releasing DATA will drive the DATA to logic level zero during the first half of the CLK clock cycle. This is used by the master as the indication of the end of frame.

3.5 RFFE serial interface extended mode

All the registers in the device can be addressed in extended mode, by sending appropriate command sequences as per MIPI RFFE specification (Figure 15. Extended register WRITE command sequence).

3.6 RFFE serial interface broadcast capability

Registers #28 to #31 can be addressed in broadcast mode, by sending appropriate command sequences as per MIPI RFFE specification.

3.7 RFFE Interface – command and data frame structure

The STHVDAC-253C7 RFFE interface has been implemented to support the following command sequences.

- Register WRITE
- Register READ
- Extended register write

These supported command sequences are described in Figure 7. Supported command sequences.

Figure 6. Supported command sequences

	SSC			Command Frame								Data frame									
Register WRITE	0	1	0	USID	0	1	0	REG Address[4,0]	P	DATA[7,0]							P	BP			
Register READ	0	1	0	USID	0	1	1	REG Address[4,0]	P	BP	DATA[7,0]						P	BP			
Extended Register WRITE	0	1	0	USID	0	0	0	0	0 0 0 0 / BC[3,0] / 1 1 1 1	P	Address[7,0]						P	Up to 4 bytes of data with parity			BP

USID : Unique Slave Identifier
SSC : Sequence Start Condition
P : Parity Bit
BP : Bus Park Cycle
BC : Byte Count

All frames are required to end with a single parity bit. In case the device detects a parity error, the frame is considered not valid and is ignored.

3.8 Power-up / down sequence

Table 7. Timing (AV_{dd} from 2.3 to 5 V, $V_{I/O}$ from 1.65 to 1.95 V, T_{amb} from - 30 °C to + 85 °C, OUTA-OUTC unless otherwise specified) and Figure 12. Operation with triggers and extended commands are describing the HVDAC settling time requirements and recommended timing diagrams.

Switching from shutdown to active mode is triggered by setting $V_{I/O}$ to high level.

Switching from low power to active mode will occur by setting power mode bits to 00b (register #28 or #0).

Switching from active to low power mode will occur by setting power mode bits to 10b (register #28 or #0).

Following active mode command (from low power), the HVDAC is immediately operational. If a command to change the DAC is sent with the active command, the DAC outputs will rise with the VHV boost voltage in order to reduce the time required to activate the outputs from shutdown to less than 125 µs. Once in active mode, a settling time of 10 µs typ. (Tset) is required following each DAC command in active mode. During this settling time the HVDAC output voltages will vary from the initial to the updated DAC command.

3.9 Power supply sequencing

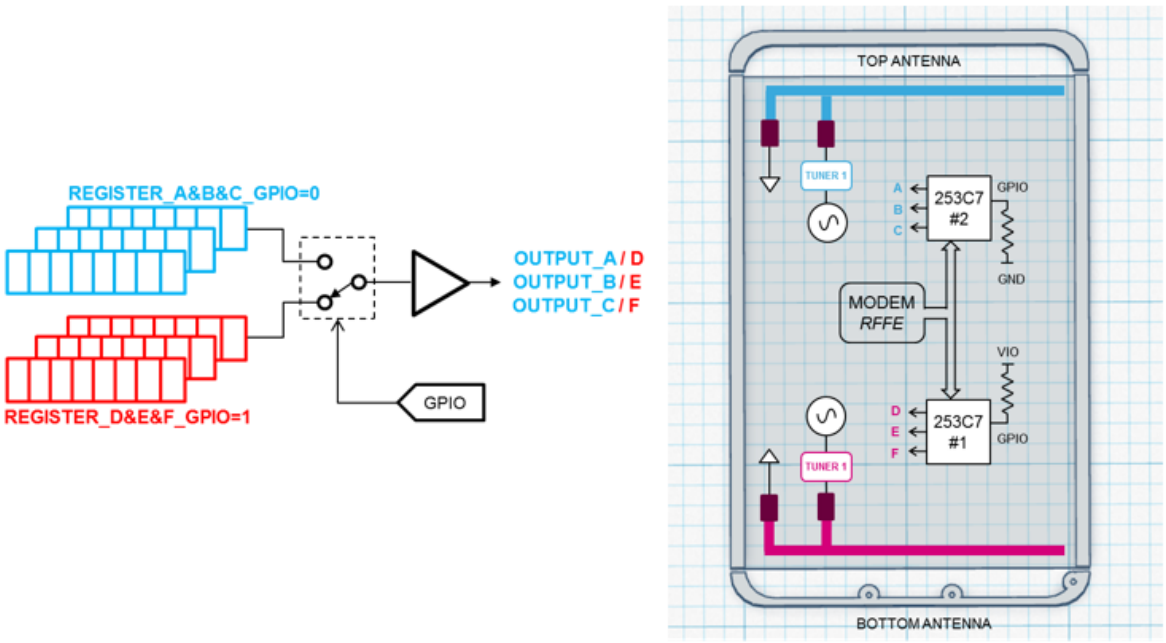
The AVDD is typically directly connected to the battery voltage and is first supplied to the device. After AVDD is supplied and before VIO is applied, the device is in shut down mode and draw minimum leakage current. The STHVDAC-253C7 is fully functional only once both AVDD and VIO are supplied.

3.10 Dual tuner

When two tuners are required on the same phone, it is needed to have two different STHVDAC-253C7 on the PCB board that will be connected to a same RFFE bus. However, as both STHVDAC-253C7 will have the same USID, both of them will respond to the RFFE command. In order to overcome this problem, the GPIO can be used in order to differentiate which output registers will be used by the STHVDAC-253C7. On one STHVDAC-253C7 the GPIO will be tied to GND in order to use register A, B and C for the first tuner. On the other STHVDAC-253C7 the GPIO will be tied to VIO in order to use register D, E and F for the second tuner.

Please refer to Figure below that illustrate how to connect two STHVDAC-253C7 to control two different antenna tuners.

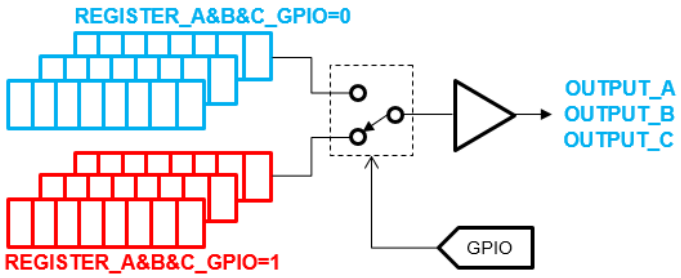
Figure 7. Logic diagram procedure connection



3.11 Antenna diversity mode

When tunable capacitor are implemented on main and secondary antennas, the DAC controlling these tunable capacitor need to be changed when the main and secondary antennas are swapped. A specific GPIO is available in order to change the DAC registers when the DPDT switch the antennas. When the GPIO is activated during a GLIDE transition, the GLIDE will be stopped and the DAC registers will be swapped immediately

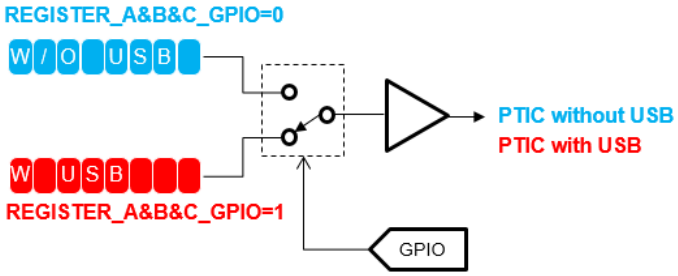
Figure 8. Logic diagram register swap with GPIO control



3.12 USB cable mode

When tunable capacitor are implemented on bottom antenna, the DAC controlling these tunable capacitor need to be changed when the USB cable is plugged as the cable will shift the resonant frequency of the bottom antenna located in close proximity. A specific GPIO is available in order to change the DAC registers to compensate the frequency shift when the USB cable is plugged on the bottom antennas. Each DAC has 2 registers, one with USB cable and one without USB cable.

Figure 9. Logic diagram for GPIO control with USB cable detect



3.13 Trigger mode

To meet precise timing requirements and avoid RFFE interface traffic congestion at critical timing, trigger mode has been implemented in the RFFE interface.

Three triggers (TRIG0, TRIG1 and TRIG2) are available and can be controlled through the RFFE interface.

By default, registers #2 to #4 (DAC A, DAC B and DAC C) are associated to TRIG0. Each DAC can be independently mapped to TRIG0, TRIG1 or TRIG2 by controlling trigger configuration bits in registers #9 and #10.

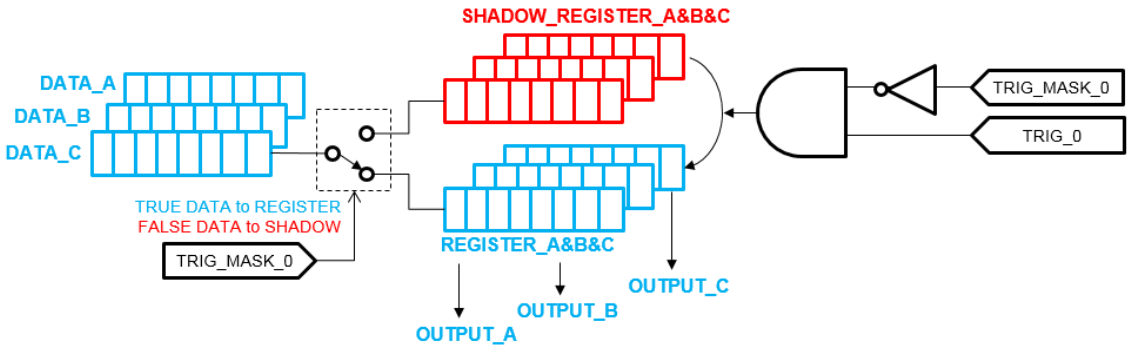
Trigger mode enabled (default mode): by default, the different triggers are enabled and the device is running in triggered mode. In this case, once in active mode, the following sequence must be followed to control the HVDAC outputs:

- Send any valid register #0-#11 write command sequence. The new DAC register values will be temporarily stored in shadow registers
- Send a register #28 write command sequence, setting trigger bits (D2 to D0) and keeping trigger mask bits (D5 to D3) low. The shadow registers will be loaded to destination registers and this will trigger the corresponding DAC outputs to their new values.

Trigger mode disabled: The different triggers are disabled setting corresponding trigger mask bits in register #28 (D5 to D3). In this case, any valid DAC register write command sequence is directly loaded to the destination register, directly triggering the corresponding DAC output to its new value.

The following logic diagram illustrates the trigger mode function. By default the trigger mode is enabled and the DATA are first sent to SHADOW REGISTERS, then transferred into DAC REGISTER once valid trigger is sent to register #28.

Figure 10. Logic diagram trigger mode / default trigger mapping



3.14 Settling time

The STHVDAC will set the bias voltage of the tunable capacitors within 10 µs typical after

- Bus Park (BP) of register #28 write sequence data frame if trigger mode is enabled,
- Parity bit (P) of each data frame of register #1 to #8 extended write sequence if trigger mode is disabled.

Table 7. Timing (AV_{dd} from 2.3 to 5 V, $V_{I/O}$ from 1.65 to 1.95 V, T_{amb} from - 30 °C to + 85 °C, OUTA-OUTC unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{active}	Activation time	Internal voltages activation time from low power to active mode Chv = 33 nF, L = 15 µH	-	90	250	µs
T_{rise}	Output rise time at 95 % of voltage	Chv = 33 nF, V_{out} 2 V to 20 V, equivalent load of 15 kΩ and 2 nF / normal mode	-	5	15	
T_{fall}	Output fall time at 95 % of voltage	Chv = 33 nF, V_{out} 20 V to 2 V, equivalent load of 15 kΩ and 2 nF / normal mode	-	5	15	

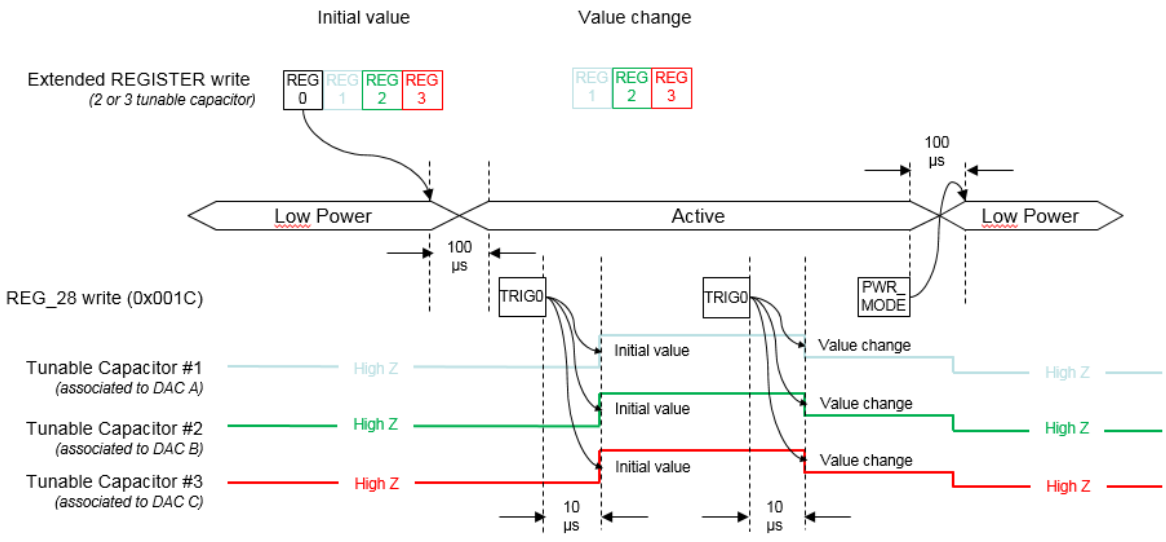
3.15 Recommended operation with trigger and extended commands

It is recommended to use trigger so that outputs will be activated by write to register #28. By default the device is set in triggered mode.

PWR_Mode bits from register #28 have been duplicated in register #0 to ensure the device can be setup from low power to active using one single extended mode RFFE command, as illustrated on Figure 12. Operation with triggers and extended commands.

By default, DAC_A, B and C are mapped to TRIG0. In this configuration, DAC values can be updated through RFFE extended commands, and DAC outputs for a given antenna synchronized through trigger control. Each DAC output can be mapped to TRIG0, 1 or 2 through registers #9 to #11. The Timing diagram below represents recommended operation when default trigger mapping and extended write are in use.

Figure 11. Operation with triggers and extended commands



3.16 Registers table

The HVDAC is embedding 17 x 8 bits registers. Registers content is described in Table 8. Registers table, and registers default values are provided in Table 9. Registers default values.

Table 8. Registers table

Reg#	Reg address hex	Reg address bin	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	Access type
0	00h	[00000]	x	x	Active	0	0	0	PWR mode		RW
1	01h	[00001]	Glide step delay					Glide A EN	Glide B EN	Glide C EN	RW
2	02h	[00010]	TM_A	DAC A with GPIO = 0							RW
3	03h	[00011]	TM_B	DAC B with GPIO = 0							RW
4	04h	[00100]	TM_C	DAC C with GPIO = 0							RW
5	05h	[00101]	Reserved								RW
6	06h	[00110]	TM_A	DAC A with GPIO = 1							RW
7	07h	[00111]	TM_B	DAC B with GPIO = 1							RW
8	08h	[01000]	TM_C	DAC C with GPIO = 1							RW
9	09h	[01001]	TRIG_CONFIG_A		PTIC_select_A		TRIG_CONFIG_B		PTIC_select_B		RW
10	0Ah	[01010]	TRIG_CONFIG_C		PTIC_select_C						RW
11	0Bh	[01011]	Reserved								RW
26	1Ah	[11010]	SW reset	RFFE status							RW
28	1Ch	[11100]	PWR_mode		TRIG mask 2	TRIG mask 1	TRIG mask 0	TRIG2	TRIG1	TRIG0	RW
29	1Dh	[11101]	PRODUCT_ID [00000110b], [00000111b], [00000101b]								R
30	1Eh	[11110]	MANUFACTURER ID [7,0] [00000100b]								R
31	1Fh	[11111]	0	0	MANUF_ID [9,8] [01b]	USID [0111b]					RW

Table 9. Registers default values

Reg#	Reg address hex	Reg address bin	D7	D6	D5	D4	D3	D2	D1	D0
0	00h	[00000]	0	0	1	0	0	0	0	0
1	01h	[00001]	0	0	0	0	0	0	0	0
2	02h	[00010]	0	0	0	0	0	0	0	0
3	03h	[00011]	0	0	0	0	0	0	0	0
4	04h	[00100]	0	0	0	0	0	0	0	0
5	05h	[00101]	0	0	0	0	0	0	0	0
6	06h	[00110]	0	0	0	0	0	0	0	0
7	07h	[00111]	0	0	0	0	0	0	0	0
8	08h	[01000]	0	0	0	0	0	0	0	0
9	09h	[01001]	0	0	0	0	0	0	0	0
10	0Ah	[01010]	0	0	0	0	0	1	0	0
11	0Bh	[01011]	0	1	0	0	0	1	0	0
26	1Ah	[11010]	0	0	0	0	0	0	0	0
28	1Ch	[11100]	0	0	0	0	0	0	0	0
29	1Dh	[11101]	0	0	0	0	0	1	0	1
30	1Eh	[11110]	0	0	0	0	0	1	0	0
31	1Fh	[11111]	0	0	0	1	0	1	1	1

(*)Reg #29 – PRODUCT ID default value is [00000101b] but the device will also respond to 2 other PRODUCT ID in order to program 3 different USID. This will allow to assign a specific USID to every antenna that is tuned by the HVDAC.

3.17 RFFE Interface – registers content description

Registers content and control are further described in Table 10. STHVDAC mode Selection to Table 17. Trigger configuration and PTIC selection registers – Reg#9, #10 and #11.

Table 10. STHVDAC mode Selection

D7	D6	Reg#0 D5	Comments
PWR_mode		Active	
0	0	0	Active mode - Idle
0	0	1	Active mode - operating
0	1	x	Startup / registers reset to default
1	0	x	Low power
1	1	x	n.a.

Table 11. HVDAC trigger control register – Reg#28

D5	D4	D3	D2	D1	D0	Comments
Trig mask 2	Trig mask 1	Trig mask 0	Trig 2	Trig 1	Trig 0	
0	0	0	0	0	0	Triggers 2, 1 and 0 are unmasked / triggers 2,1 and 0 are disabled (default)
0	0	0	1	1	1	Triggers 2, 1 and 0 are unmasked / triggers 2,1 and 0 are enabled
1	1	1	0	0	0	Triggers 2,1 and 0 are masked

Table 12. HVDAC unique slave identifier control – Reg#31

D7	D6	D5	D4	D3	D2	D1	D0	Comments
Spare		MANUFACTURER_ID[9,8]		USID				
0	0	0	1	0	1	1	1	Default value
0	0	0	1	x	x	x	x	USID can be modified by RFFE master, see detailed programming procedure in MIPI RFFE specification

Table 13. Glide step delay control – Reg#1

Address	D7	D6	D5	D4	D3	Comments
	Glide step delay DAC A, B, C					Glide step delay values
[00001]	0	0	0	0	0	2 µs
	0	0	0	0	1	4 µs
	0	0	0	1	0	6 µs
	.	.	.	.	.	.
	1	1	1	1	0	62 µs
	1	1	1	1	1	64 µs

Table 14. Glide enable bits – Reg#1

Address	D2	D1	D0	Comments
[00001]	Glide A EN	Glide B EN	Glide C EN	
	0	0	0	Glide enable = 0: DAC mode set by DAC register MSB
	1	1	1	Glide enable = 1: DAC in glide mode

Table 15. DAC control registers – Reg#2, #3, #4, #6, #7, #8

Address	D7	D6	D5	D4	D3	D2	D1	D0	Comments
	MSB							LSB	
[00010]	TM_A	DAC A							D7: turbo mode control: 0: turbo OFF 1: turbo ON D7 is disregarded is glide mode is enabled D6-D0: DAC output
[00011]	TM_B	DAC B							
[00100]	TM_C	DAC C							

Table 16. RFFE status register – Reg#26

Address	D7	D6	D5	D4	D3	D2	D1	D0	Access type	Triggered
	MSB							LSB		
[11010]	SW reset	RFFE status							RW	No

D7: software reset:

- 0: normal operation
- 1: software reset all configurable registers are reset to their default values (except USID and reg#28)

D6-D0: RFFE status and error reporting

Table 17. Trigger configuration and PTIC selection registers – Reg#9, #10 and #11

Reg address bin	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	Access type
[01001]	TRIG_CONFIG_A		PTIC_select_A		TRIG_CONFIG_B		PTIC_select_B		RW
[01010]	TRIG_CONFIG_C		PTIC_select_C						
[01011]									

Each DAC output can be connected to RFFE TRIG0, TRIG1 or TRIG2

- TRIG CONFIG x : 00b DAC x triggered through TRIG0 default for DAC A, B & C
- TRIG CONFIG x : 01b DAC x triggered through TRIG1
- TRIG CONFIG x : 10b DAC x triggered through TRIG2

In TURBO mode, each DAC output is optimized to supply 4 different RC loads (corresponding to 4 different PTIC designs)

- PTIC_Selection_bits = 00b Rload = 12 kΩ Cload = 2.7 nF (24 capacitor stack STPTIC F1, G1, G2 series)
- PTIC_Selection_bits = 01b Rload = 17 kΩ Cload = 2.7 nF (36 capacitor stack STPTIC H1, L2 series)
- PTIC_Selection_bits = 10b Rload = 22 kΩ Cload = 2.7 nF (48 capacitor stack STPTIC L1, L2 series)
- PTIC_Selection_bits = 11b Rload = 27 kΩ Cload = 2.7 nF (On semi PTIC)

3.18 Serial interface specification

Table 18. Interface specifications (AV_{dd} from 2.3 to 5 V, $V_{I/O}$ from 1.65 to 1.95 V, T_{amb} from -30 °C to +85 °C, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{CLK}	Clock frequency	Max WRITE CLK frequency Half speed read		52		MHz
T_{CLK}	Clock period			19.2		ns
T_{READ_BACK}	Read DATA valid from rising edge of CLK rising edge	Relative to 70 % of CLK rising edge		6		
TD_{setup}	DATA setup time	Relative to 30 % of CLK falling edge	1			
TD_{hold}	DATA hold time	Relative to 70 % of CLK falling edge	5			
C_{CLK}	CLK pin input capacitance			1.4	3.5	pF
C_{DATA}	DATA pin input capacitance			2.3	3.5	

Figure 12. Operation register WRITE command sequence

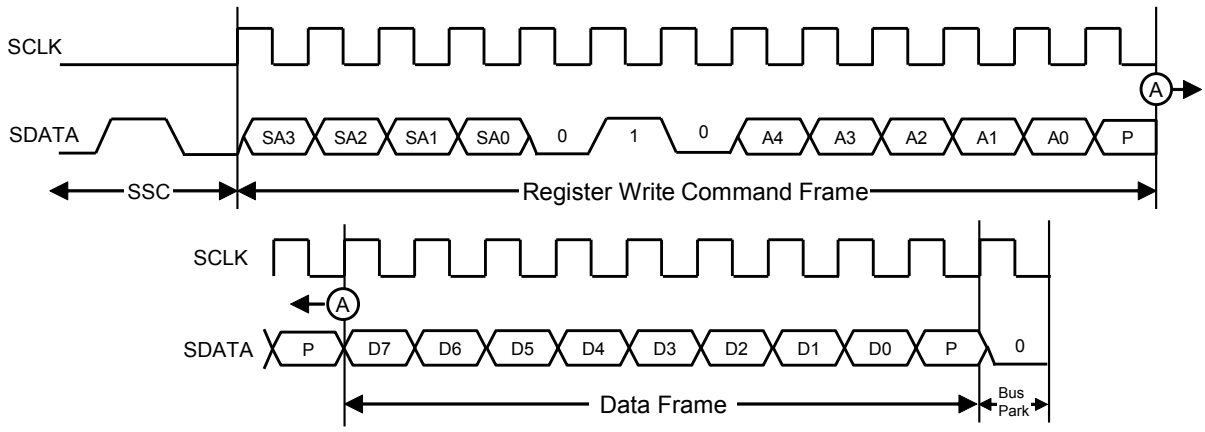


Figure 13. Operation register READ command sequence

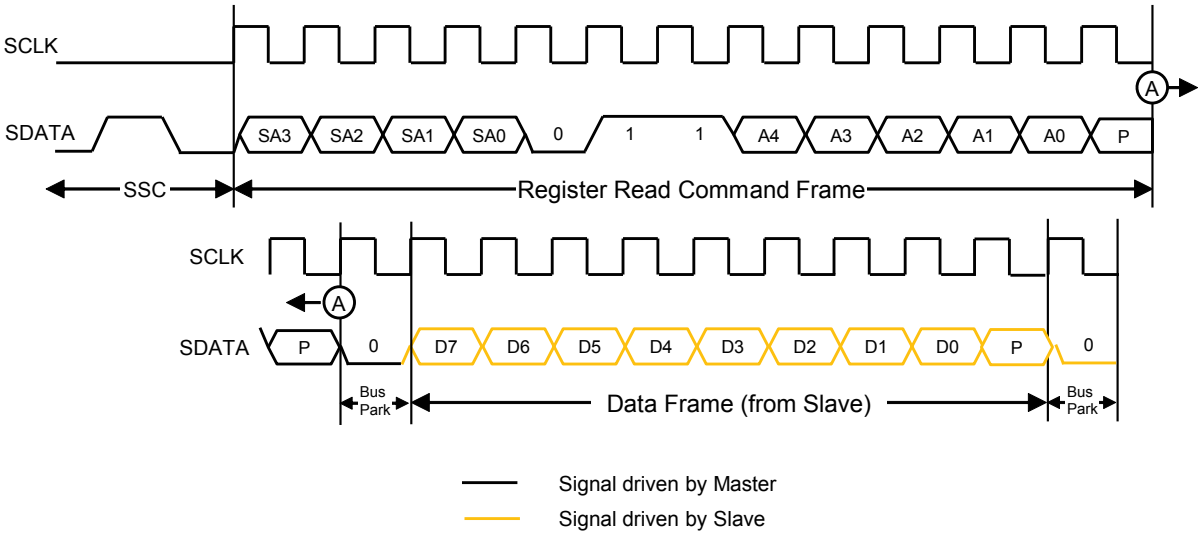
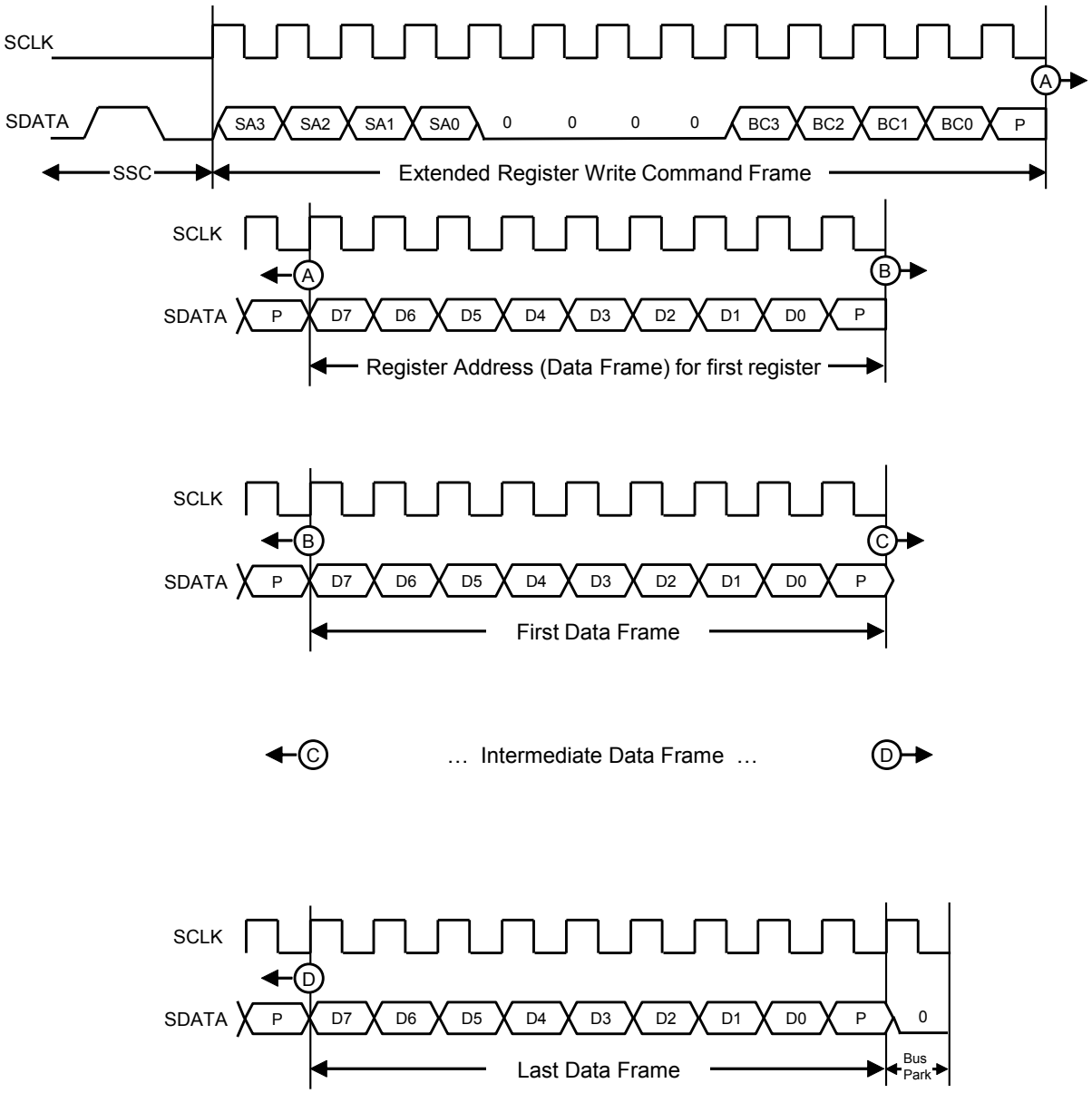


Figure 14. **Extended register WRITE command sequence**



3.19 Application schematic

Figure 15. **Recommended application schematic**

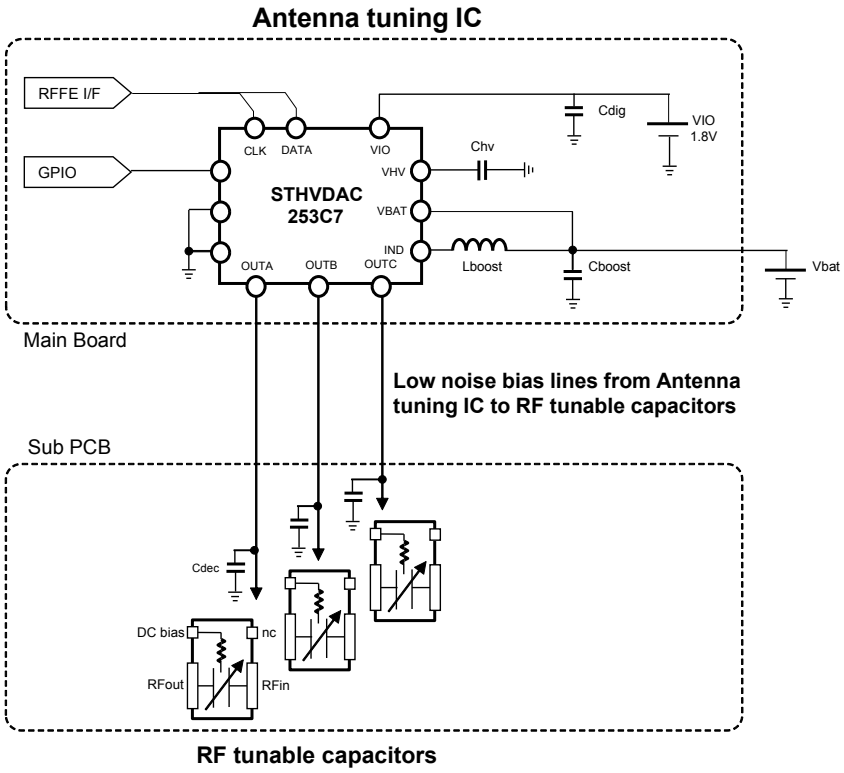
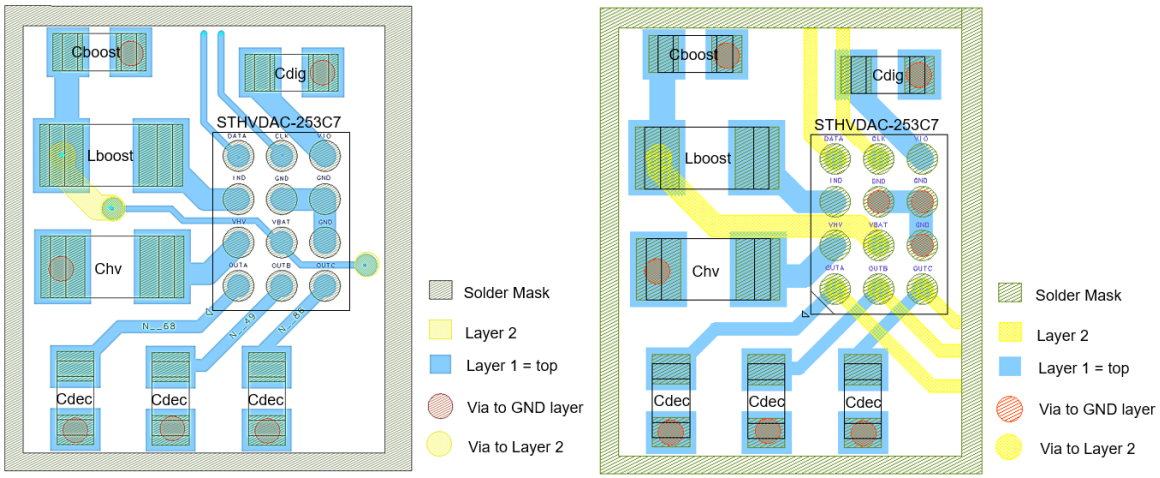


Figure 16. **Recommended PCB layout**



STHVDAC-253C7 can be mounted on a PCB without microvias (left) but can also be assembled on a PCB with microvias (right).

Table 19. Recommended external BOM

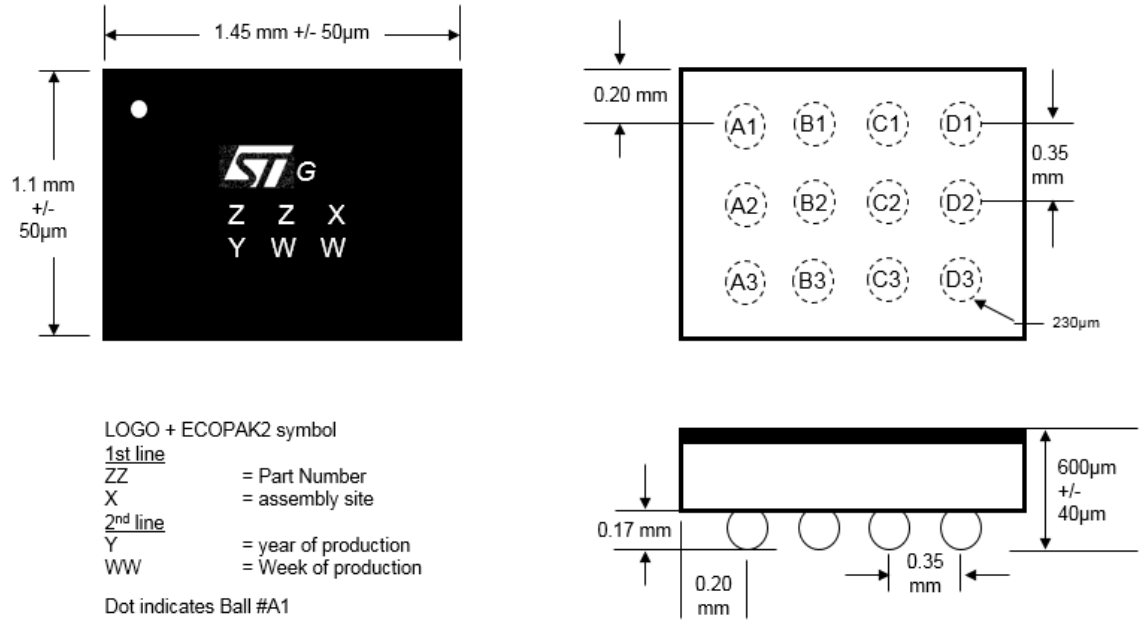
Components	Description	Nominal value	Package (inch)	Package (mm)	Recommended P/N
Cboost	Boost supply capacitor	1 µF	0201	0603	AVX: 02016D105MAT2A
Lboost	Boost inductance	15 µH	0402	1005	MURATA: LQW15DN150M00
		15 µH	0603	1608	COILCRAFT: 0603LS-153XGL
Chv	Boost output capacitance, 50 V	33 nF	0402	1005	MURATA: GRM155R61H333KE19
Cdec	Decoupling capacitance, 50 V	100 pF	0201	0603	TDK: C0603COG1H101J

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

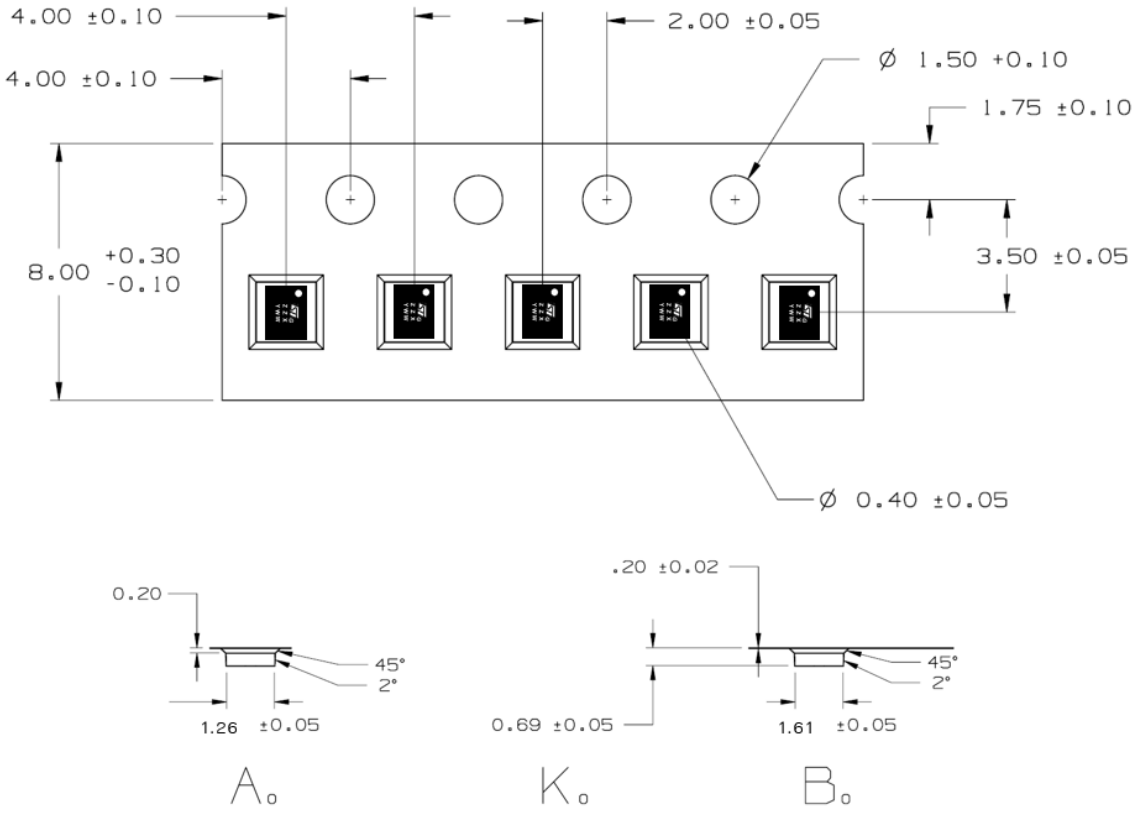
4.1 Flip-chip 0.35 mm pitch package information

Figure 17. Flip-chip 0.35 mm pitch package outline



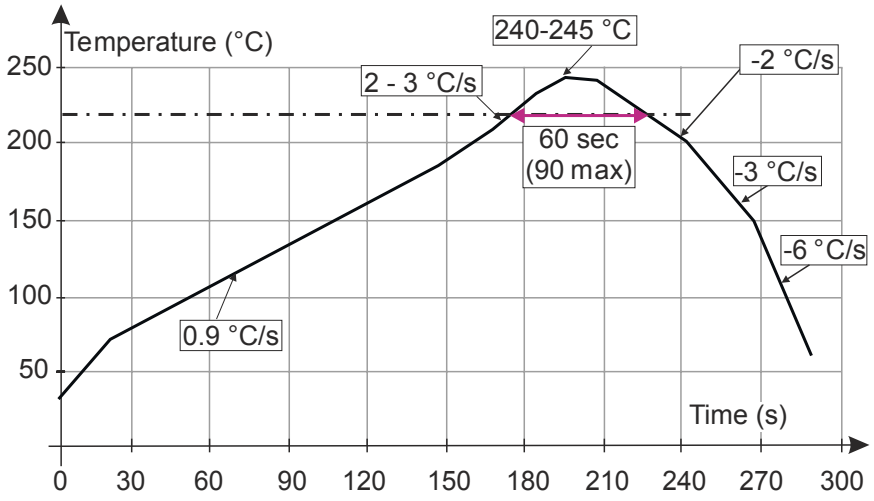
The land pattern below is recommended for soldering the device on PCB
PCB pad design: non soldered mask defined / Micro via under bump allowed
PCB pad size diameter = 200 µm
Solder mask opening Diameter = 250 µm
PCB pad finishing Cu- Ni (2-6µm) – Au (0.2µm max) or CU OSP (Organic Solderability Preservative)
Stencil aperture : 250 x 250 µm²
Stencil thickness: 100 µm max.
Solder paste: 95.8% Sn - 3.5% Ag – 0.7 Cu (no clean flux)

Figure 18. **Tape and reel specification (in mm)**



4.2 Reflow profile

Figure 19. **ST ECOPACK® recommended soldering reflow profile for PCB mounting**



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Table 20. **Recommended values for soldering reflow**

Profile	Value	
	Typical	Max.
Temperature gradient in preheat (T = 70-180 °C)	0.9 °C/s	3 °C/s
Temperature gradient (T = 200-225 °C)	2 °C/s	3 °C/s
Peak temperature in reflow	240-245 °C	260 °C
Time above 220 °C	60 s	90 s
Temperature gradient in cooling	-2 to -3 °C/s	-6 °C/s
Time from 50 to 220 °C	160 to 220 s	

5 Ordering information

Table 21. **Ordering information**

Order code	Marking	Base qty.	Delivery mode
STHVDAC-253C7	NJ	5000	Tape and reel

Revision history

Table 22. **Document revision history**

Date	Revision	Changes
08-Jun-2018	1	Initial release.
17-Sep-2018	2	Updated Table 4. DC characteristics and Table 6. Supported output RC loads (turbo mode only).
25-Sep-2018	3	Updated Section 4.1 Flip-chip 0.35 mm pitch package information.
04-Nov-2019	4	Updated Table 21. Ordering information.
25-Feb-2020	5	Updated Features.
16-Mar-2020	6	Updated Table 2. Absolute maximum ratings (limiting value).
10-Nov-2020	7	Updated Figure 17.

Contents