ON Semiconductor®

Product Bulletin

Document # : PB22146X
Issue Date: 5 February 2018

Title of Change:	AR0237 Register Reference (AND9274/D) document update.
Effective date:	5 February 2018
Contact information:	Contact your local ON Semiconductor Sales Office or <Sonya.Yip@onsemi.com>
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change category:	☐ Wafer Fab Change ☐ Assembly Change ☐ Test Change ☒ Other: Documentation

Change Sub-Category(s):

☐ Manufacturing Site Change/Addition
☐ Manufacturing Process Change
☐ Material Change
☐ Product specific change
☒ Datasheet/Product Doc change
☐ Shipping/Packaging/Marking
☐ Other: _____

Sites Affected:	ON Semiconductor Sites: None	External Foundry/Subcon Sites: None

Description and Purpose:

AR0237 Register Reference updated to match latest register database changes. These changes are the result of a documentation error only; there is no change to the product form, fit, or function.

AR0237 Register Reference Changes

1. In Tables 1 and Table 2, removed confidential registers R0x3096 and R0x398

2. In Tables 1 and Table 2, removed confidential register R0x30DC

3. In Tables 1 and 2, added register R0x31FE

New Register

R12798 (R0x31FE)	CUSTOMER_REV		???? ???? ???? ????	0 (0x0000)	
R0x31FE	15:0	0x0000	CUSTOMER REV (RO)	N	N
	Customer revision				

4. In Tables 1 and Table 2, removed confidential registers R0x3EF8 and R0x3F4A

5. In Table 2, changed R0x301A[15] definition and updated default values

Old Register Definition

R12314	15:0	0x2058	reset_register (R/W)	N	Y
R0x301A	15	0x0000	Reserved		
	14	X	Reserved		
	13	0x0001	Reserved		
	12	0x0000	smia_serialiser_dis 0: HiSPi Interface enabled. 1: HiSPi Interface disabled.	N	N
	11	0x0000	forced_pll_on 0: PLL will be powered down when the sensor is in standby (low power mode). 1: PLL will be enabled even when the sensor is in "standby."	N	N

New Register Definition

	15:0	0x2058	RESET_REGISTER (R/W)	N	Y
	15	0x0000	0: Update of many of the registers is synchronized to frame start. 1: Inhibit register updates. Register changes will remain pending until this bit is returned to 0. When this bit is returned to 0, all pending register updates will be made on the next frame start.		
	14	X	Reserved		
R12314 R0x301A	13	X	Reserved		
	12	0x0000	SMIA_SERIALISER_DIS 0: HiSPi Interface enabled. 1: HiSPi interface disabled.	N	N
	11	0x0000	FORCED_PLL_ON 0: PLL will be powered down when the sensor is in standby (low power mode). 1: PLL will be enabled even when the sensor is in "standby."	N	N

6. In Table 2, updated register R0x301C definition

Old Register Definition

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12316 R0x301C	7:0	0x00	mode_select_ (R/W)	N	Y
	7:1	X	Reserved		
	0:-1	0x00	stream Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	N	N
	-2:2	X	Reserved		
	1	0x00	mirror_row 0: Normal readout 1: Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ is read out of the sensor first.	N	Y
	0	0x00	mirror_col 0: Normal readout 1: Readout is mirrored horizontally so that the column specified by x_addr_end_ is read out of the sensor first.	N	Y
	Controls imaging modes of the sensor. For details see the bit field descriptions.				

New Register Definition

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12316 R0x301C	7:0	0x00	MODE_SELECT_ (R/W)	N	Y
	7:1	X	Reserved		
	0	0x00	STREAM Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	N	N
	Controls imaging modes of the sensor. For details see the bit field descriptions.				

7. In Table 2, changed register R0x3022 definition

Old Register Definition

R12322 R0x3022	7:0	0x00	grouped_parameter_hold_ (R/W)	N	Y
	7:1	X	Reserved		
	0:-1	0x00	grouped_parameter_hold Must be set to 0.	N	N
	-2:1	X	Reserved		
	0	0x00	mask_bad 0: The sensor will produce bad (corrupted) frames as a result of some register changes. : Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame.	N	N
	Controls group parameters of the sensor. For details see the bit field descriptions.				

New Register Definition

R12322 R0x3022	7:0	0x00	GROUPED_PARAMETER_HOLD_ (R/W)	N	Y
	7:1	X	Reserved		
	0	0x00	GROUPED_PARAMETER_HOLD Must be set to 0.	N	N
	Controls group parameters of the sensor. For details see the bit field descriptions.				
R12323 R0x3023	7:0	0x00	MASK_CORRUPTED_FRAMES_ (R/W)	N	N
	When enabled, masks the first frame after any settings change which result in the first output frame being corrupted.				

8. In Table 2, updated R0x3026 default values

Old Register Definition

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12326 R0x3026	15:0	0x6500	gpi_status (RO)	N	N
	15:3	RO	Reserved		
	2	RO	Reserved		
	1	RO	Reserved		
	0	RO	Reserved		
	Reflects the status of the input pins: TRIGGER(2), OUTPUT_ENABLE_N(1), SADDR(0). Upper bits are hardwired to a constant.				

New Register Definition

R12326 R0x3026	15:0	0x6500	GPI_STATUS (RO)	N	N
	15:3	X	Reserved		
	2	X	Reserved		
	1	X	Reserved		
	0	X	Reserved		
	Reflects the status of the input pins: TRIGGER(2), OUTPUT_ENABLE_N(1), SADDR(0). Upper bits are hardwired to a constant.				

9. In Table 2, updated R0x3064 default values

Old Register Definition

R12388 R0x3064	15:0	0x1902	smia_test (R/W)	N	N
	15:13	X	Reserved		
	12	0x0001	Reserved		
	11:10	0x0002	Reserved		
	9	0x0000	Reserved		
	8	0x0001	embedded_data 0: Frames out of the sensor exclude the embedded data. 1: Frames of data out of the sensor include 2 rows of embedded data. This register field should only be change while the sensor is in software standby. Disabling the embedded data will not reduce the number of vertical blanking rows.	N	N
	7	0x0000	embedded_stats_en 0: Embedded statistics are not transmitted on the 2 stats rows after the frame pixel data. 1: Embedded statistics are transmitted on the 2 stats data rows after the frame pixel data.	N	N
	6:4	X	Reserved		
	3:0	0x0002	Reserved		

New Register Definition

R12388 R0x3064	15:0	0x1902	SMIA_TEST (R/W)	N	N
	15:13	X	Reserved		
	12	X	Reserved		
	11:10	X	Reserved		
	9	X	Reserved		
	8	0x0001	EMBEDDED_DATA 0: Frames out of the sensor exclude the embedded data. 1: Frames of data out of the sensor include 2 rows of embedded data. This register field should only be change while the sensor is in software standby. Disabling the embedded data will not reduce the number of vertical blanking rows.	N	N
	7	0x0000	EMBEDDED_STATS_EN 0: Embedded statistics are not transmitted on the 2 stats rows after the frame pixel data. 1: Embedded statistics are transmitted on the 2 stats data rows after the frame pixel data.	N	N
	6:4	X	Reserved		
	3:0	X	Reserved		

10. In Table 2, changed R0x306E[4] to reserved

Old Register Definition

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12398 R0x306E	15:0	0x9018	datapath_select (R/W)	N	N
	15:13	0x0004	slew_rate_ctrl_parallel Selects the slew (edge) rate for the DOUT[11:0], FRAME_VALID, LINE_VALID and FLASH outputs. Only affects the FLASH output when parallel data output is disabled. The value (111) results in the fastest edge rates on these signals. Slowing down the edge rate can reduce ringing and electro-magnetic emissions.	N	N
	12:10	0x0004	slew_rate_ctrl_pixclk Selects the slew (edge) rate for the PIXCLK output. Has no effect when parallel data output is disabled. The value (111) results in the fastest edge rate. Slowing down the edge rate can reduce ringing and electromagnetic emissions.	N	N
	9	0x0000	high_vcm 0: Selects HISPI low vcm (SLVS) mode. VDD_SLVS must be 0.4V 1: Selects HISPI high vcm mode. VDD_SLVS = VDD_IO = 1.8V	N	N
	8	0x0000	datapath_select_bit8 Not used.	N	N
	7:5	X	Reserved		
	4	0x0001	Reserved		
	3	0x0001	datapath_select_row_type_exp_en When enabled, row type and exposure number information is sent to the framer in line-interleave mode. The framer embeds this information as a part of the packetized-SP sync codes. In linear mode	N	N
	2	0x0000	datapath_select_pad_rows_to_framer When disabled in Line-interleave mode, padding rows are not passed on to the framer. Has no effect in linear mode.	N	N
	1:0	0x0000	special_line_valid 00: Normal behavior of LINE_VALID 01: LINE_VALID is driven continuously (continue generating LINE_VALID during vertical blanking) 10: LINE_VALID is driven continuously as LINE_VALID XOR FRAME_VALID 11: Reserved.	N	N

New Register Definition

R12398 R0x306E	15:0	0x9018	DATAPATH_SELECT (R/W)	N	N
	15:13	0x0004	SLEW_RATE_CTRL_PARALLEL Selects the slew (edge) rate for the DOUT[11:0], FRAME_VALID, LINE_VALID and FLASH outputs. Only affects the FLASH output when parallel data output is disabled. The value (111) results in the fastest edge rates on these signals. Slowing down the edge rate can reduce ringing and electro-magnetic emissions.	N	N
	12:10	0x0004	SLEW_RATE_CTRL_PIXCLK Selects the slew (edge) rate for the PIXCLK output. Has no effect when parallel data output is disabled. The value (111) results in the fastest edge rate. Slowing down the edge rate can reduce ringing and electromagnetic emissions.	N	N
	9	X	Reserved		
	8	0x0000	DATAPATH_SELECT_BIT8 Not used.	N	N
	7:5	X	Reserved		
	4	X	Reserved		
	3	0x0001	DATAPATH_SELECT_ROW_TYPE_EXP_EN When enabled, row type and exposure number information is sent to the framer in line-interleave mode. The framer embeds this information as a part of the packetized-SP sync codes. In linear mode	N	N
	2	0x0000	DATAPATH_SELECT_PAD_ROWS_TO_FRAMER When disabled in Line-interleave mode, padding rows are not passed on to the framer. Has no effect in linear mode.	N	N
	1:0	0x0000	SPECIAL_LINE_VALID 00: Normal behavior of LINE_VALID 01: LINE_VALID is driven continuously (continue generating LINE_VALID during vertical blanking) 10: LINE_VALID is driven continuously as LINE_VALID XOR FRAME_VALID 11: Reserved.	N	N

11. In Table 2, changed R0x30B0[12] to reserved and updated default values

Old Register Definition

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12464 R0x30B0	15:0	0x0A38	digital_test (R/W)	N	Y
	15	0x0000	Reserved		
	14	0x0000	pll_complete_bypass 0: PLL is enabled 1: PLL is bypassed. EXTCLK will be used. Note that the serial interface does not function when PLL is bypassed.	N	N
	13	0x0000	context_b Context Control. 0: Use Context A 1: Use Context B	Y	N
	12	0x0000	seq_lp_mode In HiSPI 30fps mode, this bit can be set along with a halved frequency setting. This mode would use reduce the width of some of the digital signals to analog.	N	N
	11	0x0001	cont_line_valid_int Generate continuous LINE_VALIDs (even during frame-blanking)	N	Y
	10	0x0000	delta_dk_t2_read_lim Output delta-dark rows	N	Y
	9	0x0000	context_switch_operation_mode	N	N
	8	0x0000	pixclk_on When set, the parallel output PIXCLK will continue to toggle irrespective of standby mode.	N	N
	7	0x0000	mono_chrome_operation Monochrome sensor operation. 0: Normal operation. 1: Sensor will operate similar to a mono chrome sensor. Useful in the bin2 mode.	Y	N
	6	0x0000	Reserved		
	5	0x0001	Reserved		
	4	0x0001	embedded_hispi_crc 0: Normal operation of hispi_crc calculation is enabled 1: HISPI CRC is calculated from HISPI IP and is sent through embedded lines (the first two lines) in the next frame. Once test_checksum_valid is high, values of CRC are sampled and stored in a register. Logic toggles the 'test_start_checksum' once test_checksum_valid is high - so that CRC is calculated for subsequent frames. Stored CRC value is sent out through embedded data lines in the next frame.	N	N
	3:2	0x0002	Reserved		
	1	0x0000	no_sh_jump_limit When enabled	N	N
	0	0x0000	Reserved		
R12466 R0x30B2	15:0	0x0000	tempsens_data_reg (R/W)	Y	N
	Output value from temperature sensor.				

New Register Definition

	12	X	Reserved		
	11	0x0001	CONT_LINE_VALID_INT Generate continuous LINE_VALIDs (even during frame–blanking)	N	Y
	10	0x0000	DELTA_DK_T2_READ_LIM Output delta–dark rows	N	Y
	9	0x0000	CONTEXT_SWITCH_OPERATION_MODE	N	N
R12464 R0x30B0	8	0x0000	PIXCLK_ON When set, the parallel output PIXCLK will continue to toggle irrespective of standby mode.	N	N
	7	0x0000	MONO_CHROME_OPERATION Monochrome sensor operation. 0: Normal operation. 1: Sensor will operate similar to a mono chrome sensor. Useful in the bin2 mode.	Y	N
	6	X	Reserved		
	5	X	Reserved		
	4	0x0001	EMBEDDED_HISPI_CRC 0: Normal operation of hispi_crc calculation is enabled 1: HiSPi CRC is calculated from HiSPi IP and is sent through embedded lines (the first two lines) in the next frame. Once test_checksum_valid is high, values of CRC are sampled and stored in a register. Logic toggles the 'test_start_checksum' once test_checksum_valid is high – so that CRC is calculated for subsequent frames. Stored CRC value is sent out through embedded data lines in the next frame.	N	N
	3:2	X	Reserved		
	1	0x0000	NO_SH_JUMP_LIMIT When enabled	N	N
	0	X	Reserved		

12. In Table 2, updated R0x30B4[3:1]default value and R0x30B4[0] definition

Old Register Definition

R12468 R0x30B4	15:0	0x0000	tempsens_ctrl_reg (R/W)		
	15:6	0x0000	retrigger_threshold When the measured absolute temperature (ADC value) changes more than this setting, the delta dark algorithm is retriggered and the temperature is saved as the comparison level for the next measurement. If the value is set to zero, the retrigger function will be disabled.	N	N
	5	0x0000	temp_clear_value Clear data register (sanity check).	N	N
	4	0x0000	temp_start_conversion When asserted, a new temp value will be generated for each frame capture. When asserted in standby mode, a new temp value will be generated.	N	N
	3:1	0x0000	Reserved		
	0	0x0000	0: Temperature sensor power on 1: Temperature sensor power off	N	N

New Register Definition

R12468 R0x30B4	15:0	0x0000	TEMPSENS_CTRL_REG (R/W)		
	15:6	0x0000	RETRIGGER_THRESHOLD When the measured absolute temperature (ADC value) changes more than this setting, the delta dark algorithm is retriggered and the temperature is saved as the comparison level for the next measurement. If the value is set to zero, the retrigger function will be disabled.	N	N
	5	0x0000	TEMP_CLEAR_VALUE Clear data register (sanity check).	N	N
	4	0x0000	TEMP_START_CONVERSION When asserted, a new temp value will be generated for each frame capture. When asserted in standby mode, a new temp value will be generated.	N	N
	3:1	X	Reserved		
	0	0x0000	TEMPSENS_POWER_ON 0: Temperature sensor power off 1: Temperature sensor power on	N	N
			Control register for temperature sensor		

13. In Table 2, changed R0x30BA[5] to reserved and updated default values

Old Register Definition

R12474 R0x30BA	15:0	0x760C	digital_ctrl (R/W)	Y	N
	15	0x0000	Reserved		
	14:12	0x0007	Reserved		
	11:9	0x0003	Reserved		
	8	0x0000	combi_mode 1: Operation mode can switch seamlessly between HDR and Linear mode (no bad frames). The HDR sequencer is used. T1 data is output when linear mode is set by register R0x3082.	Y	N
	7	0x0000	Reserved		
	6	0x0000	Reserved		
	5	0x0000	dither_enable Enables dithering after digital gain. Dither will automatically disabled if one of digital color gains is less than 2.	N	N
	4	0x0000	Reserved		
	3:2	0x0003	Reserved		
	1:0	0x0000	Reserved		

New Register Definition

R12474 R0x30BA	15:0	0x760C	DIGITAL_CTRL (R/W)	Y	N
	15	X	Reserved		
	14:12	X	Reserved		
	11:9	X	Reserved		
	8	0x0000	COMBI_MODE 1: Operation mode can switch seamlessly between HDR and Linear mode (no bad frames). The HDR sequencer is used. T1 data is output when linear mode is set by register R0x3082.	Y	N
	7	X	Reserved		
	6	X	Reserved		
	5	X	Reserved		
	4	X	Reserved		
	3:2	X	Reserved		
	1:0	X	Reserved		

14. In Table 2, changed R0x3180[7:4] to reserved and updated default values

Old Register Definition

R12672 R0x3180	15:0	0x8089	delta_dk_control (R/W)	N	N
	15	0x0001	delta_dk_sub_en Enables the delta dark correction.	N	N
	14	0x0000	delta_dk_every_frame Running the delta dark algorithm every frame or when gain, integration time is changing.	N	N
	13	0x0000	delta_dk_recalc Forces recalculation of the delta dark value.	N	N
	12	0x0000	Reserved		
	11	0x0000	Reserved		
	10	0x0000	delta_dk_gradient_removal Enables the gradient removal algorithm.	N	N
	9	0x0000	delta_dk_gradient_every_frame 0: The measured delta dark gradient will be applied to the first frame after standby only. The delta dark values will be recalculated for the second frame after standby. 1: The measured delta dark gradient will be applied every frame.	N	N
	8	X	Reserved		
	7:4	0x0008	delta_dk_rows Number of dark rows to use for delta dark measurements.	N	N
	3:0	0x0009	Reserved		

New Register Definition

R12672 R0x3180	15:0	0x8089	DELTA_DK_CONTROL (R/W)	N	N
	15	0x0001	DELTA_DK_SUB_EN Enables the delta dark correction.	N	N
	14	0x0000	DELTA_DK_EVERY_FRAME Running the delta dark algorithm every frame or when gain, integration time is changing.	N	N
	13	0x0000	DELTA_DK_RECALC Forces recalculation of the delta dark value.	N	N
	12	X	Reserved		
	11	X	Reserved		
	10	0x0000	DELTA_DK_GRADIENT_REMOVAL Enables the gradient removal algorithm.	N	N
	9	0x0000	DELTA_DK_GRADIENT_EVERY_FRAME 0: The measured delta dark gradient will be applied to the first frame after standby only. The delta dark values will be recalculated for the second frame after standby. 1: The measured delta dark gradient will be applied every frame.	N	N
	8	X	Reserved		
	7:4	X	Reserved		
	3:0	X	Reserved		

15. In Table 2, updated default values of register R0x31C4

Old Register Definition

R12740 R0x31C4	15:0	0xF555	hispi_sync_patt (R/W)	N	N
	15:8	0x00F5	Reserved		
	7:0	0x0055	Reserved		
	HISPI Sync Pattern				

New Register Definition

R12740 R0x31C4	15:0	0xF555	HISPI_SYNC_PATT (R/W)	N	N
	15:8	X	Reserved		
	7:0	X	Reserved		
	HiSPi Sync Pattern				

16. In Table 2, updated definition of register R0x31D8

Old Register Definition

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12760 R0x31D8	15:0	0x0000	hispi_test (R/W)	N	N
	15:11	X	Reserved		
	10:7	0x0000	test_mode Define test mode to be applied to MIPI/CCP interface If test_en is asserted: HiSPi: 0: Transmit 0 on each physical line of all enabled data and clock lanes (reserved if using separate HiSPi PHY) 1: Reserved 2: Transmit differential 0 on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 3: Transmit differential 1 on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 4: Transmit a square wave at half the potential serial data rate on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 5: Transmit a square wave at the pixel data rate on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 6: Serializes and transmits the pattern specified by test_user_data 7: Transmit a continuous, repeated sequence of prbs31 data, with no SAV code, copied on all enabled data lanes 8: Transmit a continuous, repeated sequence of prbs9 data, with no SAV code, copied on all enabled data lanes	N	N
	6:4	X	Reserved		
	3:0	0x0000	hispi_test_lane_en Defines which data lanes are enabled when test_en = 1 - b0 = data lane 0 ... b3 = data lane 3	N	N
	-1:3	X	Reserved		
	2:0	0x0000	hispi_alternate_test_mode Alternate column test mode x x 0: _disable_test x 0 1: enable test - even column select even frame - even column , odd frame - odd column x 1 1: enable test - odd column select even frame - odd column , odd frame - even column 1 0 1: enable test in sticky mode - even column/ frame 1 1 1: enable test in sticky mode - odd column/ frame	N	N

New Register Definition

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12760 R0x31D8	15:0	0x0000	HISPI_TEST (R/W)	N	N
	15:11	X	Reserved		
	10:7	0x0000	TEST_MODE Define test mode to be applied to MIPI/CCP interface if test_en is asserted: HiSPi: 0: Transmit 0 on each physical line of all enabled data and clock lanes (reserved if using separate HiSPi PHY) 1: Reserved 2: Transmit differential 0 on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 3: Transmit differential 1 on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 4: Transmit a square wave at half the potential serial data rate on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 5: Transmit a square wave at the pixel data rate on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 6: Serializes and transmits the pattern specified by test_user_data 7: Transmit a continuous, repeated sequence of prbs31 data, with no SAV code, copied on all enabled data lanes 8: Transmit a continuous, repeated sequence of prbs9 data, with no SAV code, copied on all enabled data lanes	N	N
	6:4	0x0000	HISPI_ALTERNATE_TEST_MODE Alternate column test mode x x 0 : _disable_test x 0 1 : enable test – even column select even frame – even column , odd frame – odd column x 1 1 : enable test – odd column select even frame – odd column , odd frame – even column 1 0 1 : enable test in sticky mode – even column/ frame 1 1 1 : enable test in sticky mode – odd column/ frame	N	N
	3:0	0x0000	HISPI_TEST_LANE_EN Defines which data lanes are enabled when test_en = 1 – b0 = data lane 0 ... b3 = data lane 3	N	N

List of Affected Standard Parts:
AR0237CSSC00SUEA0-DR
AR0237CSSC00SHRA0-DR
AR0237CSSC00SPRA0-DR
AR0237CSSC12SHRA0-DR
AR0237CSSC12SPRA0-DR
AR0237IRSH12SHRA0-DR-E
AR0237IRSH12SPRA0-DR-E

Appendix A: Changed Products

Product	Customer Part Number
AR0237CSSC00SHRA0-DR	
AR0237CSSC00SPRA0-DR	
AR0237CSSC00SUEA0-DR	
AR0237CSSC12SHRA0-DR	
AR0237CSSC12SPRA0-DR	