

## General Description

The AOZ1325DI is a P-channel high-side load switch with slew rates of 1ms. The AOZ1325DI provide an output discharge circuit to quickly discharge the output when the switch is disabled.

The P-channel MOSFET has typical on resistance of 250mΩ at 1.8V. The very low  $R_{DS(ON)}$  significantly reduces the power path dissipation. The input voltage range of AOZ1325DI is from 1.6V to 5.5V. The control input is compatible with both TTL and CMOS logic. Ultra low quiescent current makes this product suitable for any portable applications.

The AOZ1325DI is available in 8-pin 3x3 DFN package and is rated over the -40°C to +85°C ambient temperature range.

## Features

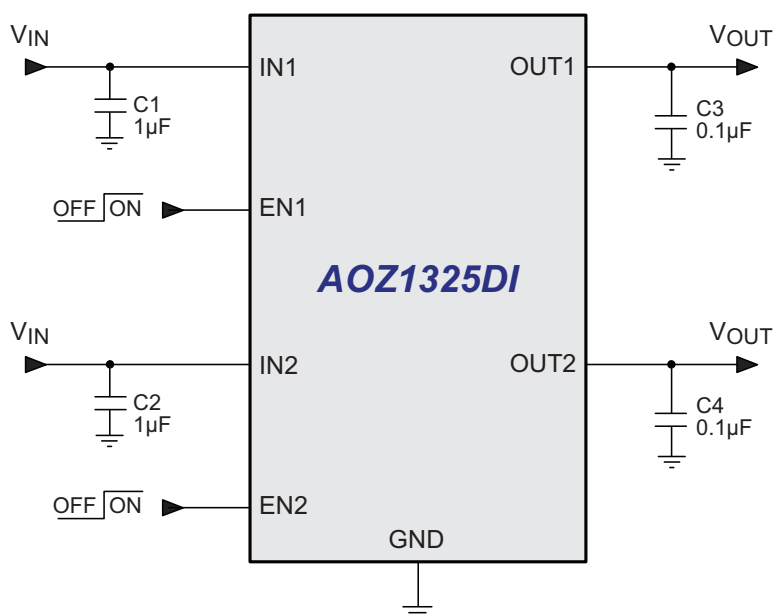
- 1.6V to 5.5V input voltage range
- Low  $R_{DS(ON)}$  (250mΩ typical at 1.8V)
- Controlled turn-on slew rate: 1ms
- Output discharge function
- Low quiescent current (1.0μA typical)
- Low Shutdown Current (<1μA)
- 4kV ESD rating
- Tiny 3x3mm DFN package

## Applications

- Cellular phones
- MP3 players
- Personal media players
- Notebook computers
- Digital still cameras
- Hot-swap applications



## Typical Applications Circuit



## Ordering Information

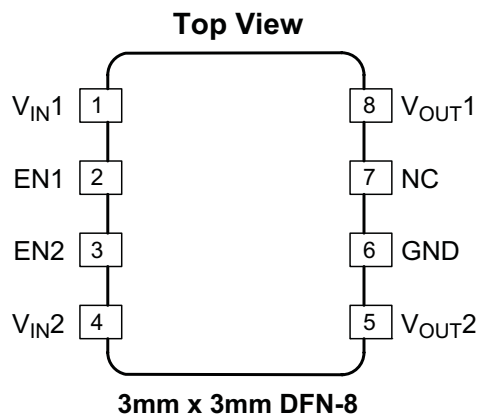
Part Number	Slew Rate	Output Discharge	Package	Environmental
AOZ1325DI	1ms	Yes	3x3 DFN-8	RoHS Compliant Green Product



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.

Please visit [www.aosmd.com/web/quality/rohs\\_compliant.jsp](http://www.aosmd.com/web/quality/rohs_compliant.jsp) for additional information.

## Pin Configuration



## Pin Description

Pin Name	Pin Number	Pin Function
$V_{IN1}$	1	Input. IN is the drain of the P-channel MOSFET. It is the supply input of the IC.
EN1	2	Enable. The P-channel MOSFET turns on when EN is logic high.
EN2	3	Enable. The P-channel MOSFET turns on when EN is logic high.
$V_{IN2}$	4	Input. IN is the drain of the P-channel MOSFET. It is the supply input of the IC.
$V_{OUT2}$	5	Output. OUT is the source of the P-channel MOSFET.
GND	6	Ground.
NC	7	No Connect.
$V_{OUT1}$	8	Output. OUT is the source of the P-channel MOSFET.

## Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Input Voltage ( $V_{IN}$ )	6V
Enable Voltage ( $V_{EN}$ )	$V_{IN} + 0.3V$
Continuous Drain Current ( $I_D$ ) $T_A = 25^\circ C$ $T_A = 85^\circ C$	$\pm 1.0A$ $\pm 0.7A$
Pulsed Drain Current ( $I_{DP}$ )	$\pm 6A$
Continuous Diode Current ( $I_S$ )	-50mA
Storage Temperature ( $T_S$ )	-55°C to +150°C
ESD Rating <sup>(1)</sup>	4kV

### Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model is a 100pF capacitor discharging through a 1.5k $\Omega$  resistor.

## Thermal Ratings

The device is not guaranteed to operate beyond the Thermal Ratings.

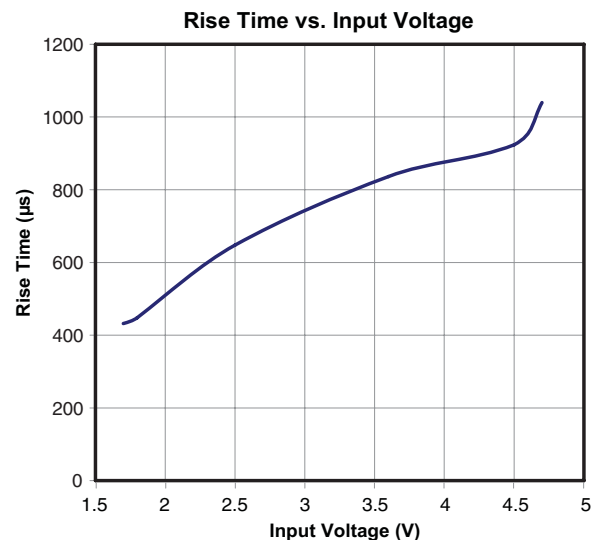
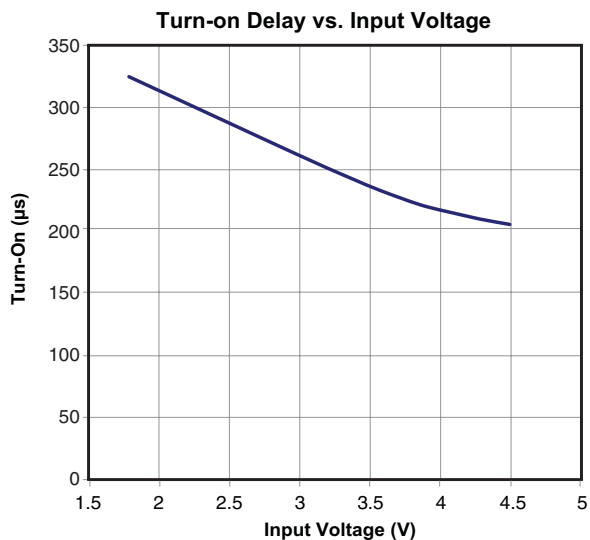
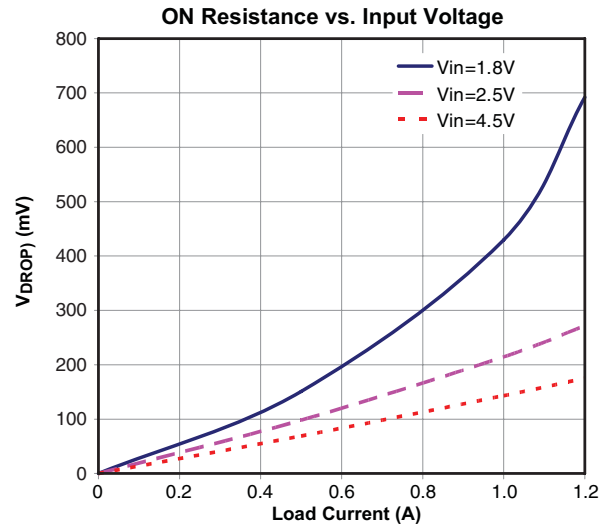
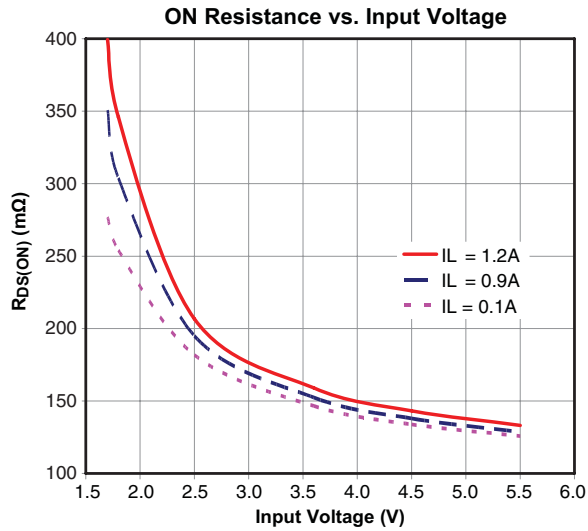
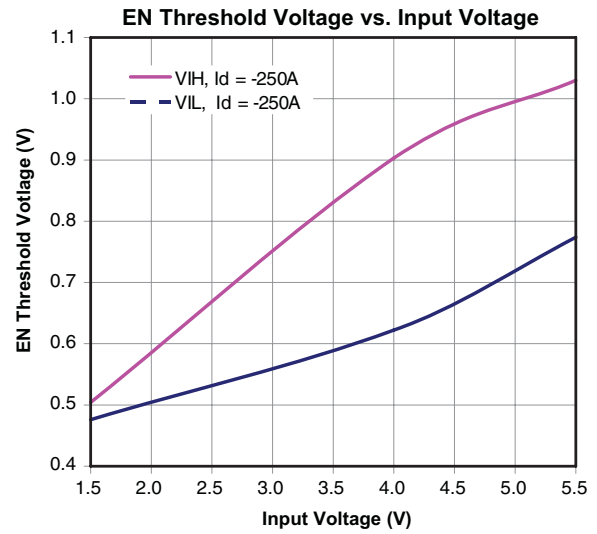
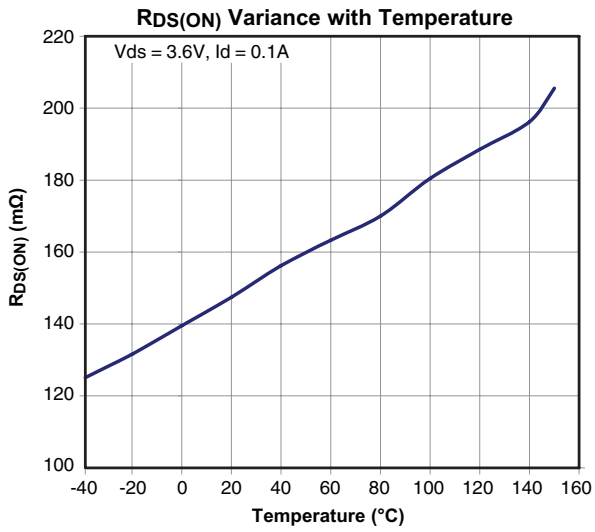
Parameter	Rating
Input Voltage ( $V_{IN}$ )	+1.6 to +5.5V
Junction Temperature ( $T_J$ )	-40°C to +125°C
Package Thermal Resistance, 3 X 3 DFN-8 ( $\Theta_{JA}$ )	136°C/W

## Electrical Characteristics

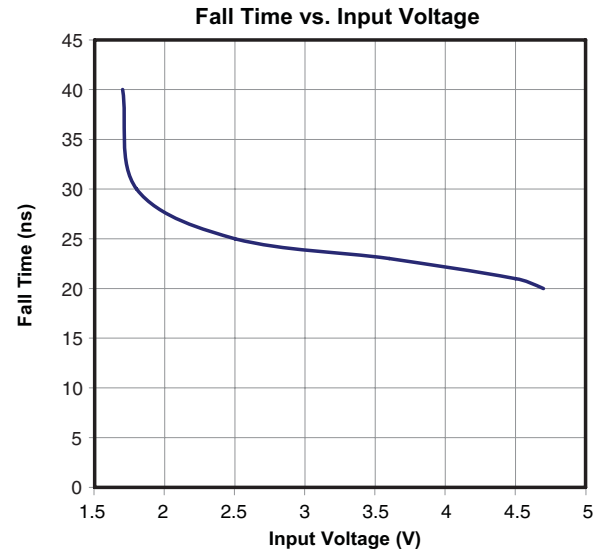
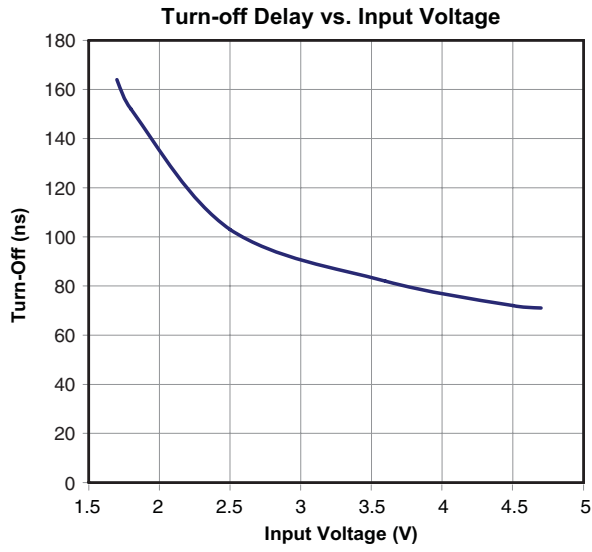
$T_A = 25^\circ C$ ,  $V_{IN} = V_{EN} = 5V$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
$V_{EN\_TH}$	Enable Threshold Voltage	$V_{IN} = 1.6V$ to $4.5V$ , $I_D = -250\mu A$	0.3		1.2	V
$I_{IN}$	Quiescent Supply Current (Single Channel)	$V_{IN} = V_{EN} = 5.5V$		1.6	3	$\mu A$
$I_{OFF}$	OFF state Leakage Current (Single Channel)	$V_{IN} = +5.5V$ , $V_{EN} = 0V$			1	$\mu A$
$R_{DS(ON)}$	Switch On-Resistance (Single Channel)	$V_{IN} = 3.3V$ , $I_D = -100mA$ , $V_{EN} = 1.5V$ $V_{IN} = 1.8V$ , $I_D = -100mA$ , $V_{EN} = 1.5V$		150 250	210 350	m $\Omega$ m $\Omega$
$R_{SHUTDOWN}$	Turn-off Resistance (Single Channel)	$V_{IN} = 3.6V$ , $I_{TEST} = 1mA$ , $V_{EN} = 0V$		162	220	$\Omega$
<b>DELAY TIME</b>						
$T_{D(ON)}$	Output Turn-on Delay	$V_{IN} = 3.6V$ , $I_D = -100mA$ , $V_{EN} = 1.5V$		320	700	$\mu s$
$T_R$	Output Rise-time	$V_{IN} = 3.6V$ , $I_D = -100mA$ , $V_{EN} = 1.5V$	500	1000	1500	$\mu s$
$T_{D(OFF)}$	Output Turn-off Delay	$V_{IN} = 3.6V$ , $I_D = -100mA$ , $V_{EN} = 1.5V$ without output cap		60	200	ns
$T_F$	Output Fall-time	$V_{IN} = 3.6V$ , $I_D = -100mA$ , $V_{EN} = 1.5V$ without output cap		20	100	ns

## Typical Operating Characteristic

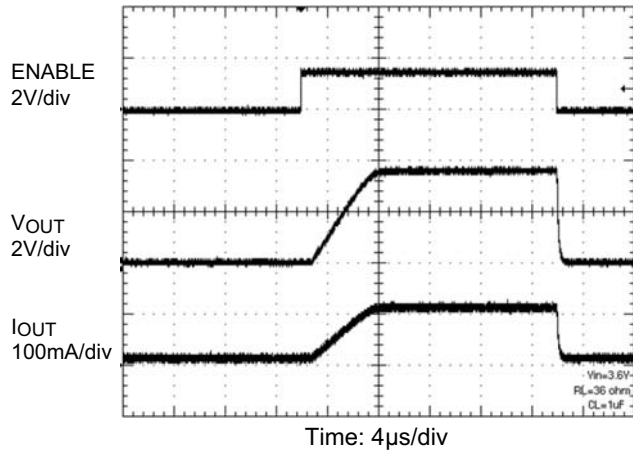


**Typical Operating Characteristic** (Continued)

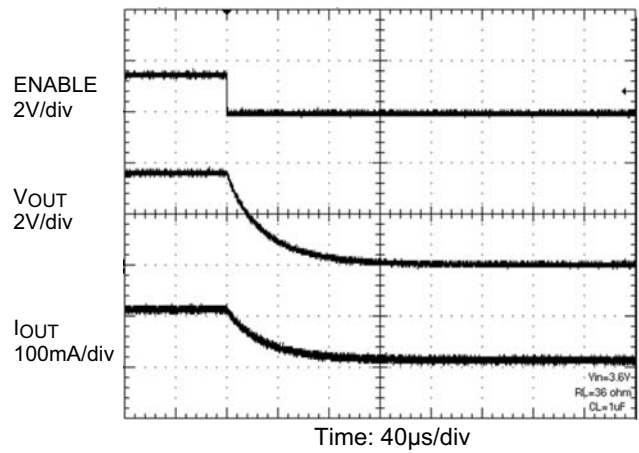


## Functional Characteristics

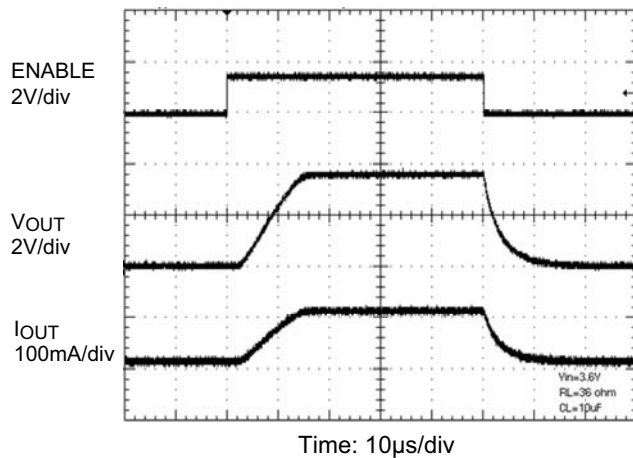
Turn-On/Turn-Off Timing



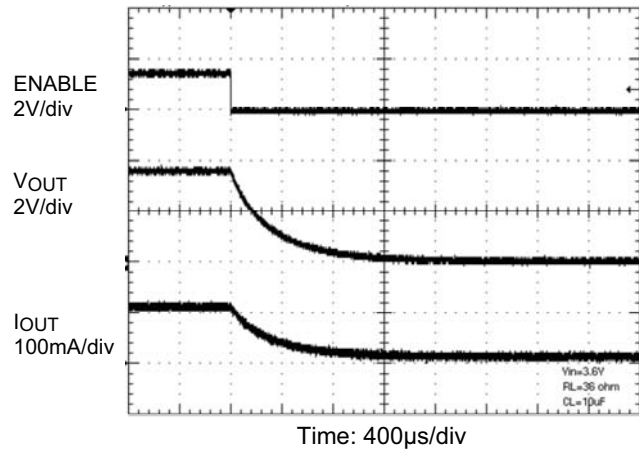
Turn-Off Timing



Turn-On/Turn-Off Timing



Turn-Off Timing



### Timing Diagram

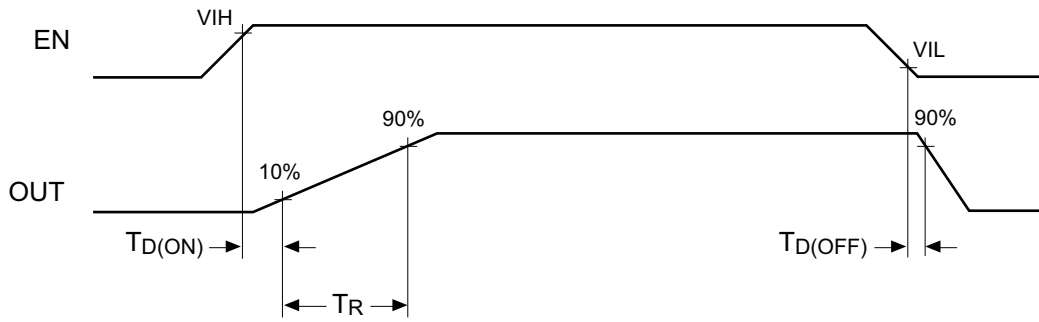


Figure 1. AOZ1325DI Timing Diagram

### Functional Block Diagram

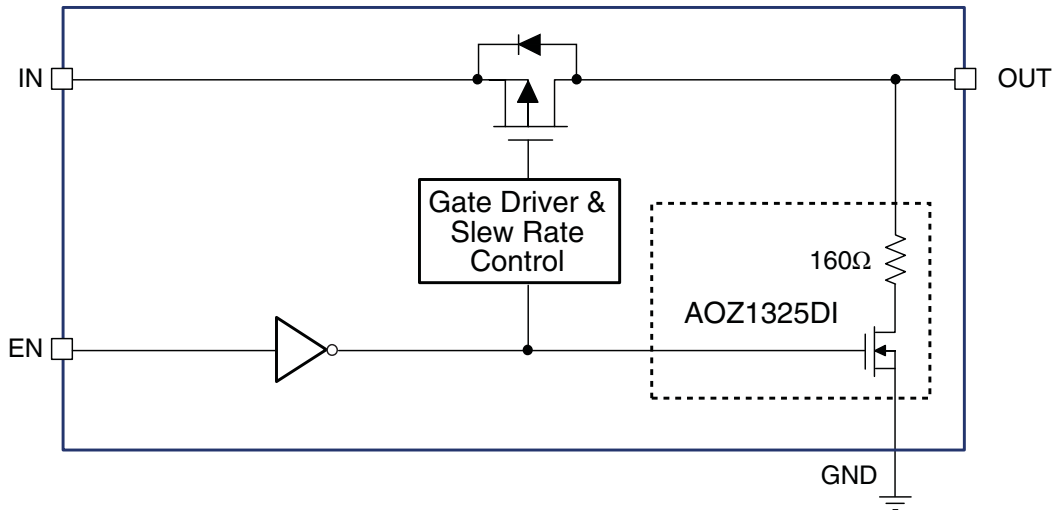


Figure 2. Functional Block Diagram (single channel)

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## Detailed Description

### Internal Discharge Resistor

The AOZ1325DI has an internal 160Ω resistor to discharge any remaining voltage from the system to the ground that is store in a capacitive load. This provides a safe shutdown of the system to prevent any damages to the devices. This function is controlled from the Enable pin.

### Slew Rate Control

The AOZ1325DI is a family of P-channel high-side load switches with controlled slew rate. The device is enabled when the EN pin is high. Once enabled, the gate driver and slew-rate control circuitry immediately raises the source-to-gate voltage of the P-channel MOSFET to its threshold level, and then gradually turns on the MOSFET by linearly increases the source-to-gate voltage. This slow turn-on action effectively limits the input inrush current and provides a nice ramp for the output voltage. After the MOSFET is fully enhanced, the AOZ1325DI quickly increases the source-to-gate voltage to the full input voltage to minimize on resistance and reduce power dissipation.

AOZ1325DI has a slew rate of 1ms. This option significantly reduces the inrush current when the MOSFET turns on, allowing the use of very small input capacitor. The AOZ1325DI also include an internal output discharge circuit that quickly discharges the output to ground when the device is disabled.

### On/Off Control

The AOZ1325DI is enabled when the EN pin is asserted high. The device is disabled when the EN pin is asserted low. The EN input is compatible with both TTL and CMOS logic.



## Applications Information

### Input Capacitor Selection

Use a 1μF or larger capacitor for input bypassing. Place the capacitor close to the IN pins of AOZ1325DI.

### Output Capacitor Selection

Use a 0.1μF or larger capacitor between OUT and GND. The capacitance does not affect the turn-on slew rate. However, a larger capacitor makes the initial turn-on transient smoother.

### Thermal Considerations

To ensure proper operation, the maximum junction temperature ( $T_{J(MAX)}$ ) of the AOZ1325DI should not exceed 125°C. Several factors attribute to the junction temperature rise: load current, MOSFET on resistance ( $R_{DS(ON)}$ ), junction-to-ambient thermal resistance ( $\Theta_{JA}$ ), and ambient temperature ( $T_A$ ). Use the following equation to determine the maximum continuous load current  $I_{LOAD(MAX)}$ :

$$I_{LOAD(MAX)} = \sqrt{\frac{T_{J(MAX)} - T_A}{\Theta_{JA} \times R_{DS(ON)}}}$$

where;

$R_{DS(ON)}$  is the maximum value of the MOSFET on resistance at 25°C.

Please note the maximum load current should not exceed the absolute maximum current rating of the switch.

For example, when  $V_{IN} = 1.8V$ , the maximum continuous load current at room temperature is:

$$I_{LOAD(MAX)} = \sqrt{\frac{125^{\circ}C - 25^{\circ}C}{136^{\circ}C \times R_{DS(ON)}}} = 1.4A$$

Since the calculated current is greater than the absolute maximum current rating, the maximum load current at  $V_{IN} = 1.8V$  and room temperature is 1A. Exceeding the maximum continuous load current may cause damage to the device.

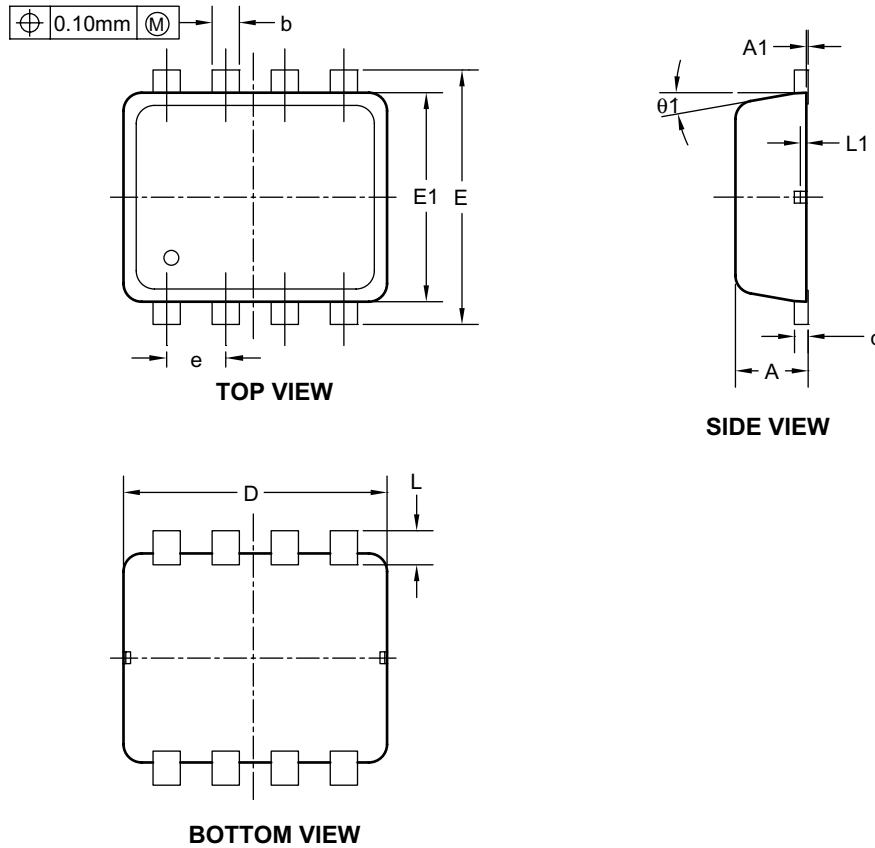
### Power-up Sequence

EN pin must be powered up after  $V_{IN}$  pin, in order to avoid latch-up, or mis-operation of switch. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the product.

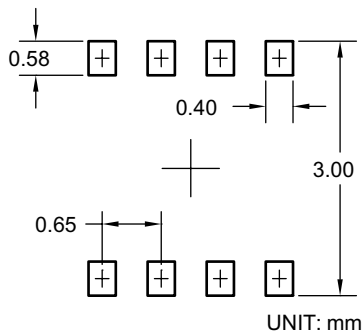
### Layout Guidelines

Good PCB is important for improving the thermal performance of AOZ1325DI. Place the input and output bypass capacitors close to the IN and OUT pins. The input and output PCB traces should be as wide as possible for the given PCB space. Use a ground plane to enhance the power dissipation capability of the device.

Package Dimensions, DFN 3 x 3



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.70	0.80	0.90
A1	0.00	—	0.05
b	0.24	0.30	0.35
c	0.08	0.15	0.25
D	2.90 BSC		
E	2.80 BSC		
E1	2.30 SC		
e	0.65 BSC		
L	0.20	0.38	0.45
L1	0.05	—	—
$\theta 1$	0°	10°	12°

Dimensions in inches

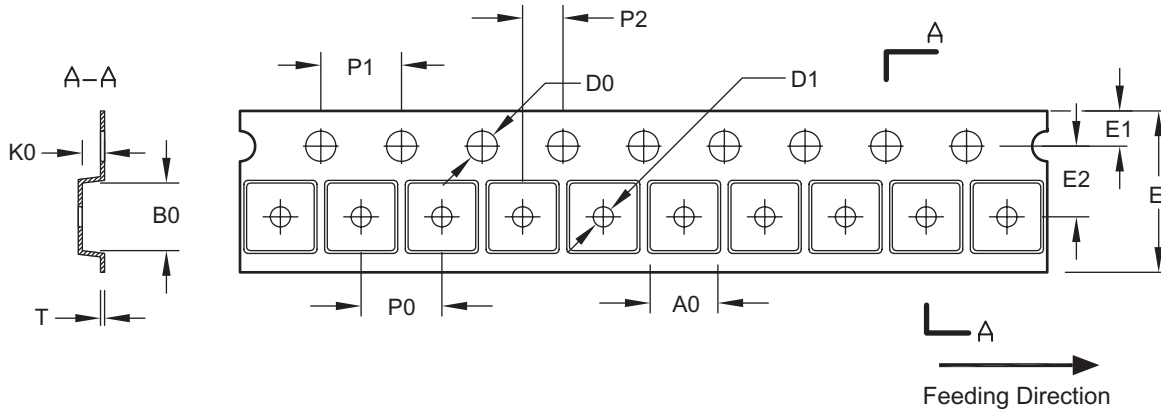
Symbols	Min.	Nom.	Max.
A	0.028	0.031	0.035
A1	0.000	—	0.002
b	0.009	0.012	0.014
c	0.003	0.006	0.010
D	0.114 BSC		
E	0.110 BSC		
E1	0.091 SC		
e	0.026 BSC		
L	0.008	0.015	0.018
L1	0.002	—	—
$\theta 1$	0°	10°	12°

Notes:

1. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils each.
2. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

### Tape and Reel Dimensions, DFN 3 x 3

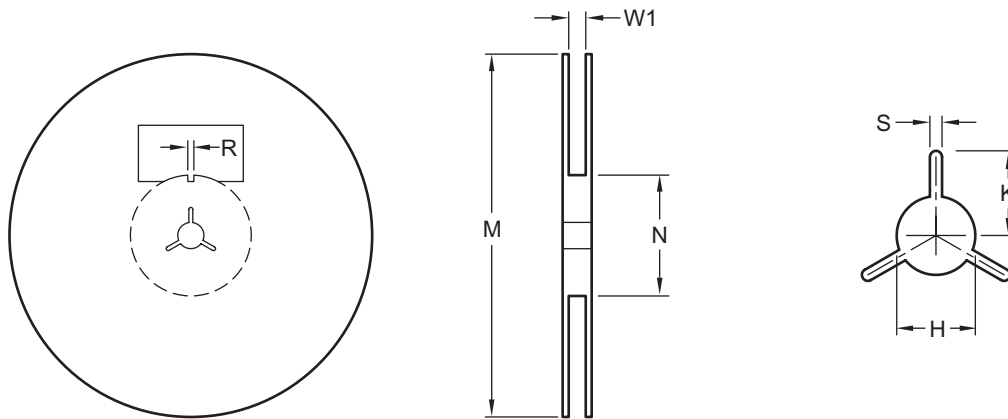
#### Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 3x3 EP	3.40 ±0.10	3.35 ±0.10	1.10 ±0.10	1.50 +0.10/-0.00	1.00 +0.25/-0.00	8.00 +0.30/-0.10	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.23 ±0.20

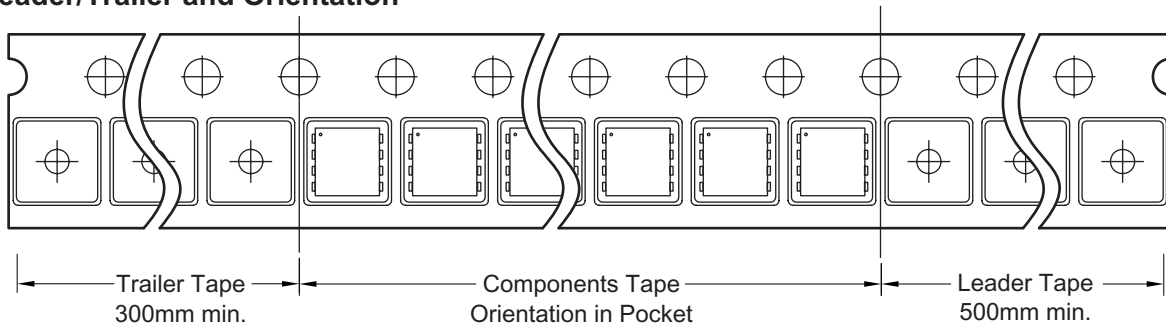
#### Reel



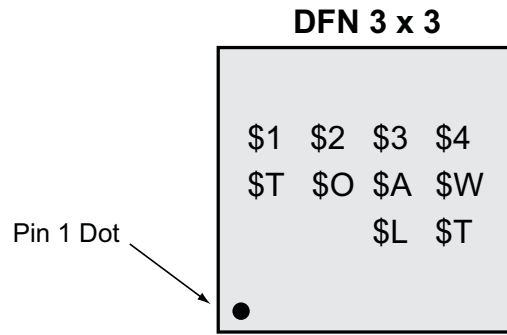
UNIT: mm

Tape Size	Reel Size	M	N	W1	H	S	K	R
8mm	ø180	ø180.00 ±0.50	60.0 ±0.50	8.4 +1.5/-0	13.0 ±0.20	1.5 Min.	13.5 Min.	3.0 ±0.50

#### Leader/Trailer and Orientation



**Package Marking**



**This datasheet contains preliminary data; supplementary data may be published at a later date. Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.**

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