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2Mb Ultra-Low Power Asynchronous CMOS SRAM

128K × 16bit

Overview

The N02L63W3A is an integrated memory device containing a 2 Mbit Static Random Access Memory organized as 131,072 words by 16 bits. The device is designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with a single chip enable ($\overline{CE}$) control and output enable ($\overline{OE}$) to allow for easy memory expansion. Byte controls ($\overline{UB}$ and $\overline{LB}$) allow the upper and lower bytes to be accessed independently. The N02L63W3A is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40°C to +85°C and is available in JEDEC standard packages compatible with other standard 128Kb x 16 SRAMs.

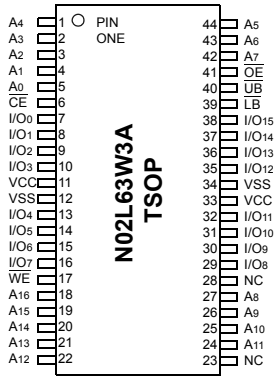
Features

- **Single Wide Power Supply Range**
  2.3 to 3.6 Volts
- **Very low standby current**
  2.0µA at 3.0V (Typical)
- **Very low operating current**
  2.0mA at 3.0V and 1µs (Typical)
- **Very low Page Mode operating current**
  0.8mA at 3.0V and 1µs (Typical)
- **Simple memory control**
  Single Chip Enable ($\overline{CE}$)
  Byte control for independent byte operation
  Output Enable ($\overline{OE}$) for memory expansion
- **Low voltage data retention**
  Vcc = 1.8V
- **Very fast output enable access time**
  30ns $\overline{OE}$ access time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**
- **Compact space saving BGA package available**

Product Family

Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed	Standby Current (I_{SB}), Typical	Operating Current (Icc), Typical
N02L63W3AB	48 - BGA	-40°C to +85°C	2.3V - 3.6V	55ns @ 2.7V 70ns @ 2.3V	2 µA	2 mA @ 1MHz
N02L63W3AT	44 - TSOP II					
N02L63W3AB2	48 - BGA Green					
N02L63W3AT2	44 - TSOP II Green					

Pin Configurations



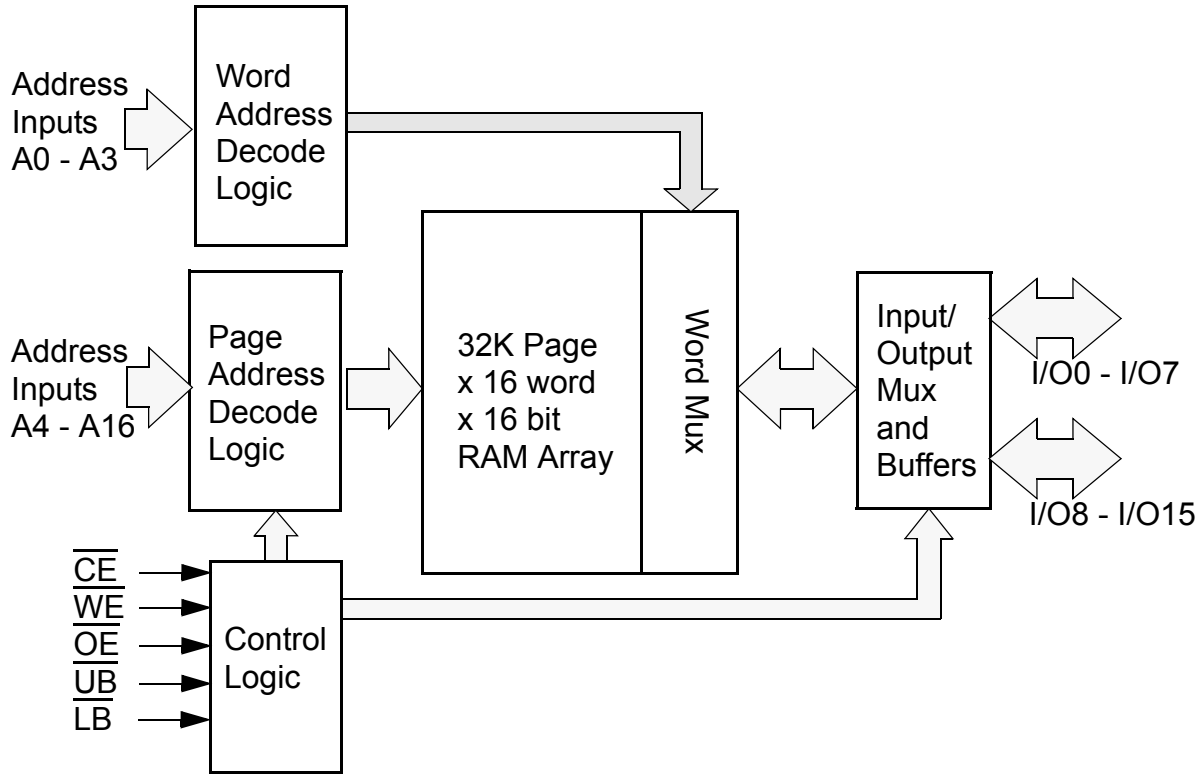
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	NC	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	NC	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	NC	A_8	A_9	A_{10}	A_{11}	NC

48 Pin BGA (top)
6 x 8 mm

Pin Descriptions

Pin Name	Pin Function
A_0-A_{16}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Enable Input
$\overline{UB}$	Upper Byte Enable Input
I/O_0-I/O_{15}	Data Inputs/Outputs
NC	Not Connected
V_{CC}	Power
V_{SS}	Ground

Functional Block Diagram



Functional Description

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O_0 - I/O_{15}[1]	MODE	POWER
H	X	X	X	X	High Z	Standby[2]	Standby
L	X	X	H	H	High Z	Active	Active
L	L	X[3]	L[1]	L[1]	Data In	Write[3]	Active
L	H	L	L[1]	L[1]	Data Out	Read	Active
L	H	H	X	X	High Z	Active	Active

1. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - I/O_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown.
2. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
3. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec	°C

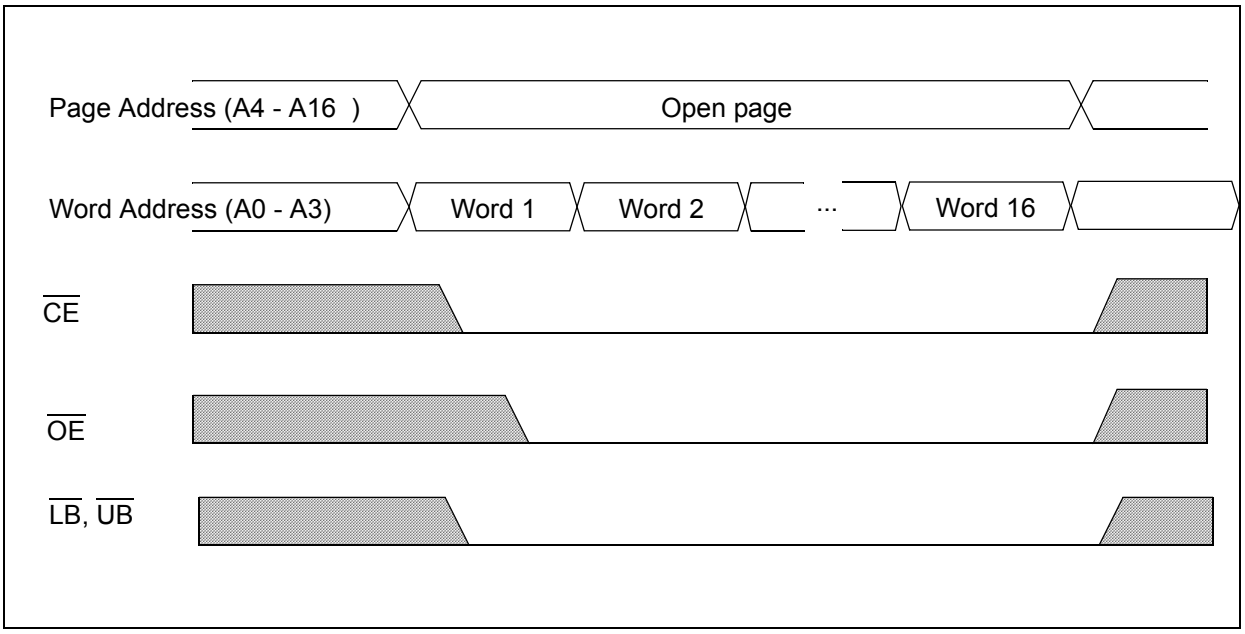
1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Test Conditions	Min.	Typ[1]	Max	Unit
Supply Voltage	V_{CC}		2.3		3.6	V
Data Retention Voltage	V_{DR}	Chip Disabled[2]	1.8			V
Input High Voltage	V_{IH}		1.8		V_{CC}+0.3	V
Input Low Voltage	V_{IL}		–0.3		0.6	V
Output High Voltage	V_{OH}	I_{OH} = 0.2mA	V_{CC}–0.2			V
Output Low Voltage	V_{OL}	I_{OL} = -0.2mA			0.2	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}			0.5	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled			0.5	µA
Read/Write Operating Supply Current @ 1 µs Cycle Time[2]	I_{CC1}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		2.0	4.0	mA
Read/Write Operating Supply Current @ 70 ns Cycle Time[2]	I_{CC2}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		12	16.0	mA
Page Mode Operating Supply Current @ 70ns Cycle Time[2] (Refer to Power Savings with Page Mode Operation diagram)	I_{CC3}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		4		mA
Read/Write Quiescent Operating Supply Current[3]	I_{CC4}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0, f = 0			3.0	mA
Maximum Standby Current[3]	I_{SB1}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 85°C, VCC = 3.6 V		2.0	20	µA
Maximum Data Retention Current[3]	I_{DR}	V_{CC} = 1.8V, V_{IN} = V_{CC} or 0 Chip Disabled, t_A= 85°C			10	µA

1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and are not 100% tested.
2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
3. This device assumes a standby mode if the chip is disabled ($\overline{CE}$ high). In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS

Power Savings with Page Mode Operation ($\overline{WE}$ = V_{IH})



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 16-bit words of data are read from the open page. By treating addresses A0-A3 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

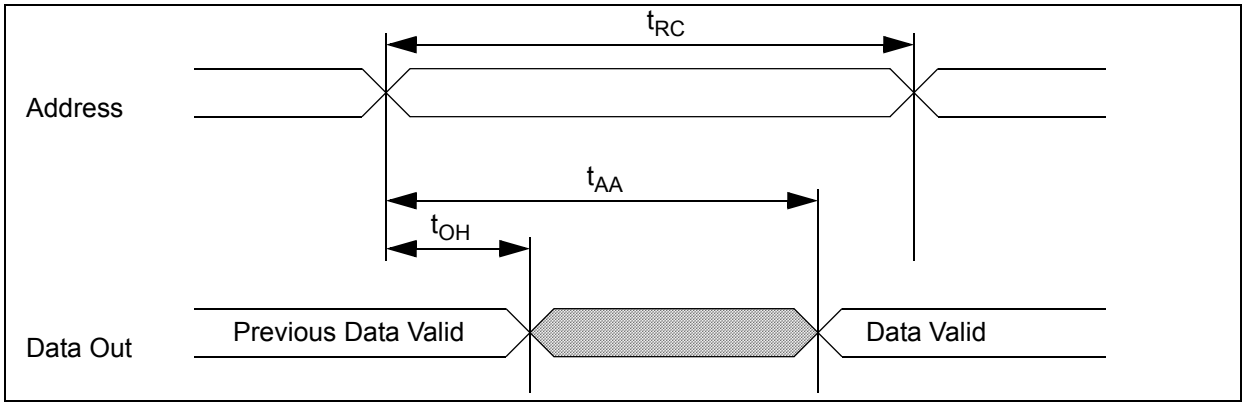
Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Output Load	CL = 30pF
Operating Temperature	-40 to +85 ^{O}C

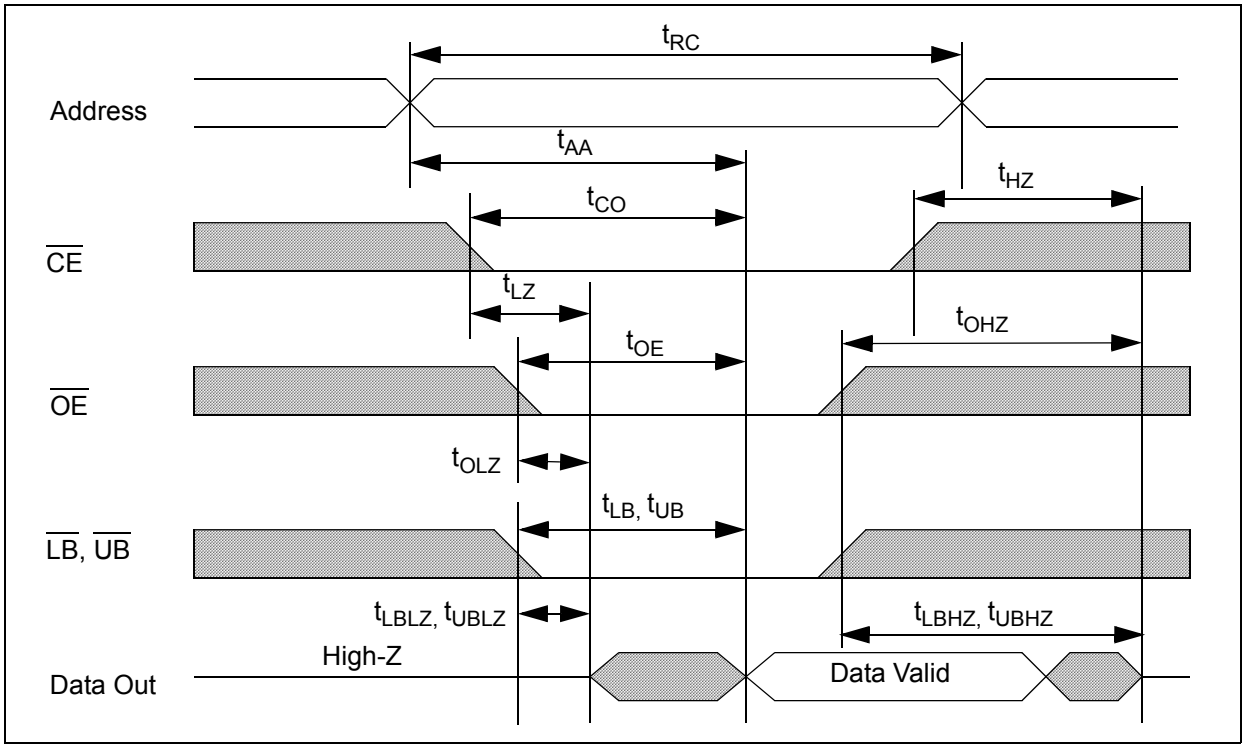
Timing

Item	Symbol	2.3 - 3.6 V		2.7 - 3.6 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	70		55		ns
Address Access Time	t_{AA}		70		55	ns
Chip Enable to Valid Output	t_{CO}		70		55	ns
Output Enable to Valid Output	t_{OE}		35		30	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		35		30	ns
Chip Enable to Low-Z output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	10		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	20	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	20	ns
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	0	20	0	20	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Write Cycle Time	t_{WC}	70		55		ns
Chip Enable to End of Write	t_{CW}	50		40		ns
Address Valid to End of Write	t_{AW}	50		40		ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	50		40		ns
Write Pulse Width	t_{WP}	40		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		20		20	ns
Data to Write Time Overlap	t_{DW}	40		35		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	10		10		ns

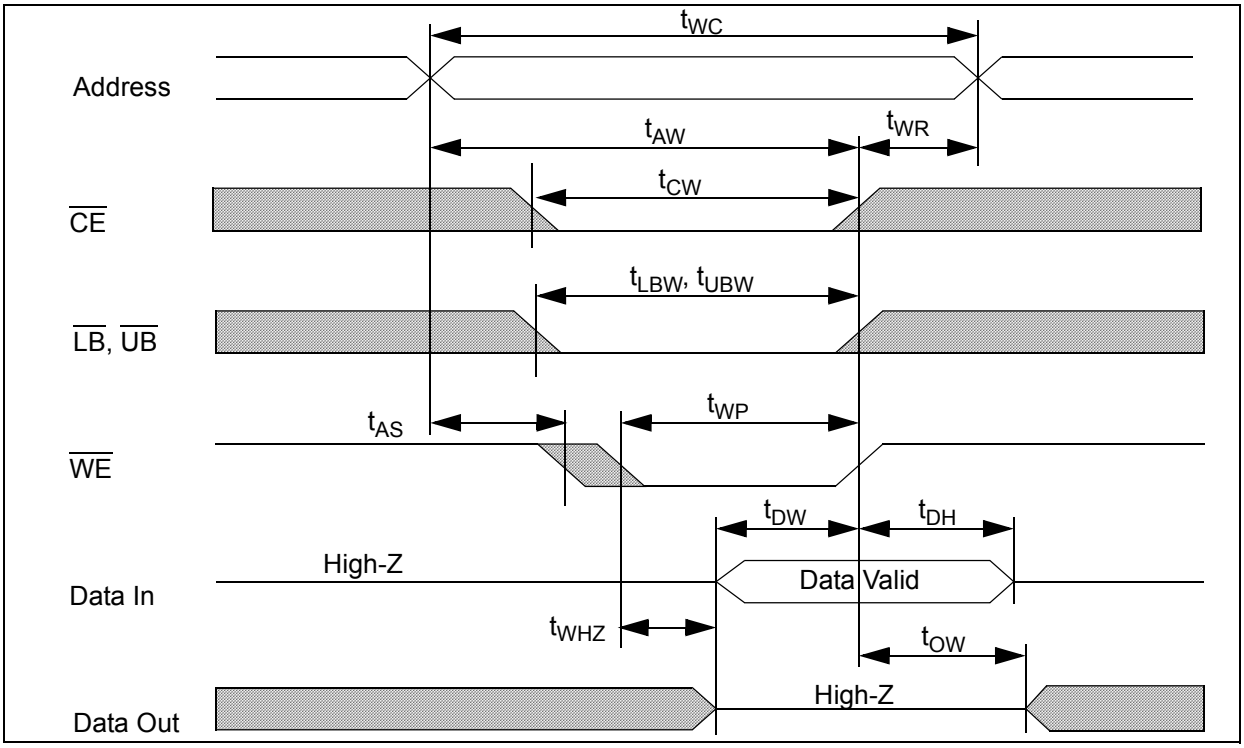
Timing of Read Cycle ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



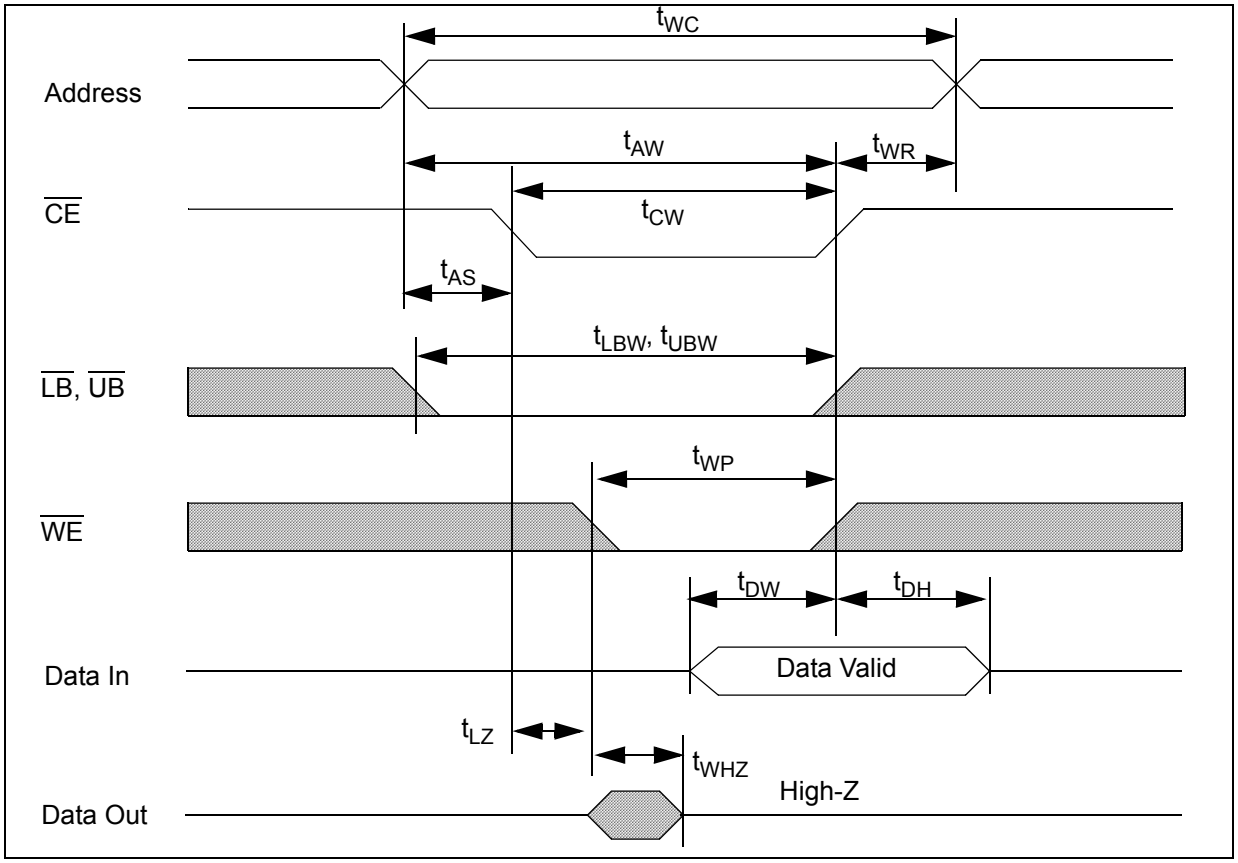
Timing Waveform of Read Cycle ($\overline{WE}$= V_{IH})



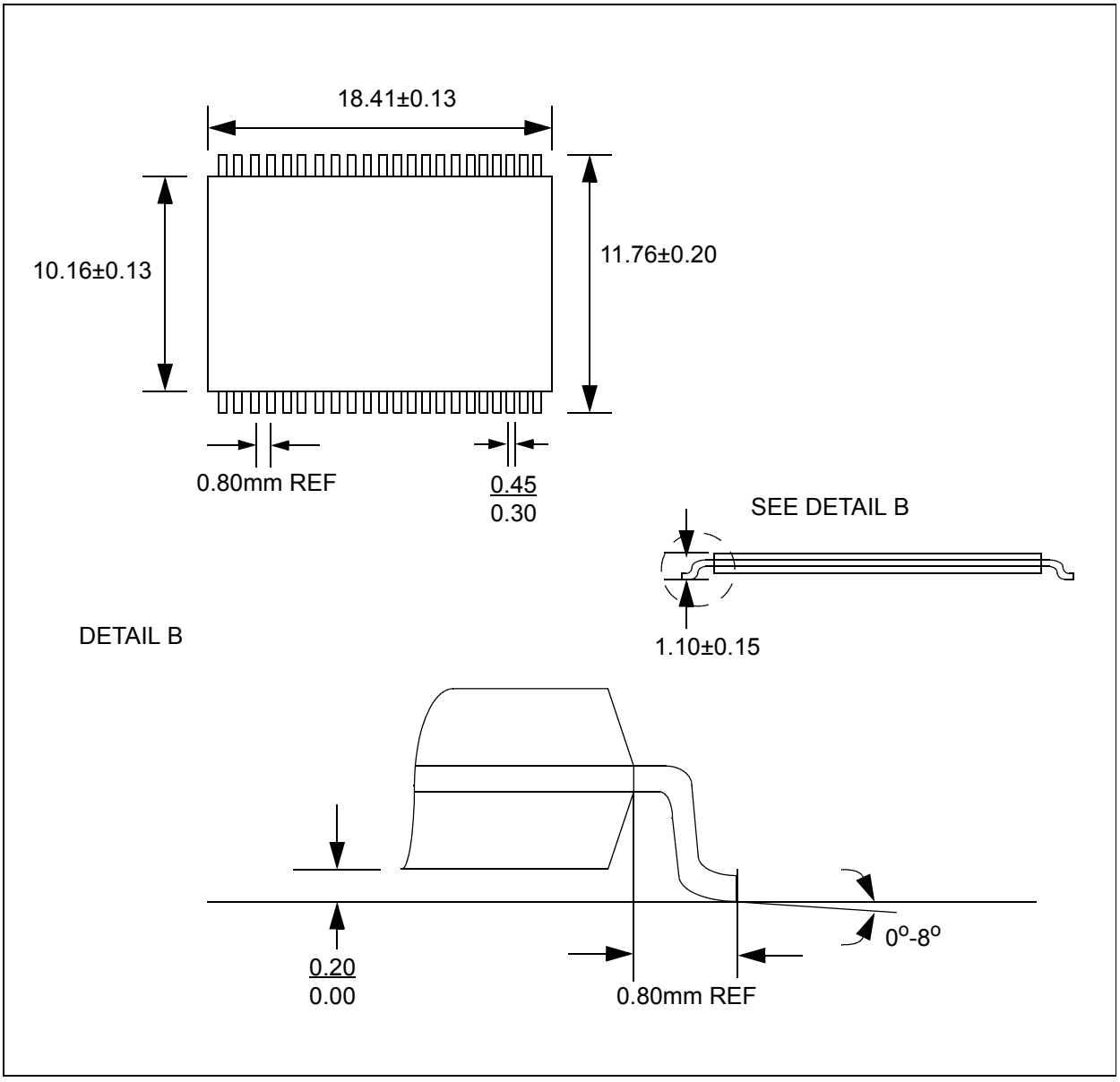
Timing Waveform of Write Cycle ($\overline{WE}$ control)



Timing Waveform of Write Cycle ($\overline{CE}$ Control)

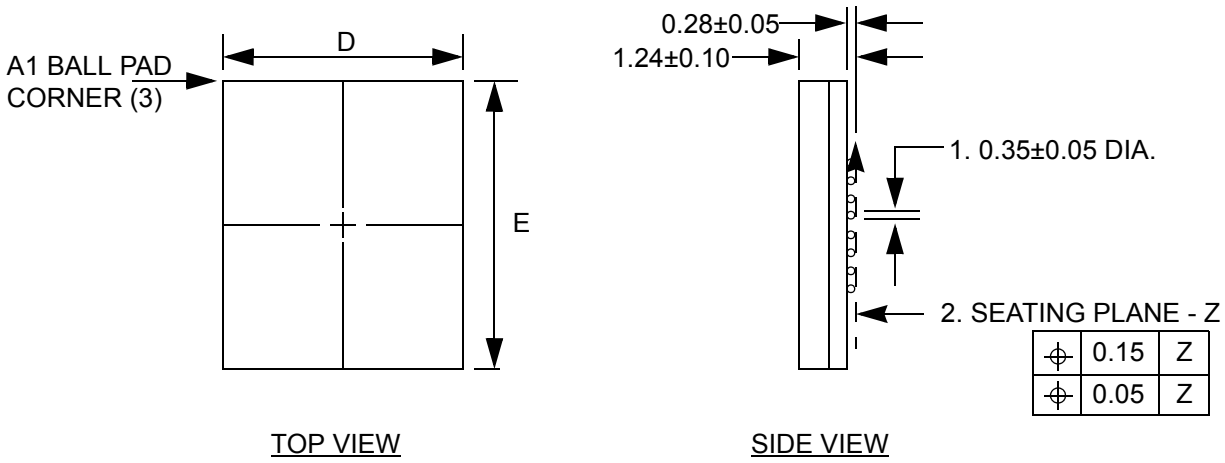


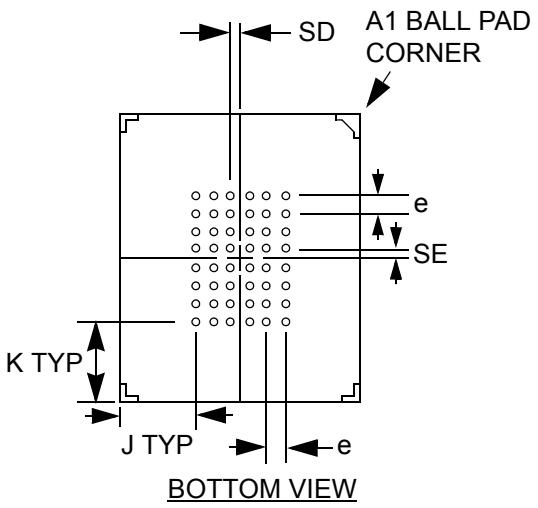
44-Lead TSOP II Package (T44)



Note:
1. All dimensions in inches (Millimeters)
2. Package dimensions exclude molding flash

Ball Grid Array Package





1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

Ordering Information

Part Number	Package	Shipping Method
N02L63W3AT5I	Leaded 44-TSOP II	Tray
N02L63W2AT25I	Green 44-TSOP II (RoHS Compliant)	Tray
N02L63W3AB5I	Leaded 48-BGA	Tray
N02L63W3AB25I	Green 48-BGA (RoHS Compliant)	Tray
N02L63W3AT5IT	Leaded 44-TSOP II	Tape & Reel
N02L63W3AT25IT	Green 44-TSOP II (RoHS Compliant)	Tape & Reel
N02L63W3AB5IT	Leaded 48-BGA	Tape & Reel
N02L63W3AB25IT	Green 48-BGA (RoHS Compliant)	Tape & Reel

Revision History

Revision #	Date	Change Description
A	Dec. 1999	Initial Preliminary Release
B	Sept. 2000	Modified Voltage Range and Standby Current Limits.
C	Oct. 2000	Added Missing Tas Parameter Specification.
D	Oct. 2000	Modified Standby Current Specifications.
E	Jan. 2001	Extensive Modification to use voltage regulator design
F	Mar. 2001	Modified BGA pinout, access time 70ns @ 2.7V, misc. errata
G	May 2001	Changed access time to 55ns, modified 44-Lead TSOP Package diagram
H	June 2001	Revised voltage range in Timing table, revised Dimensions table
I	Sept. 2001	Minor parametric modifications, full production release
J	Dec. 2001	Part number change from EM128L16, modified Overview and Features, added Page Mode Operation diagram, revised Operating Characteristics table, Package diagram, Functional Description table and Ordering Information diagram
K	Nov. 2002	Replaced Isb and Icc on Product Family table with typical values
L	Oct. 2004	Added Pb-Free and Green Package Option
M	Nov. 2005	Removed Pb-Free Pkg, added Green Pkg and RoHS Compliant
N	September 2006	Converted to AMI Semiconductor
15	July 2008	Converted to ON Semiconductor and new part numbers

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