

0.4Ω Ultra Low ON-Resistance, Dual, SPDT Analog Switch

UM2268 QFN10 1.8×1.4

General Description

The UM2268 is a dual, low-power single-pole/double-throw (SPDT) analog switch that operates from a single +1.8V to +4.4V supply.

The UM2268 features guaranteed on-resistance matching (0.04Ω TYP) between switches and guaranteed on-resistance flatness over the signal range (0.08Ω TYP), as well as high off-isolation and low crosstalk. This ensures excellent linearity and low distortion when switching audio signals.

The UM2268 is available in Pb-free QFN10 package (1.8mm×1.4mm×0.55mm).

Applications

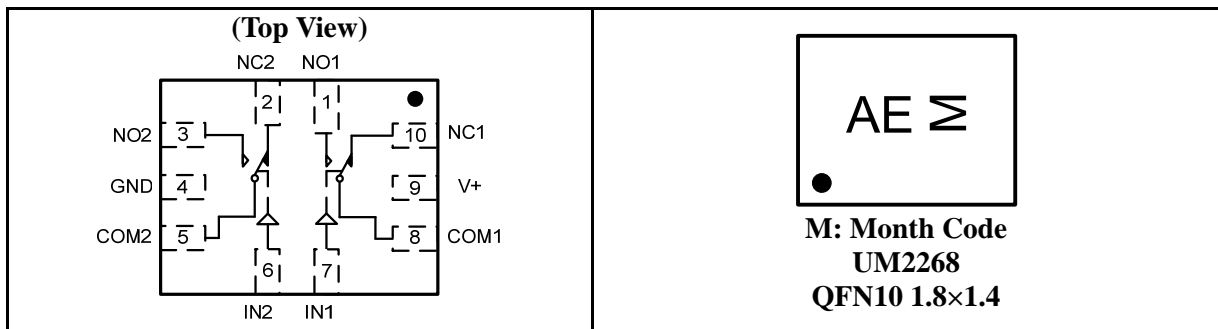
- Portable Instrumentation
- Battery-Operated Equipment
- Computer Peripherals
- Speaker and Earphone Switching
- Medical Equipment
- Audio and Video Switching

Features

- V_{CC} Operating Range: +1.8V to +4.4V
- Low On-Resistance: 0.4Ω (TYP) @ +4.4V
- On-Resistance Matching: 0.04Ω (TYP)
- On-Resistance Flatness: 0.08Ω (TYP)
- -3dB Bandwidth: 80MHz
- Low Off-Isolation: -78dB (100kHz)
- Low Crosstalk: -93dB (100kHz)
- TTL/CMOS Compatible
- Break-Before-Make Switching
- Rail-to-Rail Input and Output Operation
- Lead (Pb)-Free QFN10 Package

Pin Configurations

Top View



Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM2268	QFN10 1.8×1.4	AE	3000pcs/7 Inch Tape & Reel

Pin Description

Pin Number	Pin Name	Function
1, 3	NO1, NO2	Normally-Open Terminal
10, 2	NC1, NC2	Normally-Closed Terminal
4	GND	Ground
8, 5	COM1, COM2	Common Terminal
7, 6	IN1, IN2	Digital Control Pin to Connect the COM Terminal to the NO or NC Terminals
9	V+	Power Supply

Function Table

LOGIC	NO	NC
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Symbol	Parameter	Limit	Unit
V ₊	Supply Voltage	0 to +4.6	V
V _{IS}	Analog Switch Input Voltage	-0.3 to (V _{CC} +0.3)	
V _{IN}	Digital Select Input Voltage	0 to +4.6	
I _D	Continuous DC Current	250	mA
I _P	Peak Current	350	mA
T _O	Operating Temperature Range	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	
ESD	HBM	4000	V

Electrical Characteristics

$V_+ = +4.4V$, $GND = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.

Symbol	Parameter	Test Conditions	Vcc (V)	Temp	Limits (-40°C to 85°C)			Unit
					Min	Typ (Note 1)	Max	
V_+	Power Supply Range			Full	1.8		4.4	V
I_{CC}	Quiescent Supply Current	$V_{IN} = V_+$ or 0	4.4	Full			1.0	μA
I_{IN}	Input Leakage Current	$V_{IN} = 0V/4.4V$	4.4	Full			1.0	μA
I_{OFF}	Power Off Leakage Current	$V_{NO}/V_{NC} = 3.3V/0.3V$, $V_{COM} = 0.3V/3.3V$	4.4	Full			1.0	μA
I_{ON}	Channel ON Leakage Current	$V_{COM} = 0.3V/3.3V$ V_{NO} or $V_{NC} = 0.3V/3.3V$, or Floating	4.4	Full			1.0	μA
R_{ON}	On-Resistance (Note 2)	V_{NO}, V_{NC} or $V_{COM} = 1.0V$, $I_{COM} = -100mA$	4.4	Room Full		0.4	0.75 0.85	Ω
ΔR_{ON}	On Resistance Match Between Channels (Note 2, 3, 4)	V_{NO}, V_{NC} or $V_{COM} = 1.0V$, $I_{COM} = -100mA$	4.4	Room Full		0.04	0.15 0.20	Ω
R_{FLAT}	On Resistance Flatness (Note 2, 3, 5)	V_{NO}, V_{NC} or $V_{COM} = 1.0V, 2.5V$ $I_{COM} = -100mA$	4.4	Room Full		0.08	0.12 0.20	Ω
V_{IH}	Input High Voltage		4.4	Full	2.0			V
V_{IL}	Input Low Voltage		4.4	Full			0.5	V
t_{ON}	Turn On Time	$V_{IN} = 2.1V$ to $0V$, $R_L = 50\Omega$, $C_L = 35pF$, V_{NO1} or $V_{NC1} = V_{NO2}$ or $V_{NC2} = 2.1V$, Test Circuit 1	4.4	Room		88		ns
t_{OFF}	Turn Off Time	$V_{IN} = 2.1V$ to $0V$, $R_L = 50\Omega$, $C_L = 35pF$, V_{NO1} or $V_{NC1} = V_{NO2}$ or $V_{NC2} = 2.1V$, Test Circuit 1	4.4	Room		16		ns
t_{BBM}	Break Before Make Time (Note 6)	$V_{IN} = 2.1V$ to $0V$, $R_L = 50\Omega$, $C_L = 35pF$, V_{NO1} or $V_{NC1} = V_{NO2}$ or $V_{NC2} = 2.1V$, Test Circuit 2	4.4	Room		6		ns
O_{IRR}	Off Isolation (Note 7)	$V_{BIAS} = 2.1V$, Signal=0dBm, Test Circuit 3	4.4	Room		-78		dB
				Room		-58		dB
X_{TALK}	Crosstalk	$V_{BIAS} = 2.1V$, Signal=0dBm, Test Circuit 4	4.4	Room		-93		dB
				Room		-90		dB
BW	-3dB Bandwidth	$V_{BIAS} = 2.1V$, Signal=0dBm, Test Circuit 5	4.4	Room		80		MHz
Q	Charge Injection Select Input to Common I/O	$V_G = 0V$, $R_S = 0\Omega$, $C_L = 1.0nF$, Test Circuit 6	4.4	Room		4.0		pC
C_{ON}	HSD+ HSD- ON Capacitance (Note 8)		4.4	Room		56		pF

Note 1: Typically values are at $V_+ = 4.4V$ and $T_A = +25^\circ C$.

Note 2: Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

Note 3: Parameter is characterized but not tested in production.

Note 4: $\Delta R_{ON} = |R_{ON(NO1/NC1)} - R_{ON(NO2/NC2)}|$ measured at identical V_{CC} , temperature and voltage levels.

Note 5: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

Note 6: Guaranteed by design.

Note 7: Off Isolation = $20 \log_{10} [V_{COM}/V_{NO/NC}]$.

Note 8: $T_A = +25^\circ C$, $f = 1MHz$, Capacitance is characterized but not tested in production.

Electrical Characteristics

$V_+ = +2.7V$ to $+3.6V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.

Symbol	Parameter	Test Conditions	Vcc (V)	Temp	Limits (-40°C to 85°C)			Unit
					Min	Typ (Note 1)	Max	
V_{NO}, V_{NC}, V_{COM}	Analog Signal Range			Full	0		V+	V
I_{IN}	Input Leakage Current	$V_{IN}=0V/2.7V$	2.7	Full			1.0	μA
I_{OFF}	Power Off Leakage Current	$V_{NO}/V_{NC}=3.3V/0.3V,$ $V_{COM}=0.3V/3.3V$	3.6	Full			1.0	μA
I_{ON}	Channel ON Leakage Current	$V_{COM}=0.3V/3.3V$ V_{NO} or $V_{NC}=0.3V/3.3V$, or Floating	3.6	Full			1.0	μA
R_{ON}	On-Resistance (Note 2)	V_{NO}, V_{NC} or $V_{COM}=1.0V,$ $I_{COM}=-100mA$	2.7	Room Full		0.75	1.10 1.20	Ω
ΔR_{ON}	On Resistance Match Between Channels (Note 2, 3, 4)	V_{NO}, V_{NC} or $V_{COM}=1.0V,$ $I_{COM}=-100mA$	2.7	Room Full		0.03	0.15 0.20	Ω
R_{FLAT}	On Resistance Flatness (Note 2, 3, 5)	V_{NO}, V_{NC} or $V_{COM}=1.0V, 2.5V$ $I_{COM}=-100mA$	2.7	Room Full		0.10	0.18 0.20	Ω
V_{IH}	Input High Voltage		3.0	Full	1.5			V
V_{IL}	Input Low Voltage		3.0	Full			0.4	V
t_{ON}	Turn On Time	$V_{IN}=1.5V$ to $0V,$ $R_L=50\Omega, C_L=35pF,$ V_{NO1} or $V_{NC1}=V_{NO2}$ or $V_{NC2}=1.5V, \text{Test Circuit 1}$	3.0	Room		100		ns
t_{OFF}	Turn Off Time	$V_{IN}=1.5V$ to $0V,$ $R_L=50\Omega, C_L=35pF,$ V_{NO1} or $V_{NC1}=V_{NO2}$ or $V_{NC2}=1.5V, \text{Test Circuit 1}$	3.0	Room		20		ns
t_{BBM}	Break Before Make Time (Note 6)	$V_{IN}=1.5V$ to $0V,$ $R_L=50\Omega, C_L=35pF,$ V_{NO1} or $V_{NC1}=V_{NO2}$ or $V_{NC2}=1.5V, \text{Test Circuit 2}$	3.0	Room		9.2		ns
O_{IRR}	Off Isolation (Note 7)	$V_{BIAS}=2.1V,$ Signal=0dBm, Test Circuit 3	3.0	Room			-78	dB
				Room			-58	dB
X_{TALK}	Crosstalk	$V_{BIAS}=2.1V,$ Signal=0dBm, Test Circuit 4	3.0	Room			-93	dB
				Room			-90	dB
BW	-3dB Bandwidth	$V_{BIAS}=2.1V, \text{Signal}=0dBm,$ Test Circuit 5	3.0	Room		80		MHz
Q	Charge Injection Select Input to Common I/O	$V_G=0V, R_S=0\Omega,$ $C_L=1.0nF, \text{Test Circuit 6}$	3.0	Room		3.0		pC
C_{ON}	HSD+ HSD- ON Capacitance (Note 8)		3.0	Room		56		pF

Note 1: $T_A = +25^\circ C$.

Note 2: Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

Note 3: Parameter is characterized but not tested in production.

Note 4: $\Delta R_{ON} = |R_{ON(NO1/NC1)} - R_{ON(NO2/NC2)}|$ measured at identical V_{CC} , temperature and voltage levels.

Note 5: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

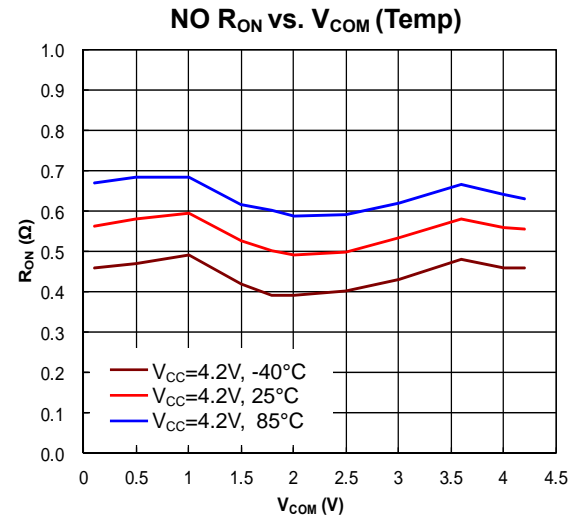
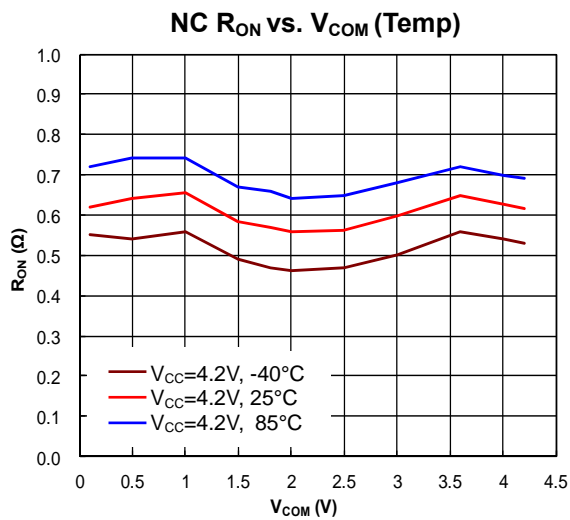
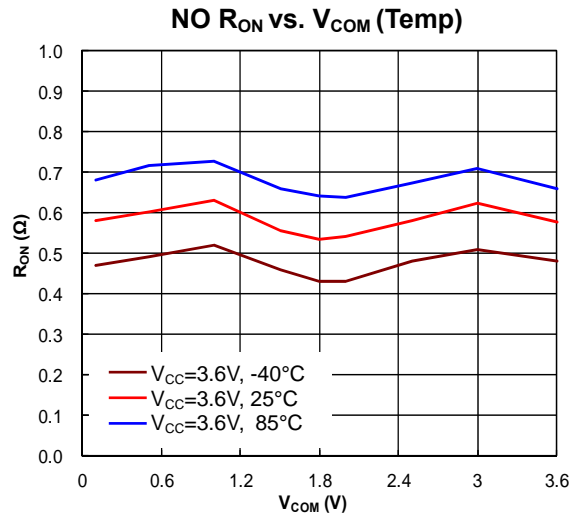
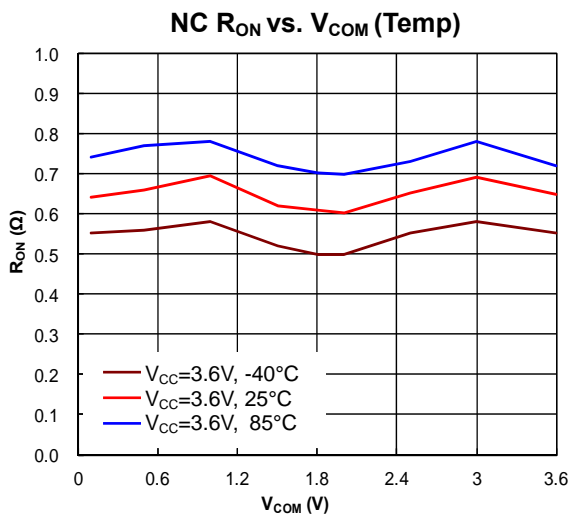
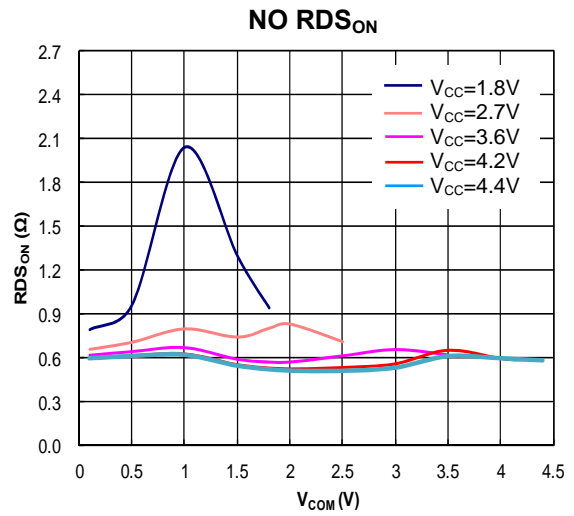
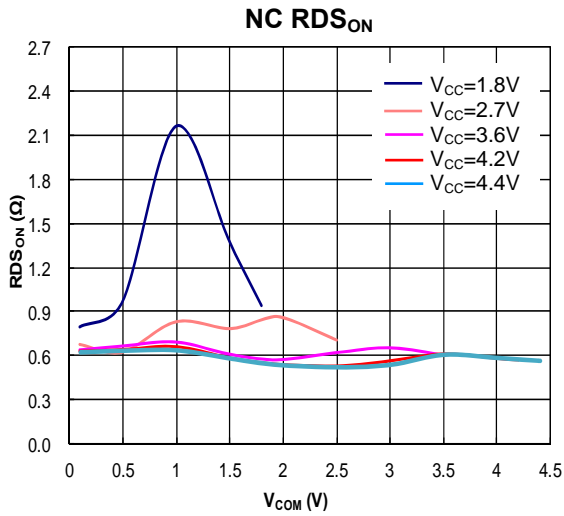
Note 6: Guaranteed by design.

Note 7: Off Isolation = $20 \log_{10} [V_{COM}/V_{NO/NC}]$.

Note 8: $T_A = +25^\circ C$, $f=1MHz$, Capacitance is characterized but not tested in production.

Typical Operating Characteristics

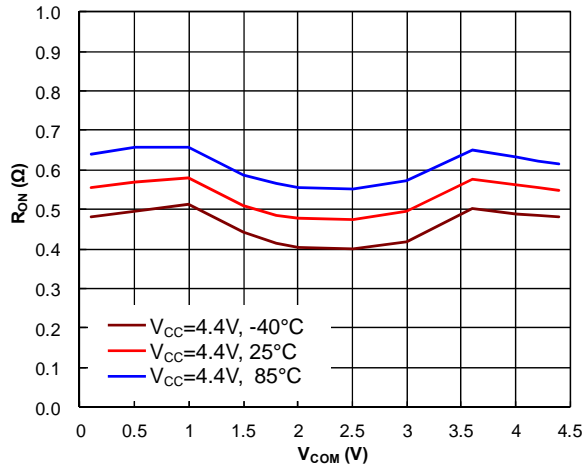
($T_A=+25^\circ\text{C}$, unless otherwise noted.)



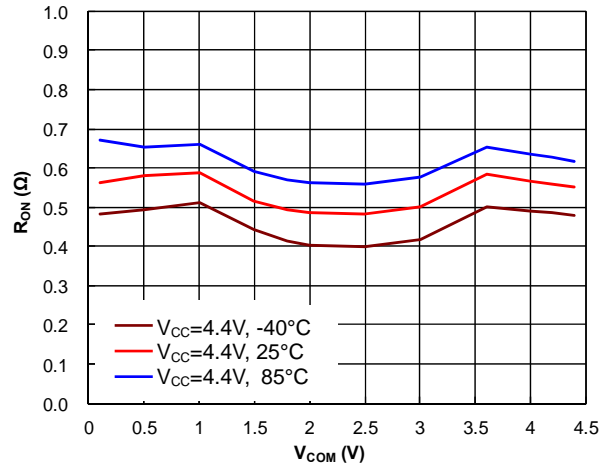
Typical Operating Characteristics (Continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

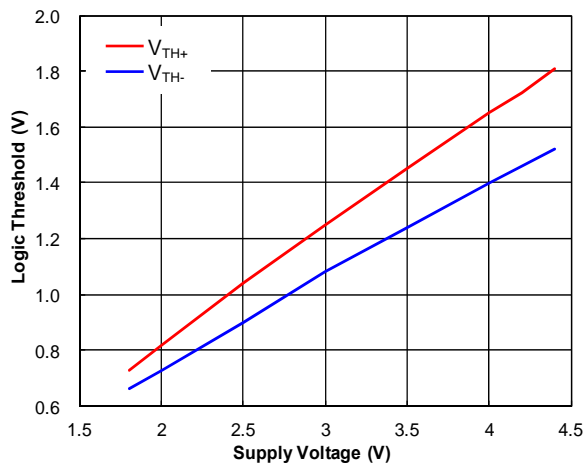
NC R_{ON} vs. V_{COM} (Temp)



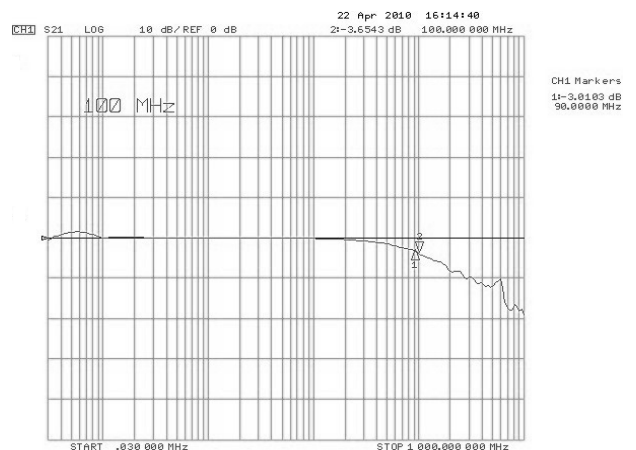
NO R_{ON} vs. V_{COM} (Temp)



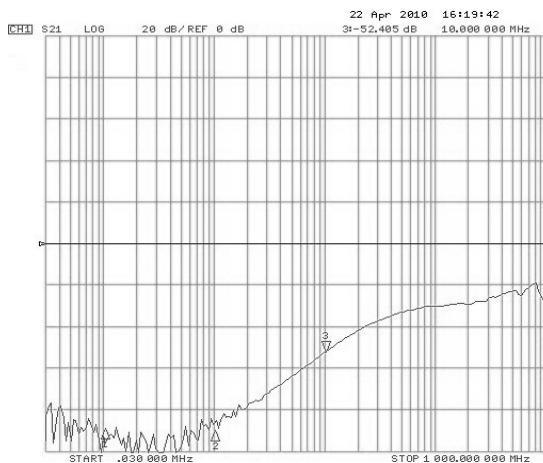
Logic Threshold vs. Supply Voltage



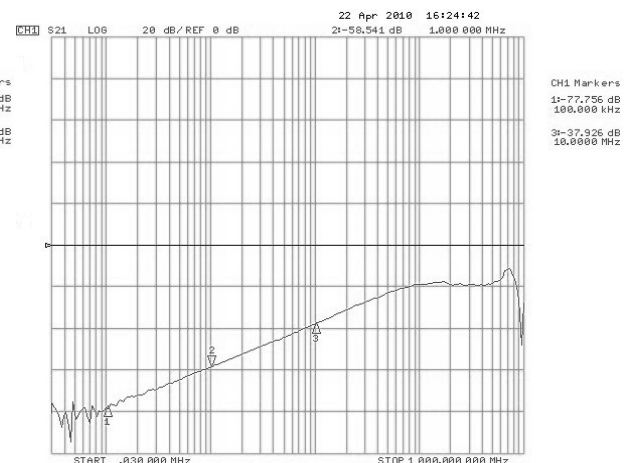
Bandwidth



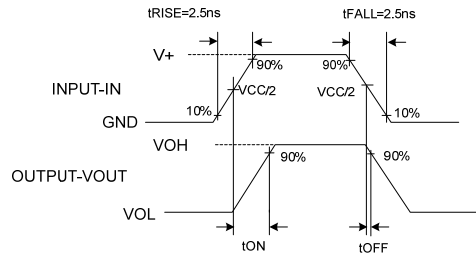
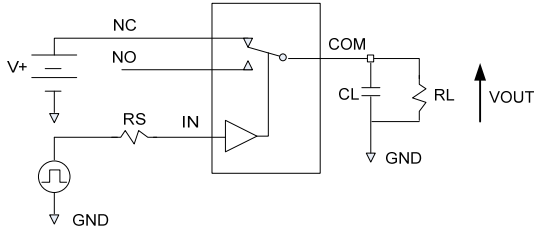
Crosstalk



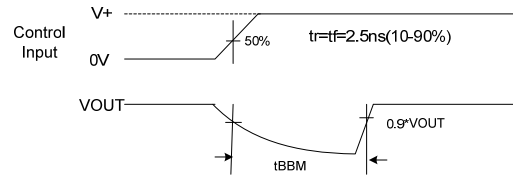
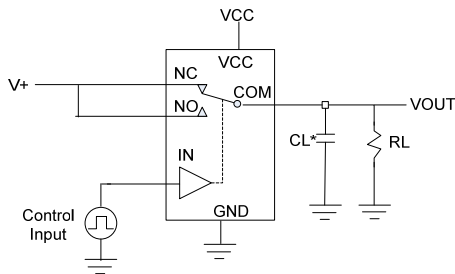
Off Isolation



Test Circuits

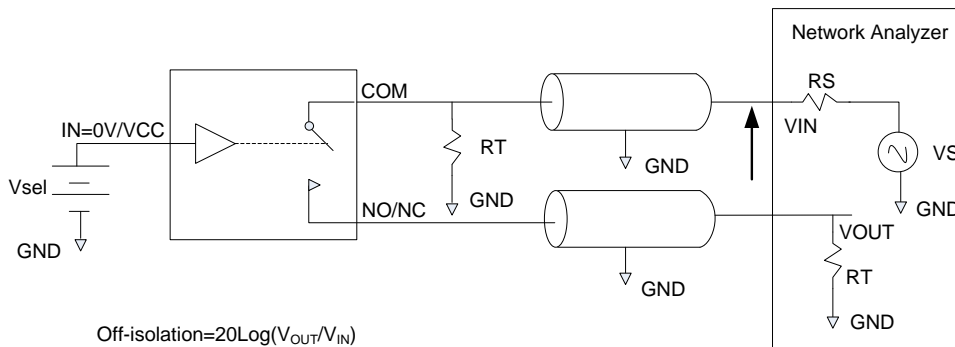


Test Circuit 1. Switching Timing (t_{ON} , t_{OFF})



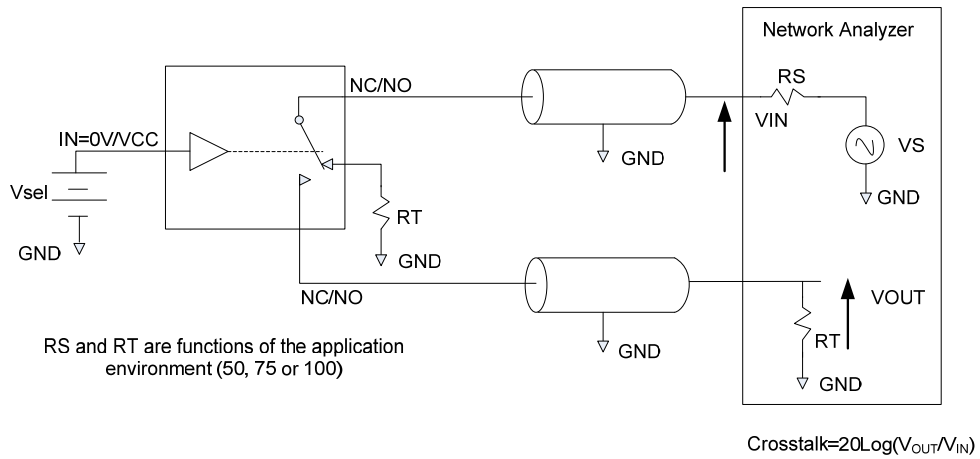
CL* includes fixture and stray capacitance

Test Circuit 2. Break-Before-Make Timing

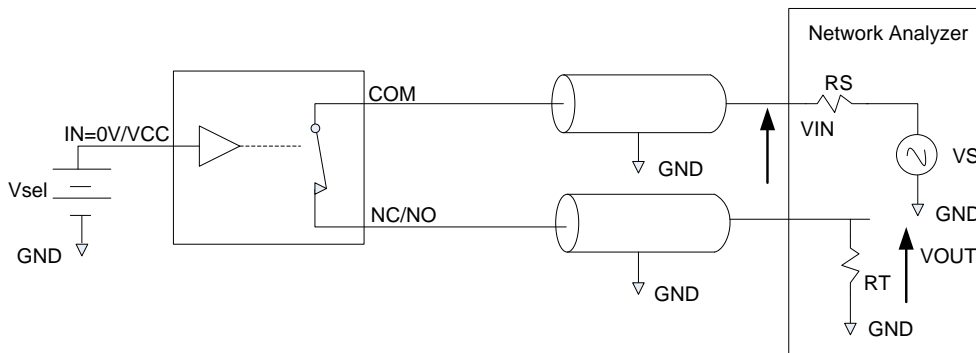


Off-isolation= $20\text{Log}(V_{OUT}/V_{IN})$

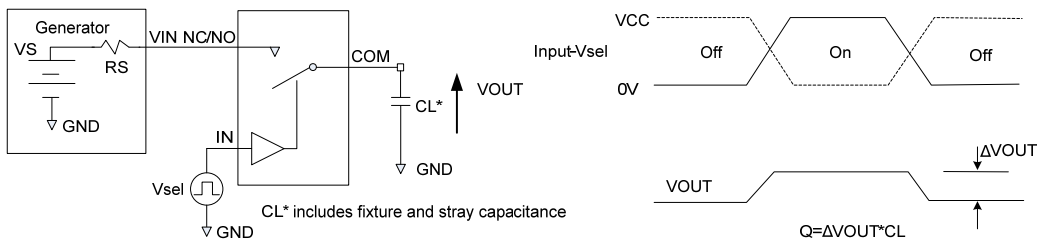
Test Circuit 3. Off-Isolation



Test Circuit 4. Channel-to-Channel Crosstalk



Test Circuit 5. Bandwidth

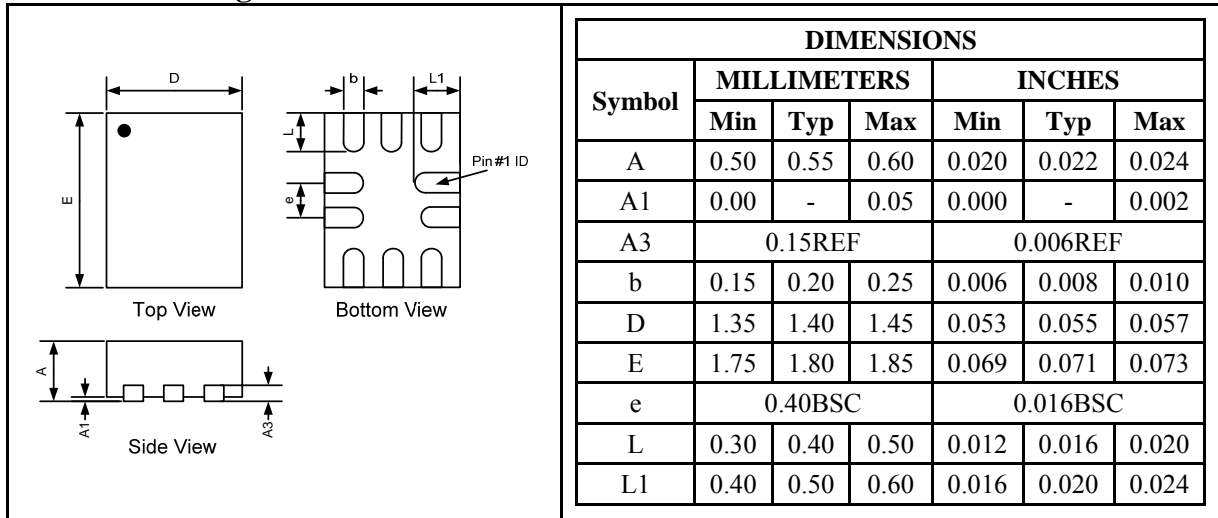


Test Circuit 6. Charge Injection Test

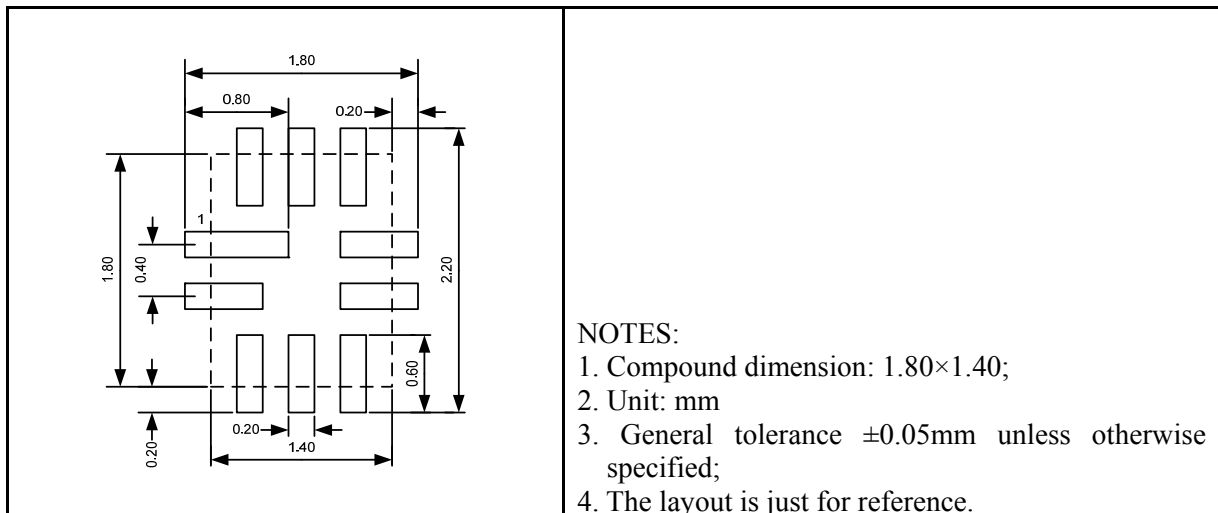
Package Information

UM2268 QFN10 1.8×1.4

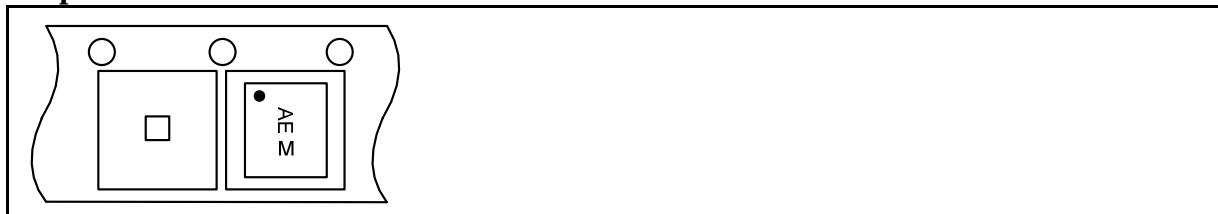
Outline Drawing



Land Pattern



Tape and Reel Orientation



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