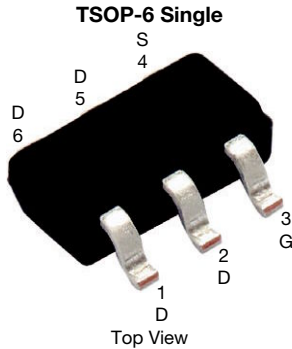


N-Channel 100 V (D-S) MOSFET

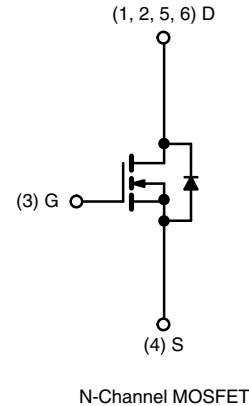


FEATURES

- High-efficiency PWM optimized
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available



PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.170
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 6$ V	0.185
Q_g typ. (nC)	5.5
I_D (A)	2.4
Configuration	Single

ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free	Si3430DV-T1-E3
Lead (Pb)-free and halogen-free	Si3430DV-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	5 s	STEADY STATE	UNIT
Drain-source voltage	V_{DS}	100	100	V
Gate-source voltage	V_{GS}	± 20	± 20	
Continuous drain current ($T_J = 175$ °C) ^a	I_D	$T_A = 25$ °C	2.4	A
		$T_A = 85$ °C	1.7	
Pulsed drain current	I_{DM}	8	8	mJ
Avalanche current	I_{AR}	6	6	
Repetitive avalanche energy (duty cycle ≤ 1 %)	E_{AR}	1.8	1.8	
Continuous source current (diode conduction) ^a	I_S	1.7	1	A
Maximum power dissipation ^a	P_D	$T_A = 25$ °C	2	W
		$T_A = 85$ °C	1	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	-55 to +150	°C

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^a	R_{thJA}	$t \leq 5$ s	45	62.5	°C/W
		Steady state	90	110	
Maximum junction-to-foot (drain)	R_{thJF}	25	30		

Note

a. Surface mounted on 1" x 1" FR4 board



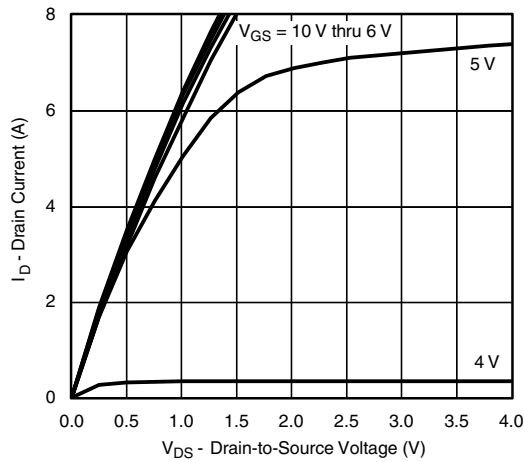
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{DS} , I _D = 250 μA	2	-	4.2	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 85 °C	-	-	25	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	8	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 2.4 A	-	0.148	0.170	Ω
		V _{GS} = 6 V, I _D = 2.3 A	-	0.160	0.185	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 2.4 A	-	7	-	S
Diode forward voltage ^a	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	-	0.8	1.2	V
Dynamic^b						
Total gate charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 2.4 A	-	5.5	8.2	nC
Gate-source charge	Q _{gs}		-	1.5	-	
Gate-drain charge	Q _{gd}		-	1.4	-	
Gate resistance	R _g		1	-	4	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω	-	9	20	ns
Rise time	t _r		-	11	20	
Turn-off delay time	t _{d(off)}		-	16	30	
Fall time	t _f		-	9	20	
Gate resistance	R _g	V _{GS} = 0.1 V, f = 5 MHz	-	2.8	-	Ω
Source-drain reverse recovery time	t _{rr}	I _F = 1.7 A, di/dt = 100 A/μs	-	50	80	ns

Notes

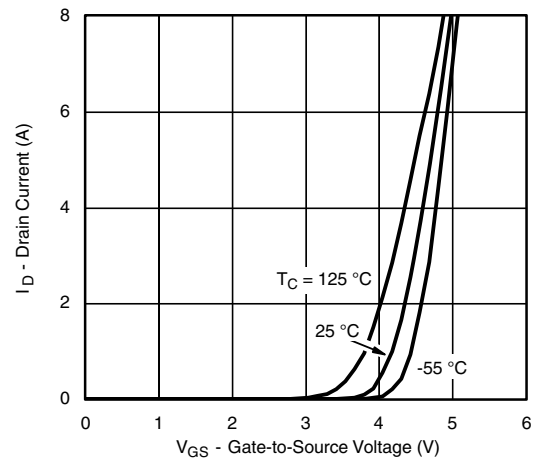
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

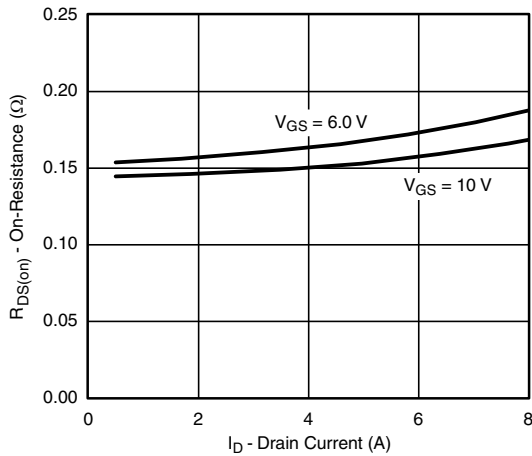
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



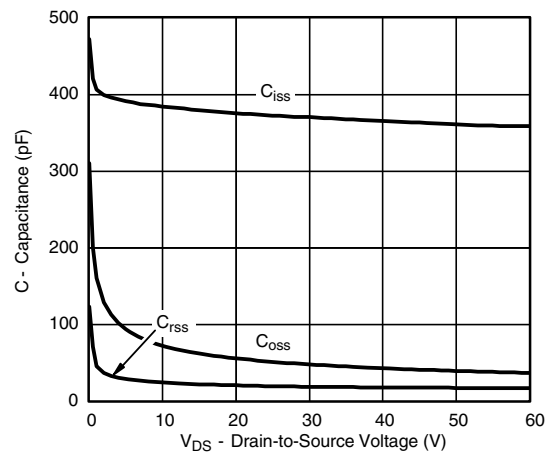
Output Characteristics



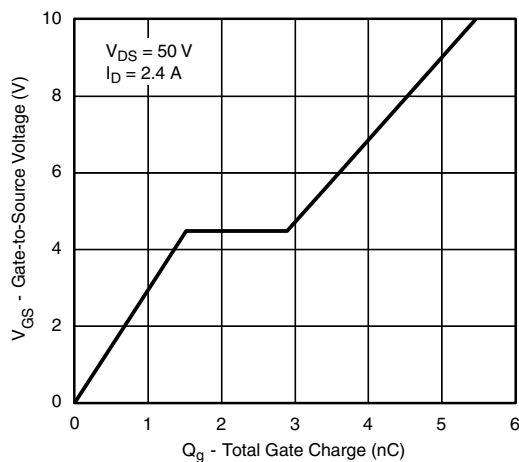
Transfer Characteristics



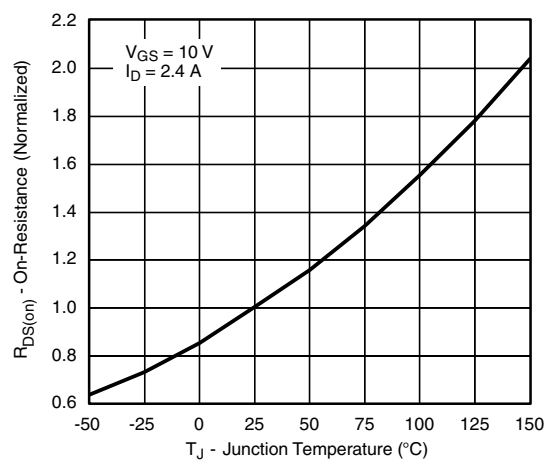
On-Resistance vs. Drain Current



Capacitance



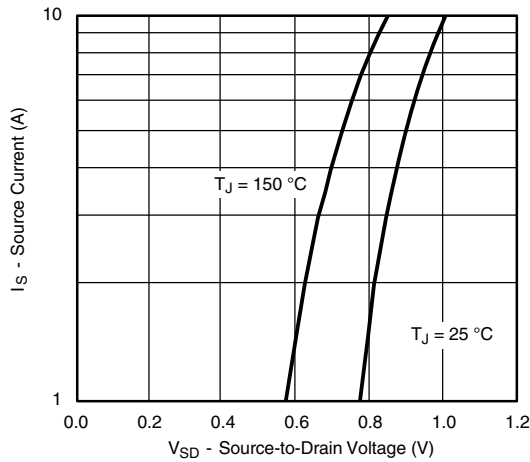
Gate Charge



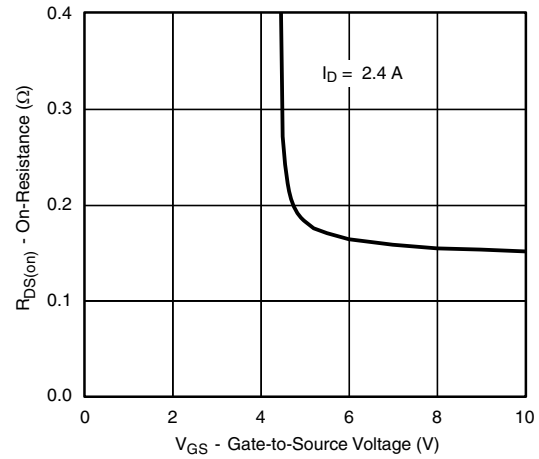
On-Resistance vs. Junction Temperature



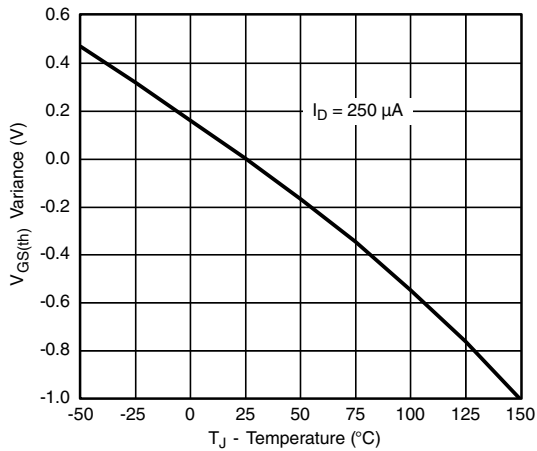
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



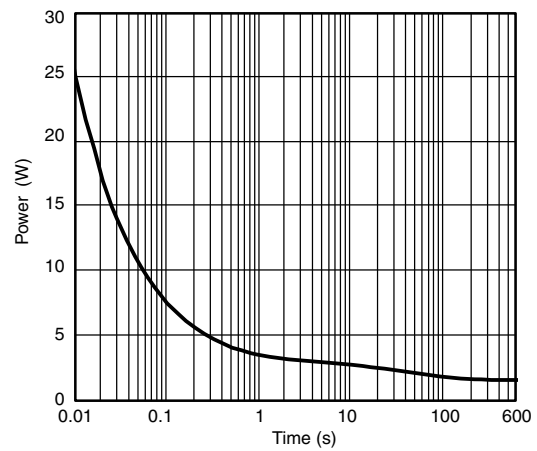
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



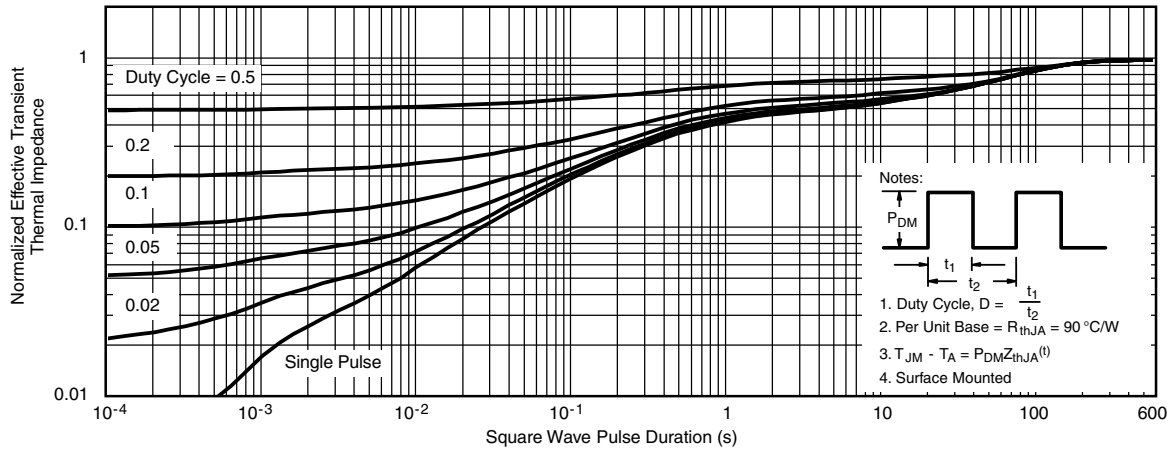
Threshold Voltage



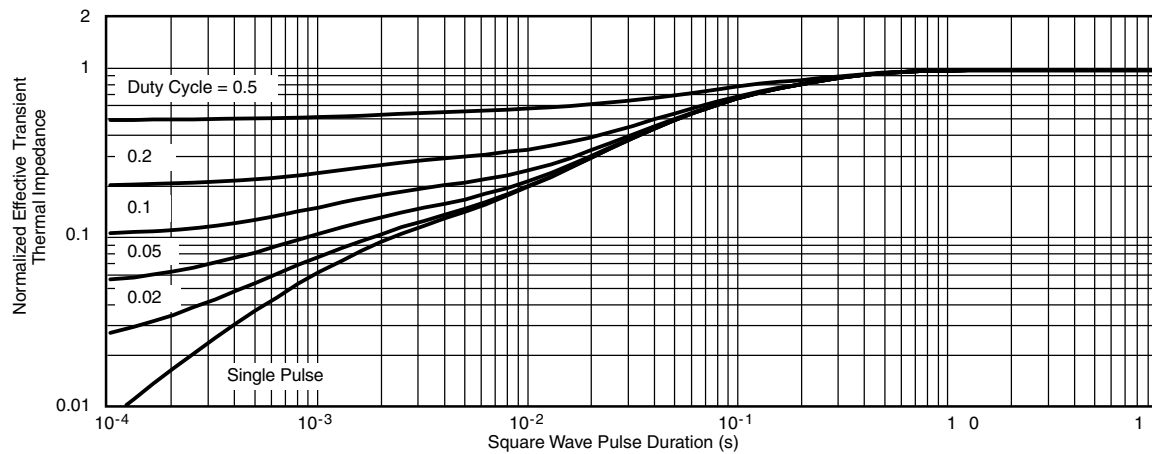
Single Pulse Power



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71235.



TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C



5-LEAD TSOP



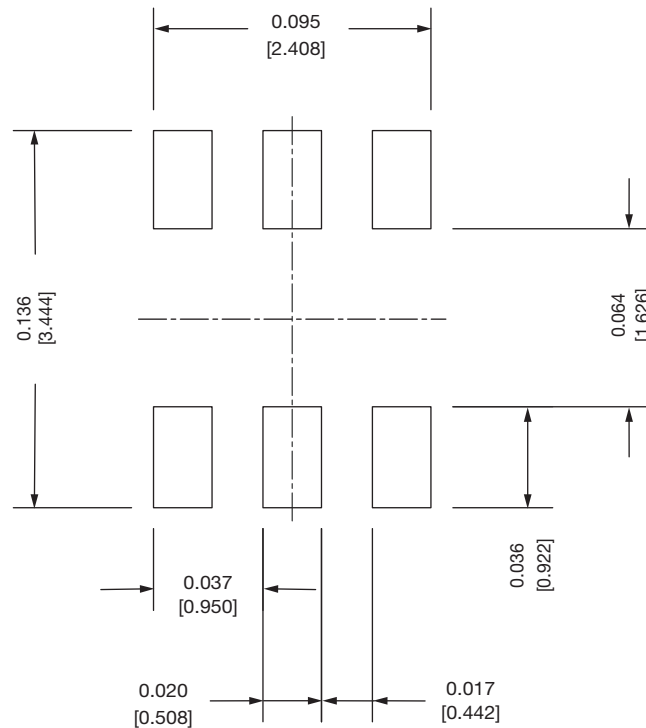
6-LEAD TSOP



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						



Recommended Land Pattern For TSOP-5L / TSOP-6L



Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
 DWG: 3010



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