ISO154x-Q1 Low-Power Bidirectional I²C Isolators

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
  - Device HBM ESD classification level 3A
  - Device CDM ESD classification level C6
- Functional Safety-Capable
  - Documentation available to aid functional safety system design: ISO1540-Q1, ISO1541-Q1
- Isolated bidirectional, I²C compatible, communication
- Supports up to 1-MHz operation
- 3-V to 5.5-V supply range
- Open-drain outputs With 3.5-mA Side 1 and 35-mA Side 2 sink current capability
- ±50-kV/µs transient immunity (Typical)
- Safety-related certifications:
  - 4242-V_{PK} isolation per DIN VDE V 0884-11:2017-01
  - 2500-V_{RMS} isolation for 1 minute per UL 1577
  - CSA approval per IEC 60950-1 and IEC 62368-1 end equipment standards
  - CQC basic insulation per GB4943.1-2011

2 Applications

- Electric and hybrid-electric vehicles
- Isolated I²C buses
- SMBus and PMBus interfaces
- Open-drain networks
- Motor control systems
- Battery management
- I²C level shifting

3 Description

The ISO1540-Q1 and ISO1541-Q1 devices are low-power, bidirectional isolators that are compatible with I²C interfaces. These devices have logic input and output buffers that are separated by Texas Instruments Capacitive Isolation technology using a silicon dioxide (SiO_2) barrier. When used with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

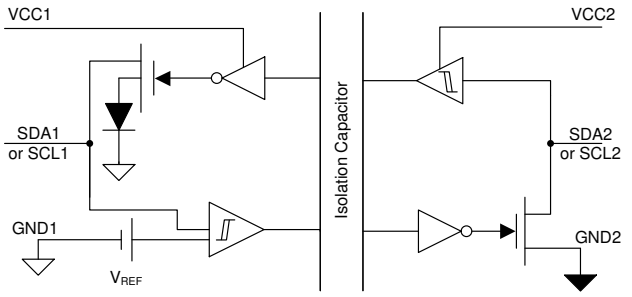
This isolation technology provides for function, performance, size, and power consumption advantages when compared to optocouplers. The ISO1540-Q1 and ISO1541-Q1 devices enable a complete isolated I²C interface to be implemented within a small form factor.

The ISO1540-Q1 has two isolated bidirectional channels for clock and data lines while the ISO1541-Q1 has a bidirectional data and a unidirectional clock channel. The ISO1541-Q1 is useful in applications that have a single master while the ISO1540-Q1 is suitable for multi-master applications. For applications where clock stretching by the slave is possible, the ISO1540-Q1 device should be used.

Isolated bidirectional communication is accomplished within these devices by offsetting the low-level output voltage on side 1 to a value greater than the high-level input voltage on side 1, thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO1540-Q1 ISO1541-Q1	SOIC (8)	4.90 mm × 3.91 mm



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2020) to Revision C (November 2021)	Page
• Changed scaling on mutiple images	23

Changes from Revision A (March 2019) to Revision B (October 2020)	Page
• Added Section 1 bullet for Functional Safety Information	1

Changes from Revision * (November 2016) to Revision A (March 2019)	Page
• Changed VDE Standard name From: DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 To: DIN VDE V 0884-11:2017-01 in Section 1	1
• Changed Section 1 bullet From: CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards To: CSA approval per IEC 60950-1 and IEC 62368-1 end equipment standards	1
• Deleted Section 1 bullet: UL 1577 Certification Complete; All Other Certifications Planned	1
• Updated certifications approval status, numbers, standard names, and details according to the latest agency certificates in Section 6.7 table	8
• Changed both bypass capacitors From: 10 µF To: 0.1 µF in . Even though larger capacitors can be used, 0.1 µF is the minimum recommended bypass capacitor size	23
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5 Pin Configuration and Functions

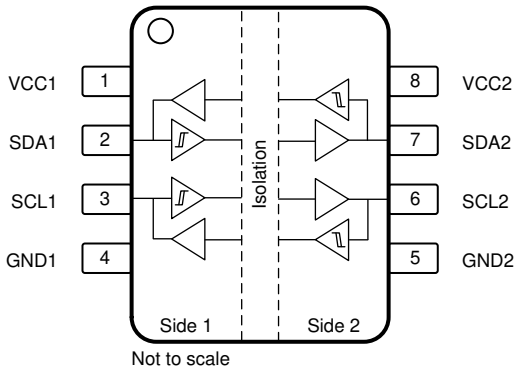


Figure 5-1. ISO1540-Q1 D Package 8-Pin SOIC Top View

Table 5-1. Pin Functions—ISO1540-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	—	Ground, side 1
GND2	5	—	Ground, side 2
SCL1	3	I/O	Serial clock input / output, side 1
SCL2	6	I/O	Serial clock input / output, side 2
SDA1	2	I/O	Serial data input / output, side 1
SDA2	7	I/O	Serial data input / output, side 2
VCC1	1	—	Supply voltage, side 1
VCC2	8	—	Supply voltage, side 2

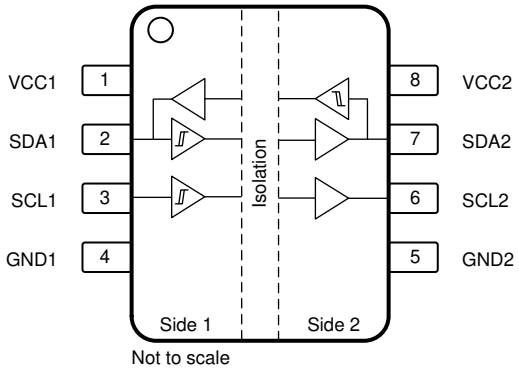


Figure 5-2. ISO1541-Q1 D Package 8-Pin SOIC Top View

Table 5-2. Pin Functions—ISO1541-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	—	Ground, side 1
GND2	5	—	Ground, side 2
SCL1	3	I	Serial clock input, side 1
SCL2	6	O	Serial clock output, side 2
SDA1	2	I/O	Serial data input / output, side 1
SDA2	7	I/O	Serial data input / output, side 2
VCC1	1	—	Supply voltage, side 1
VCC2	8	—	Supply voltage, side 2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Voltage	VCC1, VCC2	–0.5	6	V
		SDA1, SCL1	–0.5	VCC1 + 0.5(3)	
		SDA2, SCL2	–0.5	VCC2 + 0.5(3)	
I_O	Output current	SDA1, SCL1	–20	20	mA
		SDA2, SCL2	–100	100	
$T_{J(MAX)}$	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values here within are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins except bus pins	±4000	V
			Bus pins	±8000	
		Charged-device model (CDM), per AEC Q100-011		±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
VCC1, VCC2	Supply voltage	3	5.5	V
V_{SDA1}, V_{SCL1}	Input and output signal voltages, side 1	0	VCC1	V
V_{SDA2}, V_{SCL2}	Input and output signal voltages, side 2	0	VCC2	V
V_{IL1}	Low-level input voltage, side 1	0	0.5	V
V_{IH1}	High-level input voltage, side 1	0.7 × VCC1	VCC1	V
V_{IL2}	Low-level input voltage, side 2	0	0.3 × VCC2	V
V_{IH2}	High-level input voltage, side 2	0.7 × VCC2	VCC2	V
I_{OL1}	Output current, side 1	0.5	3.5	mA
I_{OL2}	Output current, side 2	0.5	35	mA
C1	Capacitive load, side 1		40	pF
C2	Capacitive load, side 2		400	pF
f_{MAX}	Operating frequency(1)		1	MHz
T_A	Ambient temperature	–40	125	°C
T_J	Junction temperature	–40	136	°C
T_{SD}	Thermal shutdown	139	171	°C

(1) This represents the maximum frequency with the maximum bus load (C) and the maximum current sink (I_O). If the system has less bus capacitance, then higher frequencies can be achieved.

6.4 Thermal Information

THERMAL METRIC[1]		ISO154x-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VCC1 = VCC2 = 5.5 V, T_J = 150 °C, C1 = 40 pF, C2 = 400 pF; Input a 1-MHz 50% duty cycle clock signal			85	mW
P_{D1}	Maximum power dissipation (side-1)				34	mW
P_{D2}	Maximum power dissipation (side-2)				51	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.014	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I–IV	
		Rated mains voltage ≤ 300 V_{RMS}	I–III	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 s (qualification) t = 1 s (100% production)	4242	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 680\ V_{PK}$, t_m = 10 s	<5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 906\ V_{PK}$, t_m = 10 s	<5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 1062\ V_{PK}$, t_m = 1 s	<5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	~1	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 2500 V_{RMS}, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC
Certified according to DIN VDE V 0884-11:2017-01 and DIN EN 61010-1 (VDE 0411-1):2011-07	Certified according to CSA/IEC 60950-1 and CSA/IEC 62368-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK}; Maximum Repetitive Peak Voltage, 566 V_{PK}	2.5-kV_{RMS} Insulation Rating; 400 V_{RMS} Basic Insulation working voltage per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2; 300 V_{RMS} Basic Insulation working voltage per CSA 62368-1-14 and IEC 62368-1:2014,	Single protection, 2500 V_{RMS}	Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40047657	Master contract number: 220991	File number: E181974	Certificate number: CQC14001109540

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 114.6°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 6-1			198	mA
		$R_{\theta JA}$ = 114.6°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 6-1			303	
T_S	Safety temperature				150	°C

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Section 6.4* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics

over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SIDE 1 (ONLY)						
V_{ILT1}	Voltage input threshold low, SDA1 and SCL1		500	550	660	mV
V_{IHT1}	Voltage input threshold high, SDA1 and SCL1		540	610	700	mV
V_{HYST1}	Voltage input hysteresis	$V_{IHT1} - V_{ILT1}$	40	60		mV
V_{OL1}	Low-level output voltage, SDA1 and SCL1(1)	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA	650		800	mV
ΔV_{OIT1}	Low-level output voltage to high-level input voltage threshold difference, SDA1 and SCL1(1) (2)	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA	50			mV
SIDE 2 (ONLY)						
V_{ILT2}	Voltage input threshold low, SDA2 and SCL2		0.3 × VCC2		0.4 × VCC2	V
V_{IHT2}	Voltage input threshold high, SDA2 and SCL2		0.4 × VCC2		0.5 × VCC2	V
V_{HYST2}	Voltage input hysteresis	$V_{IHT2} - V_{ILT2}$	0.05 × VCC2			V
V_{OL2}	Low-level output voltage, SDA2 and SCL2	0.5 mA ≤ (I_{SDA2} and I_{SCL2}) ≤ 35 mA			0.4	V
BOTH SIDES						
$\lvert I_I \rvert$	Input leakage currents, SDA1, SCL1, SDA2, and SCL2	V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2		0.01	10	µA
C_I	Input capacitance to local ground, SDA1, SCL1, SDA2, and SCL2	V_I = 0.4 × sin(2E6πt) + 2.5 V		7		pF
CMTI	Common-mode transient immunity	See Figure 7-3	25	50		kV/µs
V_{CCUV}	VCC undervoltage lockout threshold(3)		2.1	2.5	2.8	V

(1) This parameter does not apply to the ISO1541-Q1 SCL1 line as it is unidirectional.
(2) $\Delta V_{OIT1} = V_{OL1} - V_{IHT1}$. This represents the minimum difference between a Low-Level Output Voltage and a High-Level Input Voltage Threshold to prevent a permanent latch condition that would otherwise exist with bidirectional communication.
(3) Any VCC voltages, on either side, less than the minimum will ensure device lockout. Both VCC voltages greater than the maximum will prevent device lockout.

6.10 Supply Current Characteristics

over recommended operating conditions, unless otherwise noted. For more information, see Figure 7-1.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
3 V ≤ VCC1, VCC2 ≤ 3.6 V							
I_{CC1}	Supply current, side 1	ISO1540-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1, R2 = Open; C1, C2 = Open		2.4	3.6	mA
			V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		2.5	3.8	
		ISO1541-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1, R2 = Open; C1, C2 = Open		2.1	3.3	
			V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		2.3	3.6	
I_{CC2}	Supply current, side 2	ISO1540-Q1 and ISO1541-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1, R2 = Open; C1, C2 = Open		1.7	2.7	mA
			V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		1.9	3.1	
4.5 V ≤ VCC1, VCC2 ≤ 5.5 V							
I_{CC1}	Supply current, side 1	ISO1540-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1,R2 = Open; C1,C2 = Open		3.1	4.7	mA
			V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		3.1	4.7	
		ISO1541-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1, R2 = Open; C1, C2 = Open		2.8	4.4	
			V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		2.9	4.5	
I_{CC2}	Supply current, side 2	ISO1540-Q1 and ISO1541-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1, R2 = Open; C1, C2 = Open		2.3	3.7	mA
			V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		2.5	4	

6.11 Timing Requirements

			MIN	NOM	MAX	UNIT
t_{SP}	Input noise filter		5	12		ns
t_{UVLO}	Time to recover from UVLO	2.7 V to 0.9 V; See Figure 7-4	30	50	110	µs

6.12 Switching Characteristics

over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
3 V ≤ VCC1, VCC2 ≤ 3.6 V							
t_{f1}	Output Signal Fall Time (SDA1, SCL1)	See Figure 7-1 R1 = 953 Ω, C1 = 40 pF	0.7 × VCC1 to 0.3 × VCC1	8	17	29	ns
			0.9 × VCC1 to 900 mV	16	29	48	
t_{f2}	Output Signal Fall Time (SDA2, SCL2)	See Figure 7-1 R2 = 95.3 Ω, C2 = 400 pF	0.7 × VCC2 to 0.3 × VCC2	14	23	47	ns
			0.9 × VCC2 to 400 mV	35	50	100	
t_{pLH1-2}	Low-to-High Propagation Delay, Side 1 to Side 2	See Figure 7-1 R1 = 953 Ω, R2 = 95.3 Ω, C1, C2 = 10 pF	0.55 V to 0.7 × VCC2		33	65	ns
t_{PHL1-2}	High-to-Low Propagation Delay, Side 1 to Side 2		0.7 V to 0.4 V		90	181	ns
PWD_{1-2}	Pulse Width Distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$				55	123	ns
t_{PLH2-1} (1)	Low-to-High Propagation Delay, Side 2 to Side 1		0.4 × VCC2 to 0.7 × VCC1		47	68	ns
t_{PHL2-1} (1)	High-to-Low Propagation Delay, Side 2 to Side 1		0.4 × VCC2 to 0.9 V		67	109	ns
PWD_{2-1} (1)	Pulse Width Distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$				20	49	ns
t_{LOOP1} (1)	Round-trip propagation delay on Side 1	See Figure 7-2; R1 = 953 Ω, C1 = 40 pF R2 = 95.3 Ω, C2 = 400 pF	0.4 V to 0.3 × VCC1		100	165	ns
4.5 V ≤ VCC1, VCC2 ≤ 5.5 V							
t_{f1}	Output Signal Fall Time (SDA1, SCL1)	See Figure 7-1 R1 = 1430 Ω, C1 = 40 pF	0.7 × VCC1 to 0.3 × VCC1	6	11	20	ns
			0.9 × VCC1 to 900 mV	13	21	39	
t_{f2}	Output Signal Fall Time (SDA2, SCL2)	See Figure 7-1 R2 = 143 Ω, C2 = 400 pF	0.7 × VCC2 to 0.3 × VCC2	10	18	35	ns
			0.9 × VCC2 to 400 mV	28	41	76	
t_{pLH1-2}	Low-to-High Propagation Delay, Side 1 to Side 2	See Figure 7-1 R1 = 1430 Ω, R2 = 143 Ω, C1,2 = 10 pF	0.55 V to 0.7 × VCC2		31	62	ns
t_{PHL1-2}	High-to-Low Propagation Delay, Side 1 to Side 2		0.7 V to 0.4 V		70	139	ns
PWD_{1-2}	Pulse Width Distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$				38	80	ns
t_{PLH2-1} (1)	Low-to-high propagation delay, side 2 to side 1		0.4 × VCC2 to 0.7 × VCC1		55	80	ns
t_{PHL2-1} (1)	High-to-low propagation delay, Side 2 to side 1		0.4 × VCC2 to 0.9 V		47	85	ns
PWD_{2-1} (1)	Pulse Width Distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$				8	21	ns
t_{LOOP1} (1)	Round-trip propagation delay on side 1	See Figure 7-2; R1 = 1430 Ω, C1 = 40 pF R2 = 143 Ω, C2 = 400 pF	0.4 V to 0.3 × VCC1		110	180	ns

(1) This parameter does not apply to the ISO1541-Q1 SCL1 line as it is unidirectional.

6.13 Insulation Characteristics Curves

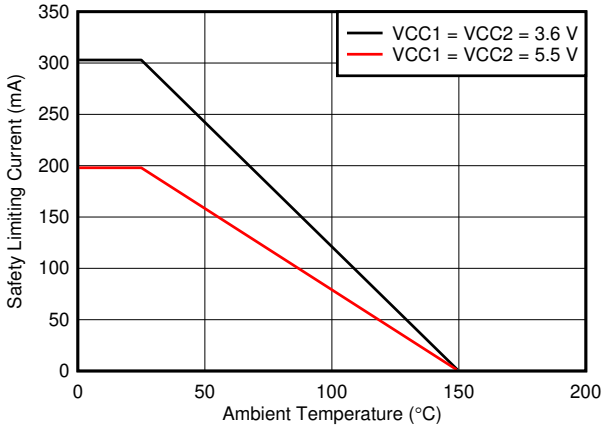


Figure 6-1. Thermal Derating Curve for Limiting Current per VDE

6.14 Typical Characteristics

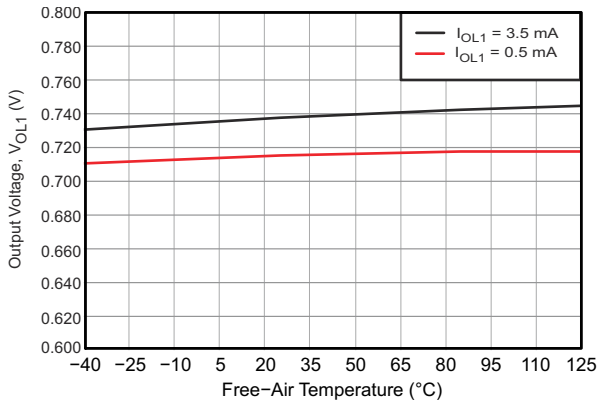
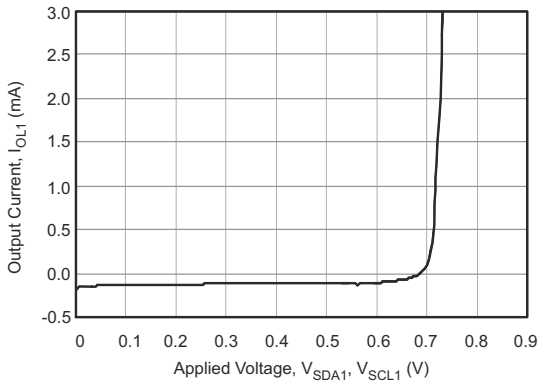
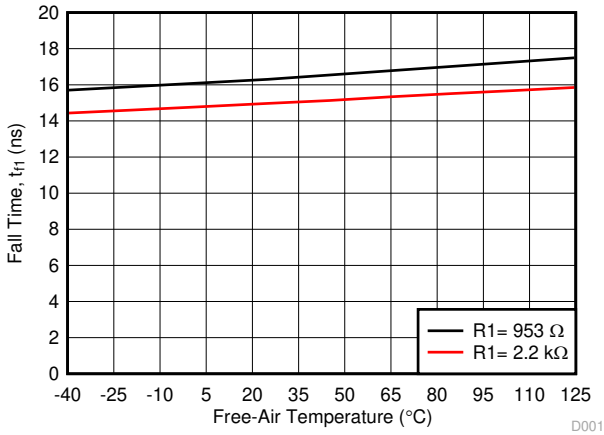


Figure 6-2. Side 1: Output Low Voltage vs Free-Air Temperature



T_A = 25°C

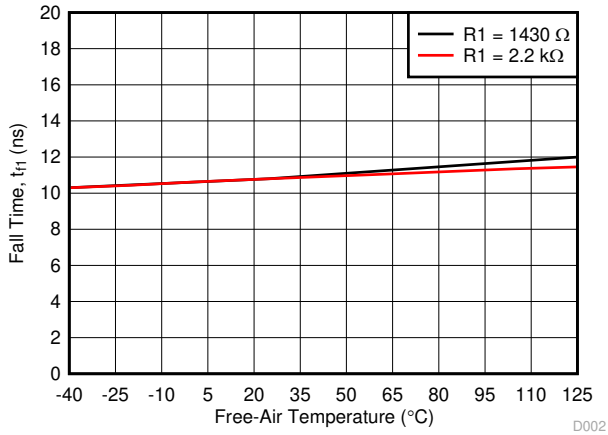
Figure 6-3. Side 1: Output Low Current vs S_{DA1} or S_{CL1} Applied Voltage



VCC1 = 3.3 V C1 = 40 pF

Fall time measured from 70% to 30% VCC1

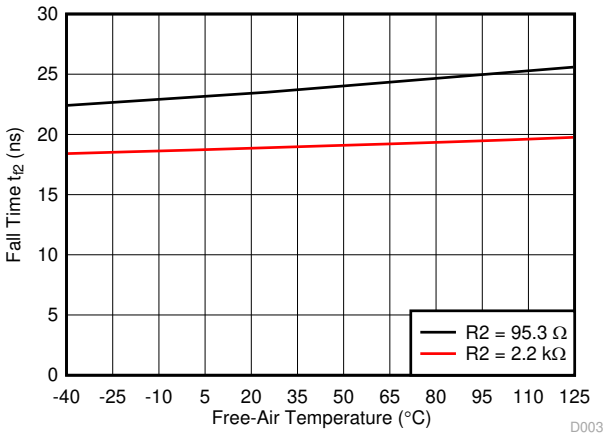
Figure 6-4. Side 1: Output Fall Time vs Free-Air Temperature



VCC1 = 5 V C1 = 40 pF

Fall time measured from 70% to 30% VCC1

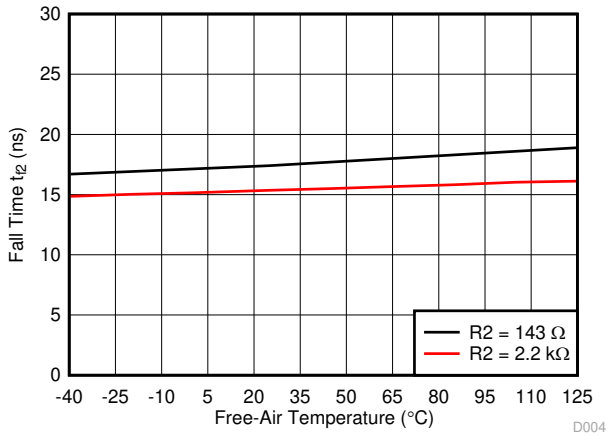
Figure 6-5. Side 1: Output Fall Time vs Free-air Temperature



VCC2 = 3.3 V C2 = 400 pF

Fall time measured from 70% to 30% VCC2

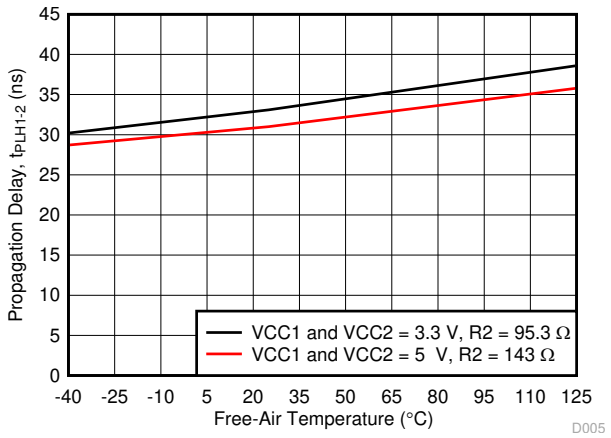
Figure 6-6. Side 2: Output Fall Time vs Free-Air Temperature



VCC2 = 5 V C2 = 400 pF

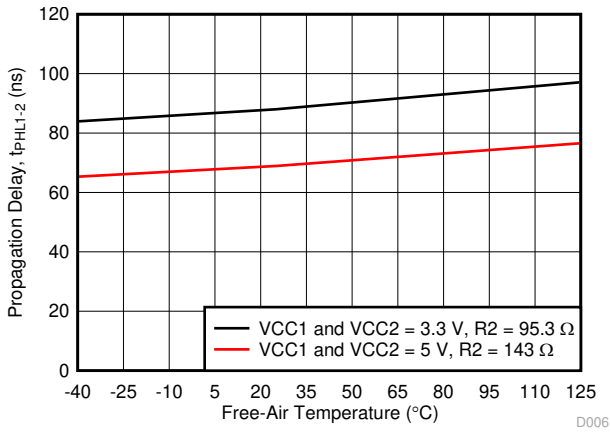
Fall time measured from 70% to 30% VCC2

Figure 6-7. Side 2: Output Fall Time vs Free-Air Temperature



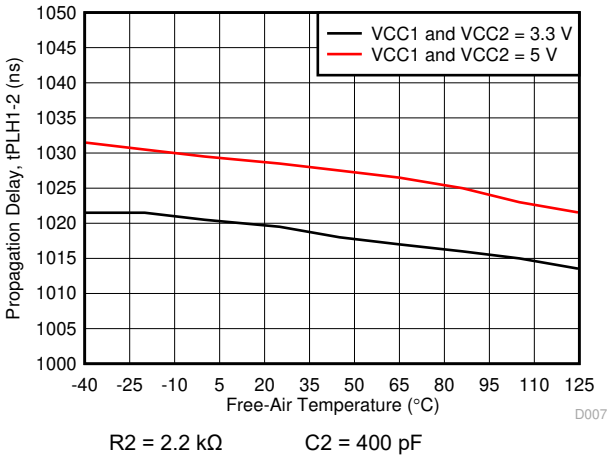
C2 = 10 pF

Figure 6-8. t_{PLH1-2} Propagation Delay vs Free-Air Temperature



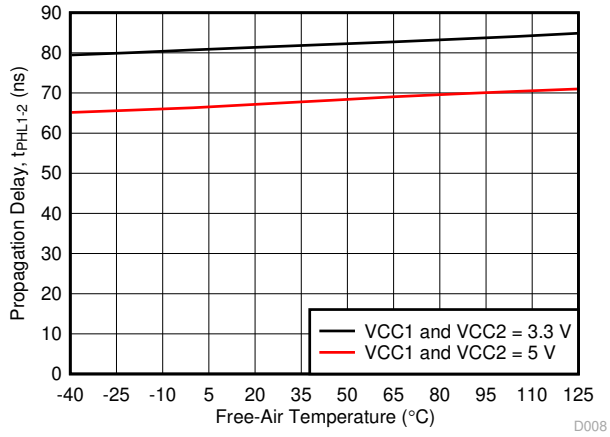
C2 = 10 pF

Figure 6-9. t_{PHL1-2} Propagation Delay vs Free-Air Temperature



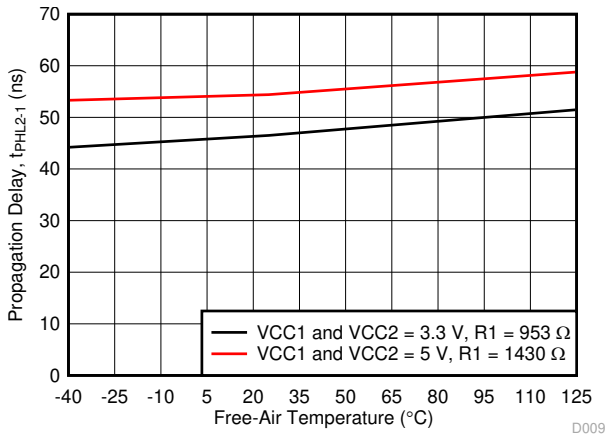
R2 = 2.2 kΩ C2 = 400 pF

Figure 6-10. t_{PLH1-2} Propagation Delay vs Free-Air Temperature



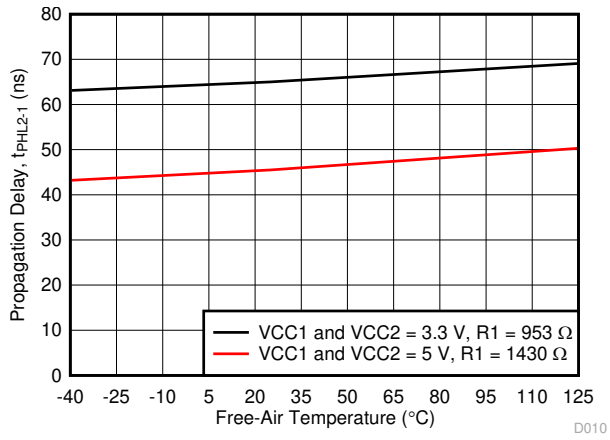
R2 = 2.2 kΩ C2 = 400 pF

Figure 6-11. t_{PHL1-2} Propagation Delay vs Free-Air Temperature



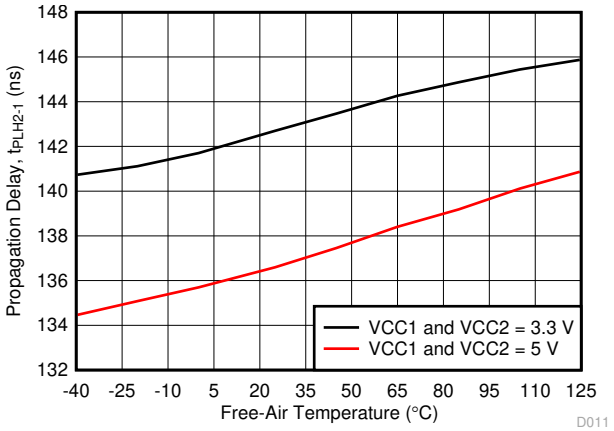
C1 = 10 pF

Figure 6-12. t_{PLH2-1} Propagation Delay vs Free-Air Temperature



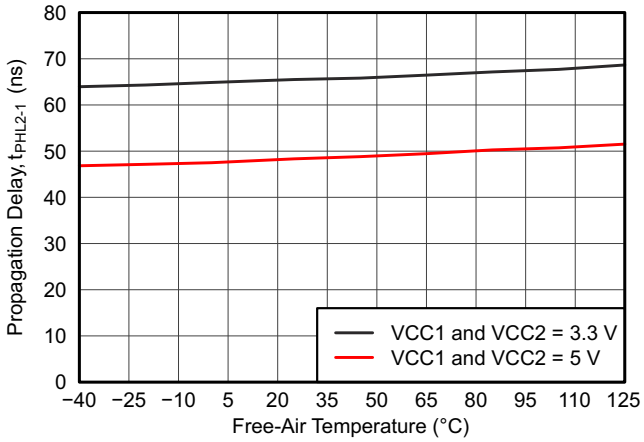
C1 = 10 pF

Figure 6-13. t_{PHL2-1} Propagation Delay vs Free-Air Temperature



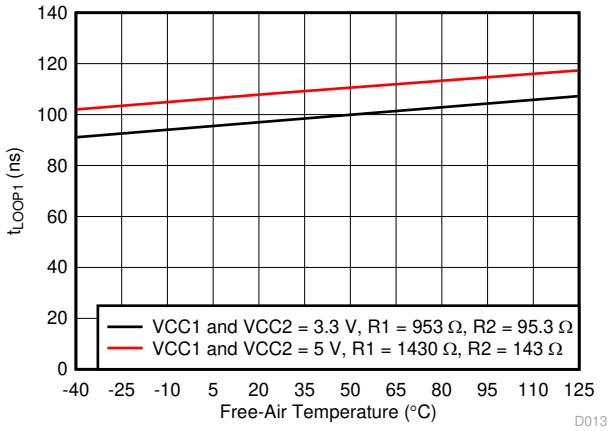
R1 = 2.2 kΩ C1 = 40 pF

Figure 6-14. t_{PLH2-1} Propagation Delay vs Free-Air Temperature



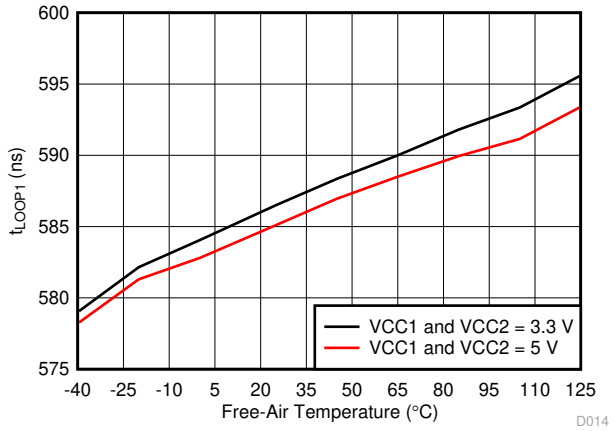
R1 = 2.2 kΩ C1 = 40 pF

Figure 6-15. t_{PHL2-1} Propagation Delay vs Free-Air Temperature



C1 = 40 pF C2 = 400 pF

Figure 6-16. t_{LOOP1} vs Free-Air Temperature



C1 = 40 pF C2 = 400 pF
R1 = 2.2 kΩ R2 = 2.2 kΩ

Figure 6-17. t_{LOOP1} vs Free-Air Temperature

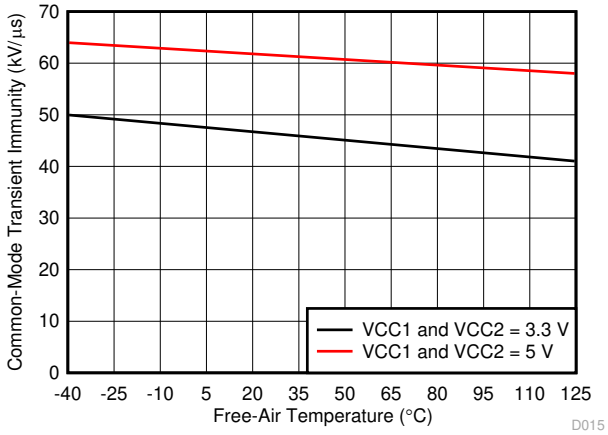


Figure 6-18. CMTI vs Free-Air Temperature

Parameter Measurement Information

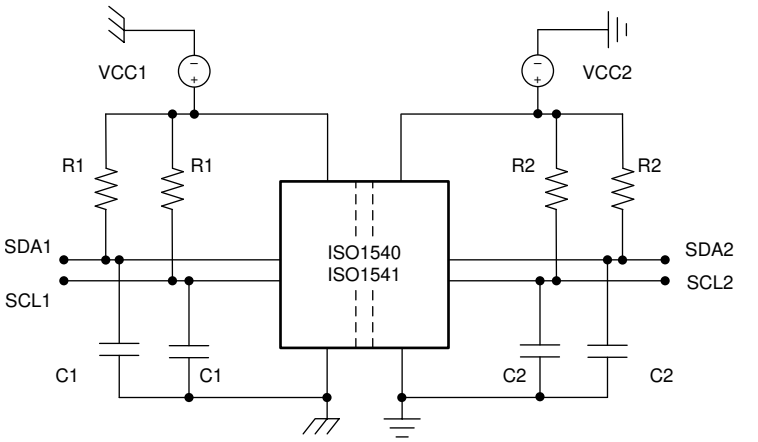


Figure 7-1. Test Diagram

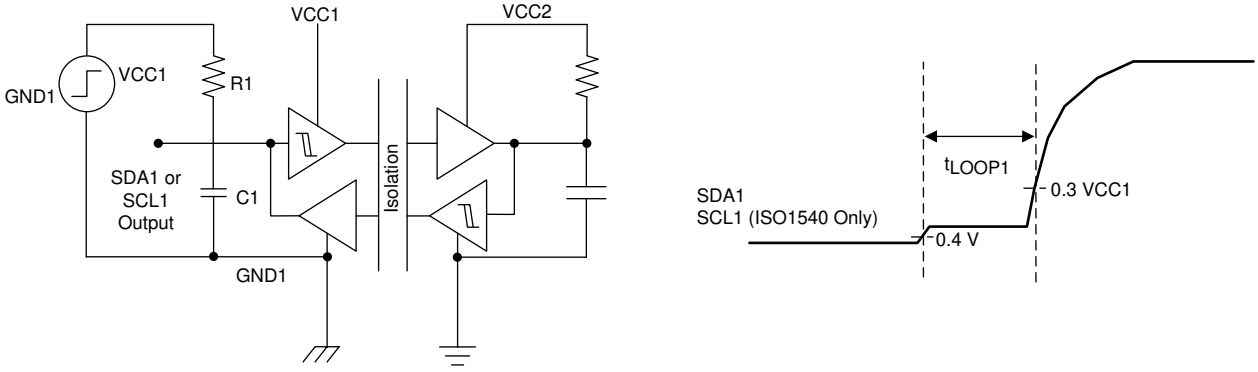


Figure 7-2. t_{Loop1} Setup and Timing Diagram

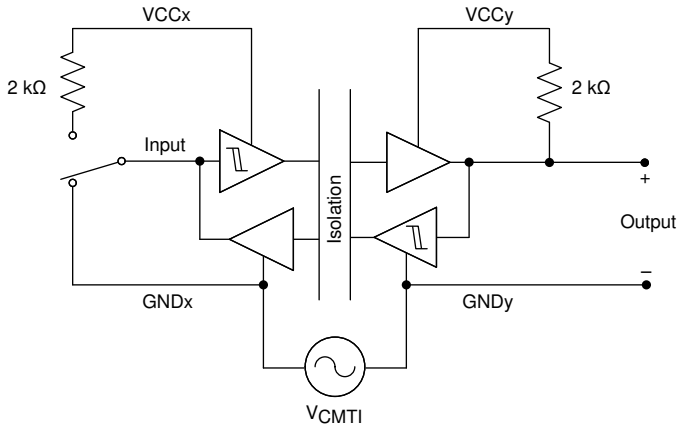
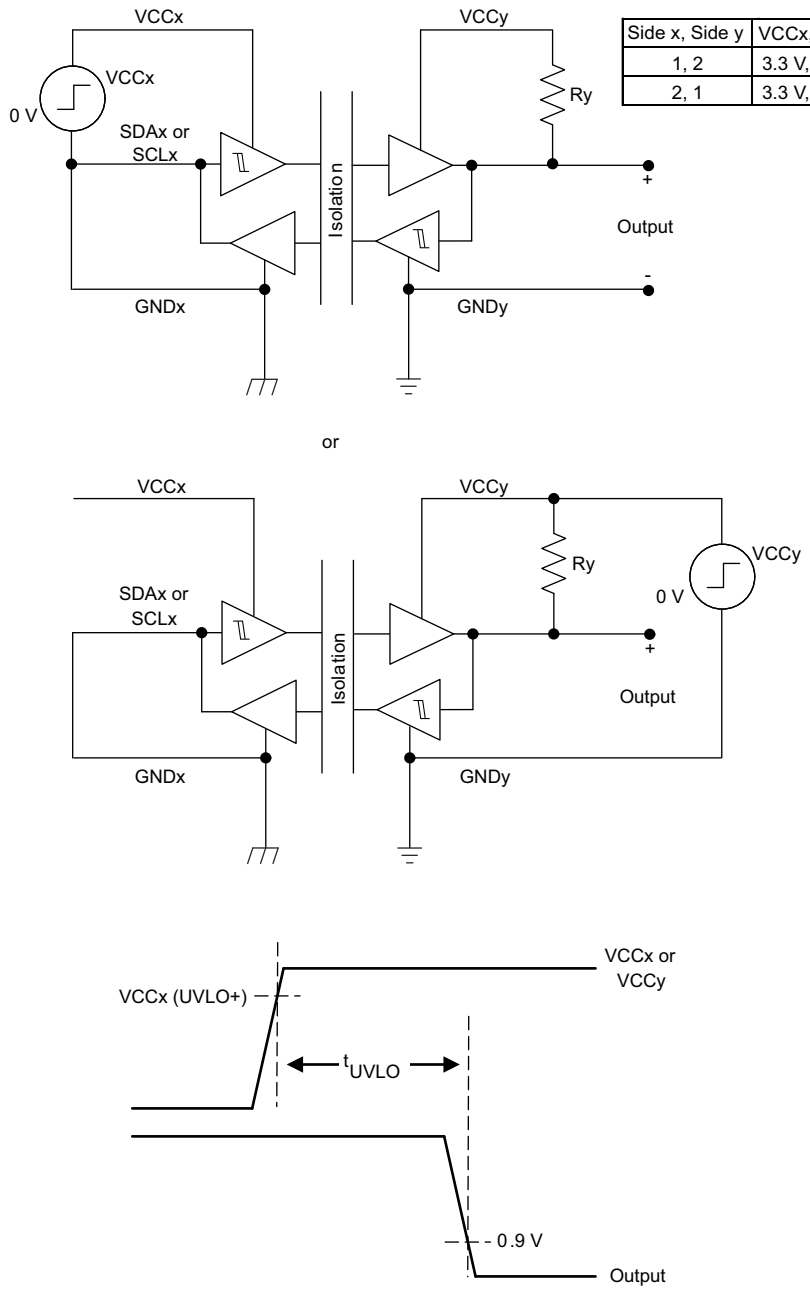


Figure 7-3. Common-Mode Transient Immunity Test Circuit



Side x, Side y	VCCx,VCCy	Ry
1, 2	3.3 V, 3.3 V	95.3 Ω
2, 1	3.3 V, 3.3 V	953 Ω

Figure 7-4. t_{UVLO} Test Circuit and Timing Diagrams

7 Detailed Description

7.1 Overview

The I^2C bus is used in a wide range of applications because it is simple to use. The bus consists of a two-wire communication bus that supports bidirectional data transfer between a master device and several slave devices. The master, or processor, controls the bus, specifically the serial clock (SCL) line. Data is transferred between the master and slave through a serial data (SDA) line. This data can be transferred in four speeds: standard mode (0 to 100 kbps), fast mode (0 to 400 kbps), fast-mode plus (0 to 1 Mbps), and high-speed mode (0 to 3.4 Mbps). The most common speeds are the standard and fast modes.

The I^2C bus operates in bidirectional, half-duplex mode, while standard digital isolators are unidirectional devices. To make efficient use of one technology supporting the other, external circuitry is required that separates the bidirectional bus into two unidirectional signal paths without introducing significant propagation delay. These devices have their logic input and output buffers separated by TI's capacitive isolation technology using a silicon dioxide (SiO_2) barrier. When used in conjunction with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

7.2 Functional Block Diagrams

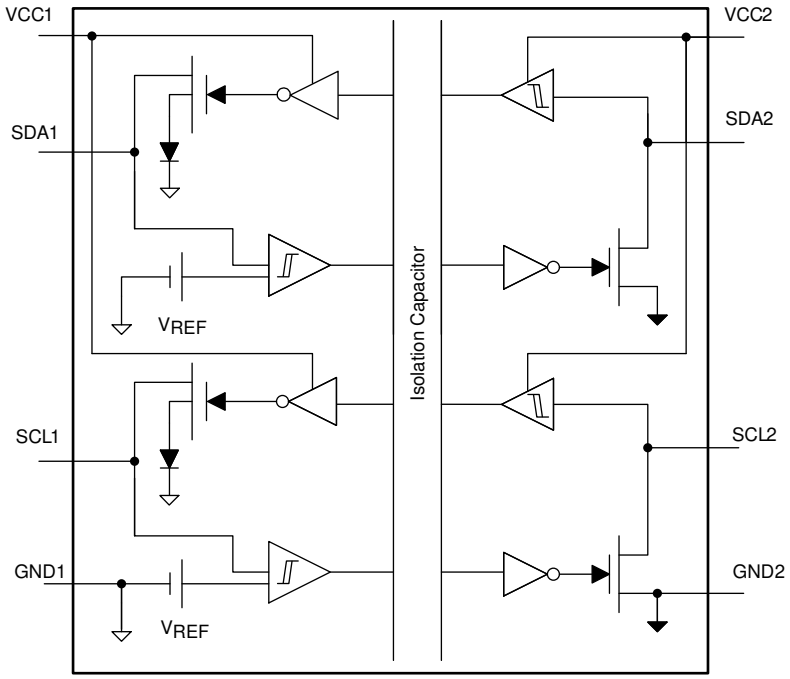


Figure 7-1. ISO1540-Q1 Block Diagram

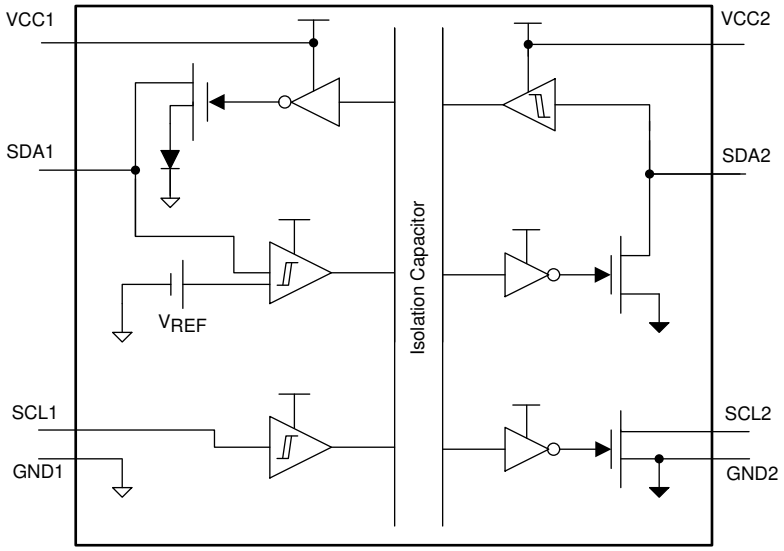


Figure 7-2. ISO1541-Q1 Block Diagram

7.3 Feature Description

The device enables a complete isolated I^2C interface to be implemented within a small form factor having the features listed in Table 7-1.

Table 7-1. Features List

PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION(1)	MAXIMUM FREQUENCY
ISO1540-Q1	Bidirectional (SCL) Bidirectional (SDA)	2500 V_{RMS} 4242 V_{PK}	1 MHz
ISO1541-Q1	Unidirectional (SCL) Bidirectional (SDA)		

(1) See *Section 6.7* for detailed Isolation specifications.

7.4 Isolator Functional Principle

To isolate a bidirectional signal path (SDA or SCL), the ISO1540-Q1 internally splits a bidirectional line into two unidirectional signal lines, each of which is isolated through a single-channel digital isolator. Each channel output is made open-drain to comply with the open-drain technology of I^2C. Side 1 of the ISO1540-Q1 connects to a low-capacitance I^2C node, while side 2 is designed for connecting to a fully loaded I^2C bus with up to 400 pF of capacitance.

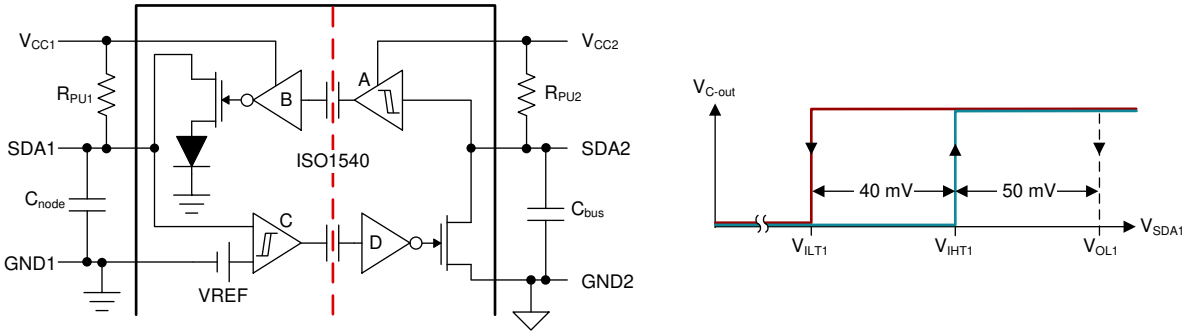


Figure 7-3. SDA Channel Design and Voltage Levels at SDA1

At first sight, the arrangement of the internal buffers suggests a closed signal loop that is prone to latch-up. However, this loop is broken by implementing an output buffer (B) whose output low-level is raised by a diode drop to approximately 0.75 V, and the input buffer (C) that consists of a comparator with defined hysteresis.

The comparator's upper and lower input thresholds then distinguish between the proper low-potential of 0.4 V (maximum) driven directly by SDA1 and the buffered output low-level of B.

Figure 7-4 demonstrate the switching behavior of the I²C isolator, ISO1540-Q1, between a master node at SDA1 and a heavy loaded bus at SDA2.

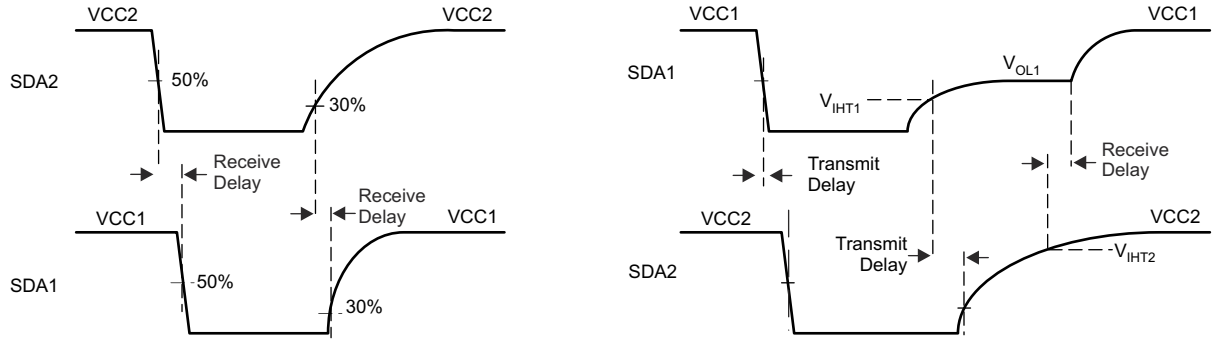


Figure 7-4. SDA Channel Timing in Receive and Transmit Directions

7.4.1 Receive Direction (Left Diagram of)

When the I²C bus drives SDA2 low, SDA1 follows after a certain delay in the receive path. The output low is the buffered output of V_{OL1} = 0.75 V, which is sufficiently low to be detected by Schmitt-trigger inputs with a minimum input-low voltage of V_{IL} = 0.9 V at 3 V supply levels.

When SDA2 is released, its voltage potential increases towards VCC2 following the time-constant formed by R_{PU2} and C_{bus}. After the receive delay, SDA1 is released and also rises towards VCC1, following the time-constant R_{PU1} × C_{node}. Because of the significant lower time-constant, SDA1 may reach VCC1 before SDA2 reaches VCC2 potential.

7.4.2 Transmit Direction (Right Diagram of)

When a master drives SDA1 low, SDA2 follows after a certain delay in the transmit direction. When SDA2 turns low it also causes the output of buffer B to turn low but at a higher 0.75 V level. This level cannot be observed immediately as it is overwritten by the lower low-level of the master.

However, when the master releases SDA1, the voltage potential increases and first must pass the upper input threshold of the comparator, V_{IHT1}, to release SDA2. SDA1 then increases further until it reaches the buffered output level of V_{OL1} = 0.75 V, maintained by the receive path. When comparator C turns high, SDA2 is released after the delay in transmit direction. It takes another receive delay until B's output turns high and fully releases SDA1 to move toward VCC1 potential.

7.5 Device Functional Modes

Table 7-2 lists the ISO154x-Q1 functional modes.

Table 7-2. Function Table

POWER STATE	INPUT	OUTPUT
VCC1 or VCC2 < 2.1 V	X	Z
VCC1 and VCC2 > 2.8 V	L	L
VCC1 and VCC2 > 2.8 V	H	Z
VCC1 and VCC2 > 2.8 V	Z(1)	?

(1) Invalid input condition as an I²C system requires that a pullup resistor to VCC is connected.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 I²C Bus Overview

The inter-integrated circuit (I^2C) bus is a single-ended, multi-master, 2-wire bus for efficient inter-IC communication in half-duplex mode.

I^2C uses open-drain technology, requiring two lines, serial data (SDA) and serial clock (SCL), to be connected to VDD by resistors (see Figure 8-1). Pulling the line to ground is considered a logic zero while letting the line float is a logic one. This logic is used as a channel access method. Transitions of logic states must occur while the SCL pin is low. Transitions while the SCL pin is high indicate START and STOP conditions. Typical supply voltages are 3.3 V and 5 V, although systems with higher or lower voltages are allowed.

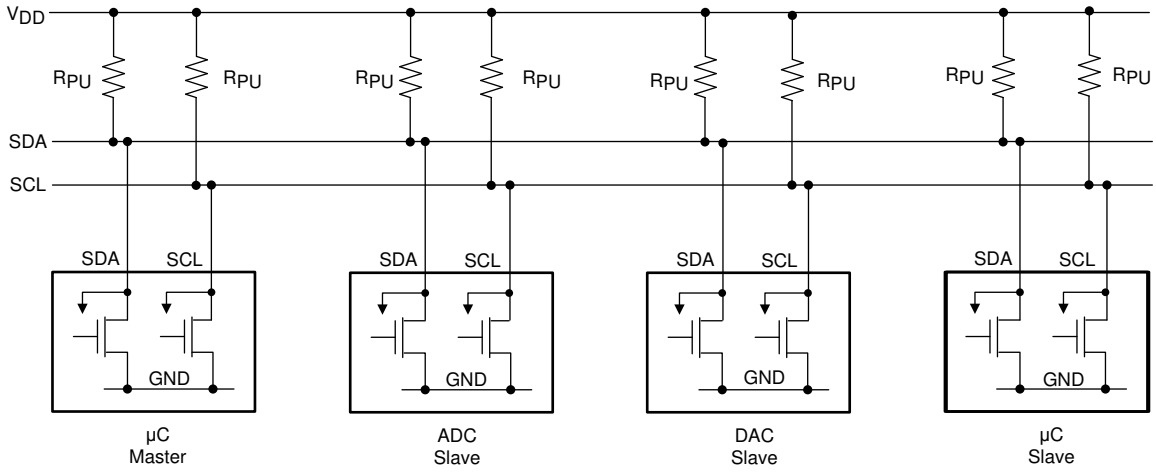


Figure 8-1. I^2C Bus

I^2C communication uses a 7-bit address space with 16 reserved addresses, so a theoretical maximum of 112 nodes can communicate on the same bus. In praxis, however, the number of nodes is limited by the specified, total bus capacitance of 400 pF, which restricts communication distances to a few meters.

The specified signaling rates for the ISO1540-Q1 and ISO1541-Q1 devices are 100 kbps (standard mode), 400 kbps (fast mode), 1 Mbps (fast mode plus).

The bus has two roles for nodes: master and slave. A master node issues the clock and slave addresses, and also initiates and ends data transactions. A slave node receives the clock and addresses and responds to requests from the master. Figure 8-2 shows a typical data transfer between master and slave.

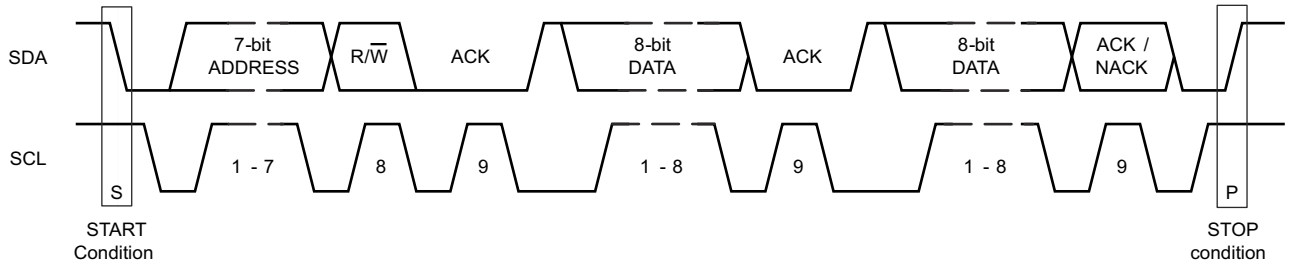


Figure 8-2. Timing Diagram of a Complete Data Transfer

The master initiates a transaction by creating a START condition, following by the 7-bit address of the slave it wishes to communicate with. This is followed by a single read and write (R/W) bit, representing whether the master wishes to write to 0, or to read from 1 the slave. The master then releases the SDA line to allow the slave to acknowledge the receipt of data.

The slave responds with an acknowledge bit (ACK) by pulling the SDA pin low during the entire high time of the 9th clock pulse on the SCL signal, after which the master continues in either transmit or receive mode (according to the R/W bit sent), while the slave continues in the complementary mode (receive or transmit, respectively).

The address and the 8-bit data bytes are sent most significant bit (MSB) first. The START bit is indicated by a high-to-low transition of SDA while SCL is high. The STOP condition is created by a low-to-high transition of SDA while SCL is high.

If the master writes to a slave, it repeatedly sends a byte with the slave sending an ACK bit. In this case, the master is in master-transmit mode and the slave is in slave-receive mode.

If the master reads from a slave, it repeatedly receives a byte from the slave, while acknowledging (ACK) the receipt of every byte but the last one (see Figure 8-3). In this situation, the master is in master-receive mode and the slave is in slave-transmit mode.

The master ends the transmission with a STOP bit, or may send another START bit to maintain bus control for further transfers.

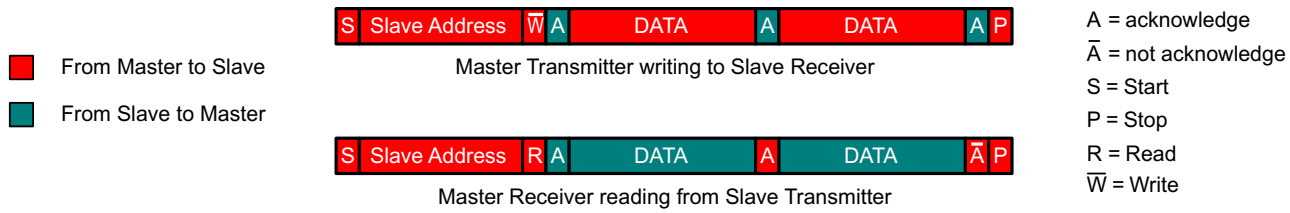


Figure 8-3. Transmit or Receive Mode Changes During a Data Transfer

When writing to a slave, a master mainly operates in transmit-mode and only changes to receive-mode when receiving acknowledgment from the slave.

When reading from a slave, the master starts in transmit-mode and then changes to receive-mode after sending a READ request (R/W bit = 1) to the slave. The slave continues in the complementary mode until the end of a transaction.

Note

The master ends a reading sequence by not acknowledging (NACK) the last byte received. This procedure resets the slave state machine and allows the master to send the STOP command.

8.2 Typical Application

Figure 8-4 shows isolated I^2C data acquisition system built with TI microcontroller, analog-to-digital converter, and I^2C isolator, ISO1541-Q1.

The entire circuit operates from a single 3.3-V supply. A low-power push-pull converter, SN6501-Q1, drives a center-tapped transformer with an output that is rectified and linearly regulated to provide a stable 5-V supply for the data converter.

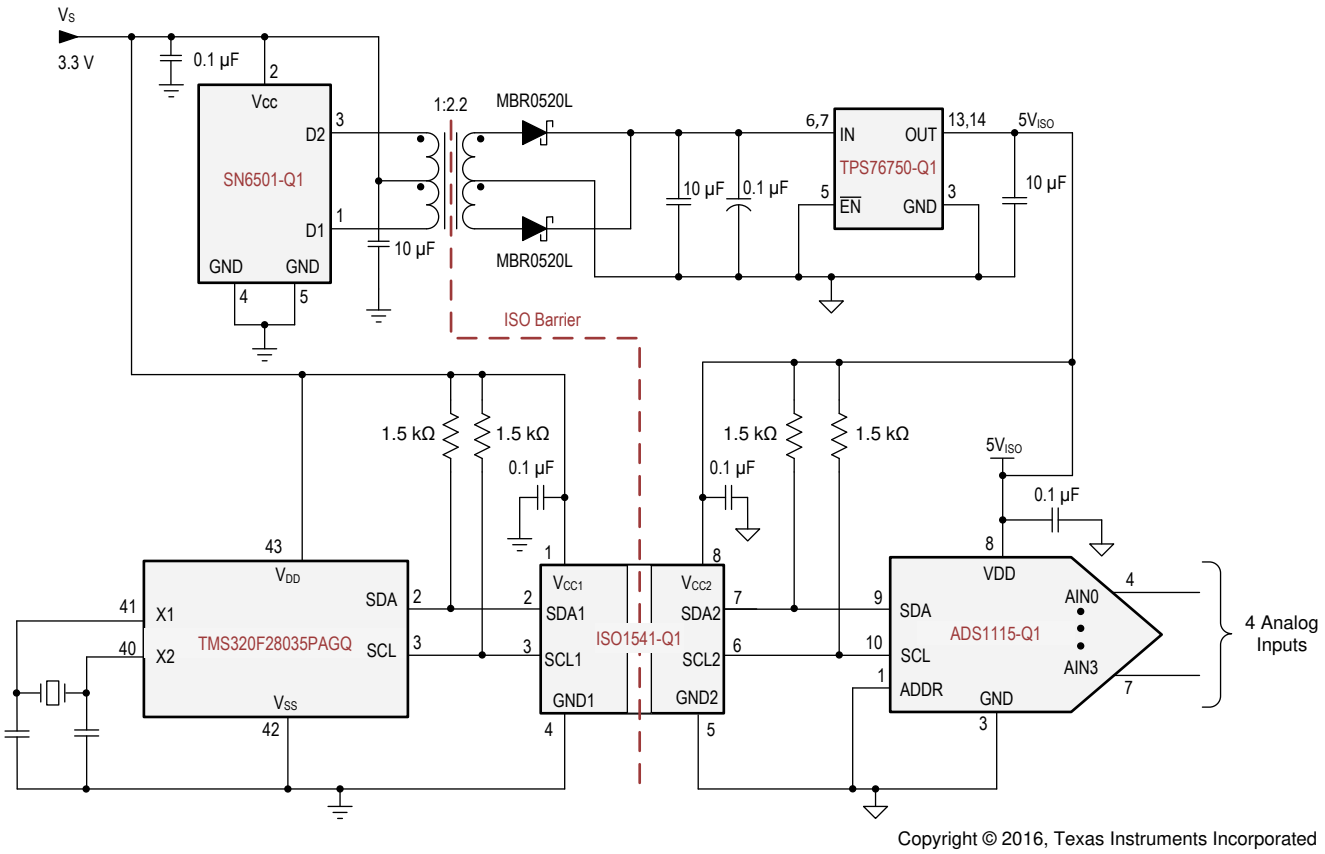


Figure 8-4. Isolated I²C Data Acquisition System

8.2.1 Design Requirements

The recommended power supply voltages (VCC1 and VCC2) must be from 3 V to 5.5 V. A recommended decoupling capacitor with a value of 0.1 µF is required between both the VCC1 and GND1 pins, and the VCC2 and GND2 pins to support of power supply voltages transient and to ensure reliable operation at all data rates.

8.2.2 Detailed Design Procedure

The power-supply capacitor with a value of 0.1-µF must be placed as close to the power supply pins as possible. The recommended placement of the capacitors must be 2-mm maximum from input and output power supply pins (VCC1 and VCC2).

The maximum load permissible on the input lines, SDA1 and SCL1, is ≤ 40 pF and on the output lines, SDA2 and SCL2, is ≤ 400 pF.

The minimum pullup resistors on the input lines, SDA1 and SCL1 to VCC1 must be selected in such a way that input current drawn is ≤ 3.5 mA. The minimum pullup resistors on the input lines, SDA2 and SCL2, to VCC2 must be selected in such a way that output current drawn is ≤ 35 mA. The maximum pullup resistors on the input

lines (SDA1 and SCL1) to VCC1 and on output lines (SDA1 and SCL1) to VCC2, depends on the load and rise time requirements on the respective lines.

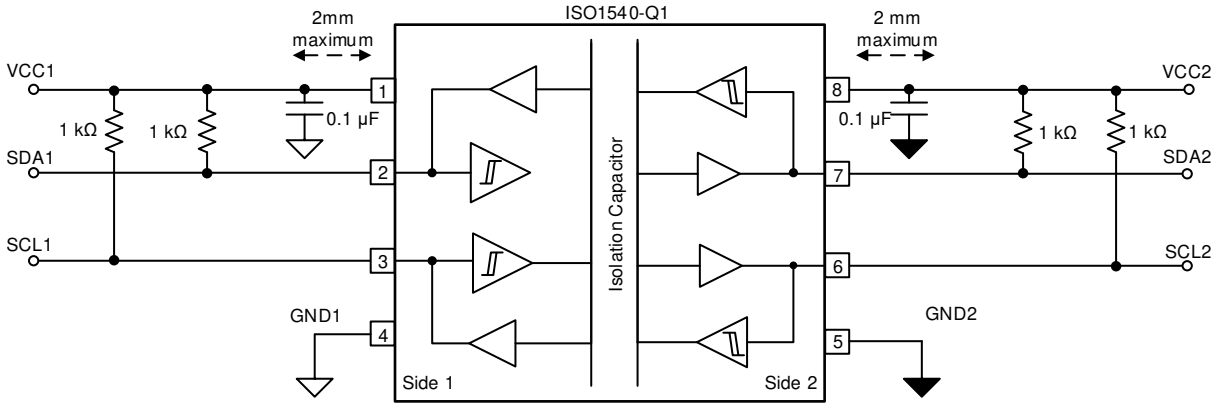


Figure 8-5. Typical ISO1540-Q1 Circuit Hookup

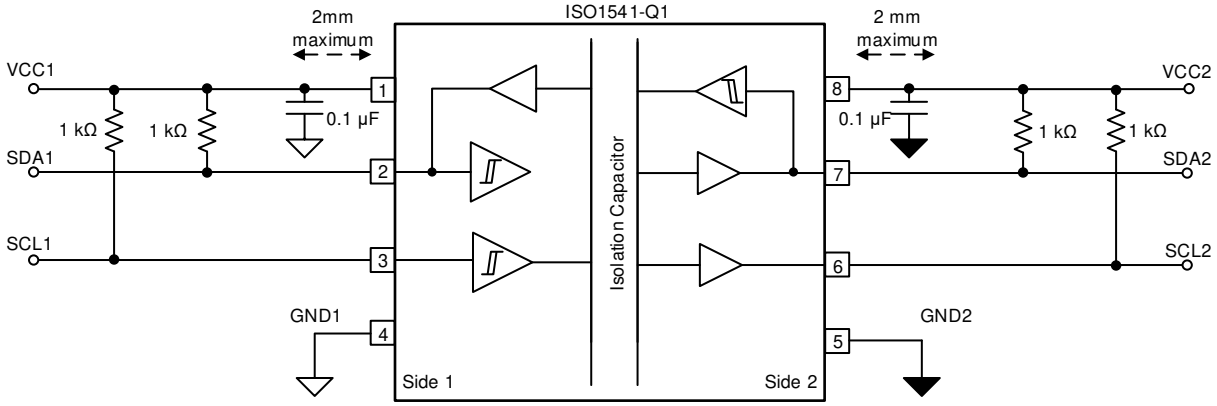


Figure 8-6. Typical ISO1541-Q1 Circuit Hookup

8.2.3 Application Curve

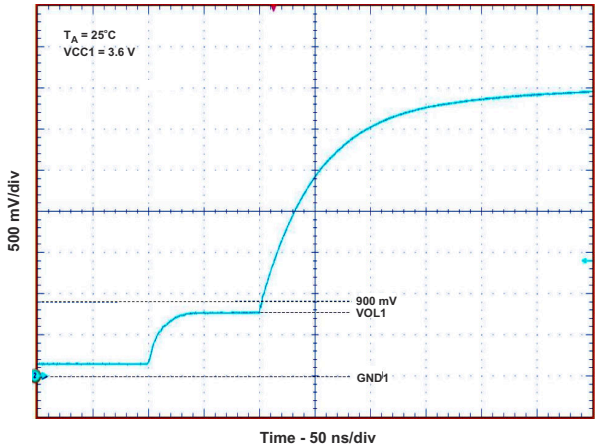


Figure 8-7. Side 1: Low-to-High Transition

9 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, TI recommends connecting a 0.1-µF bypass capacitor at the input and output supply pins (VCC1 and VCC2). The capacitors should be placed as close to the supply pins as possible. If only a single, primary-side power supply is available in an application, isolated power

can be generated for the secondary-side with the help of a transformer driver such as TI's SN6501-Q1 device. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies* (SLLSEF3).

10 Layout

10.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 10-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the *Digital Isolator Design Guide* (SLLA284)

10.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

10.2 Layout Example

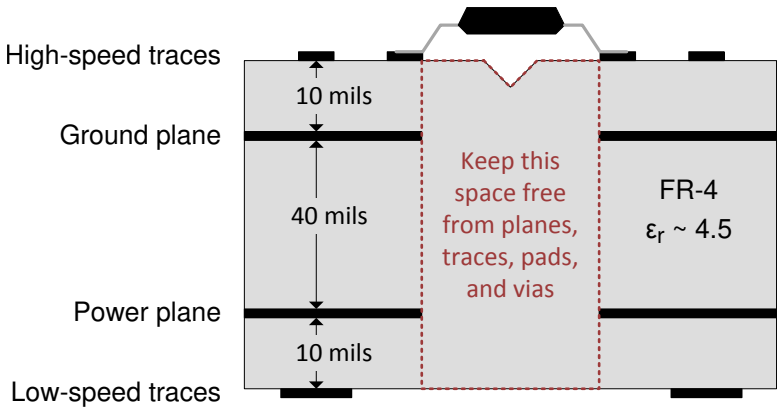


Figure 10-1. Recommended Layer Stack

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Digital Isolator Design Guide* (SLLA284)
- *TI Isolation Glossary* (SLLA353)
- *SN6501-Q1 Transformer Driver for Isolated Power Supplies.* (SLLSEF3)
- TPS767xx-Q1 *Fast-Transient-Response 1-A Low-Dropout Voltage Regulators* (SGLS009)
- *ADS1115-Q1 Low-Power, 16-Bit Analog-to-Digital Converter With Internal Reference* (SBAS563)
- *TMS320F2803x Piccolo™ Microcontrollers* (TMS320F2803x Piccolo™ Microcontrollers)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO1540-Q1	Click here	Click here	Click here	Click here	Click here
ISO1541-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

11.5 Trademarks

Piccolo™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1540QDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I1540Q	Samples
ISO1540QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I1540Q	Samples
ISO1541QDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I1541Q	Samples
ISO1541QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I1541Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO1540-Q1, ISO1541-Q1 :

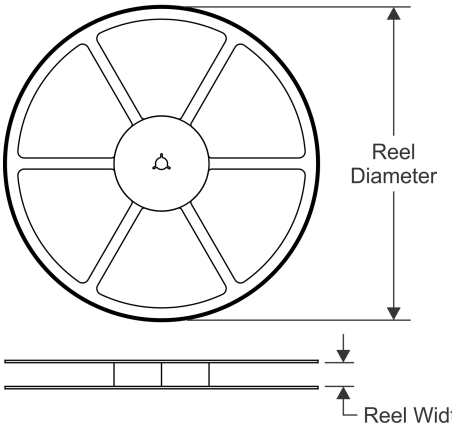
- Catalog : ISO1540, ISO1541

NOTE: Qualified Version Definitions:

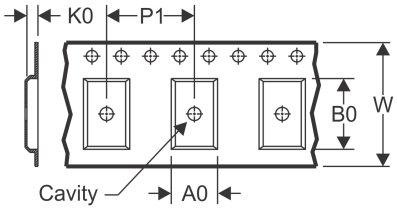
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

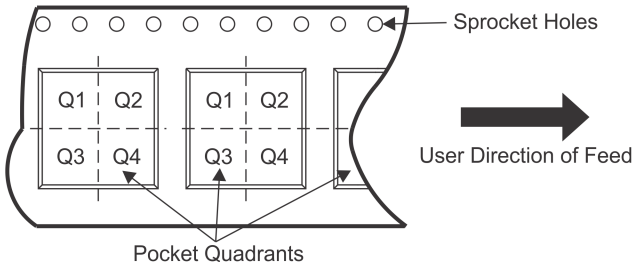


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

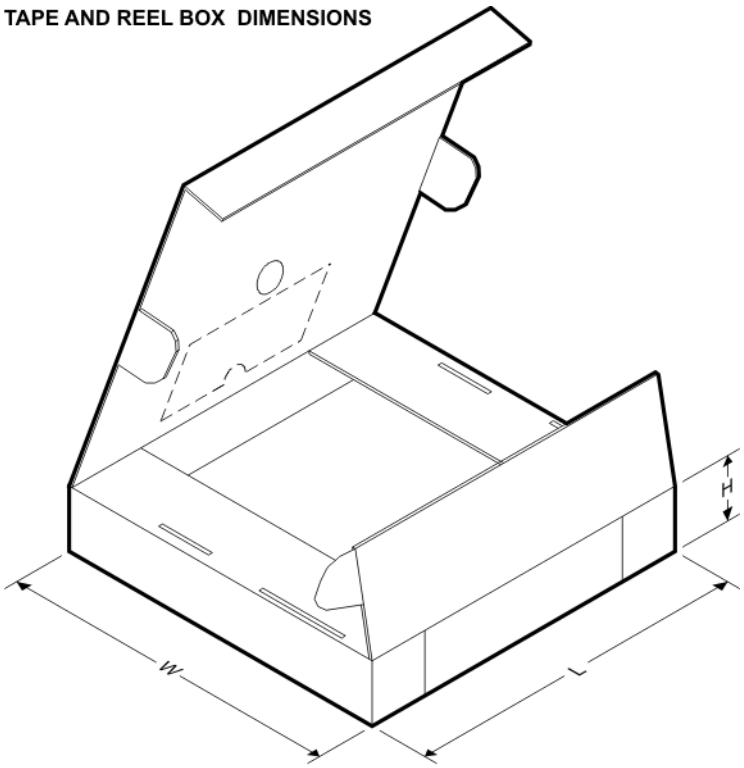
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1540QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO1541QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

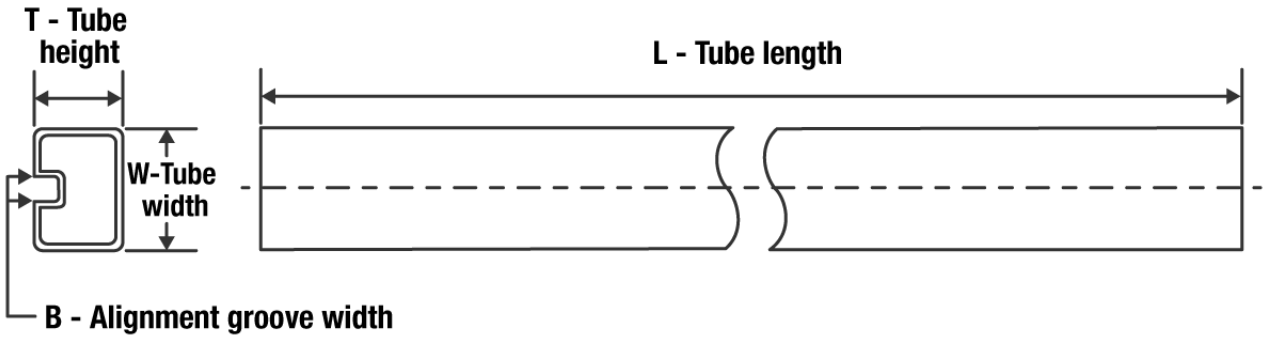
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

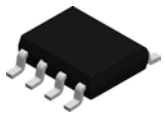
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1540QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO1541QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO1540QDQ1	D	SOIC	8	75	505.46	6.76	3810	4
ISO1541QDQ1	D	SOIC	8	75	505.46	6.76	3810	4

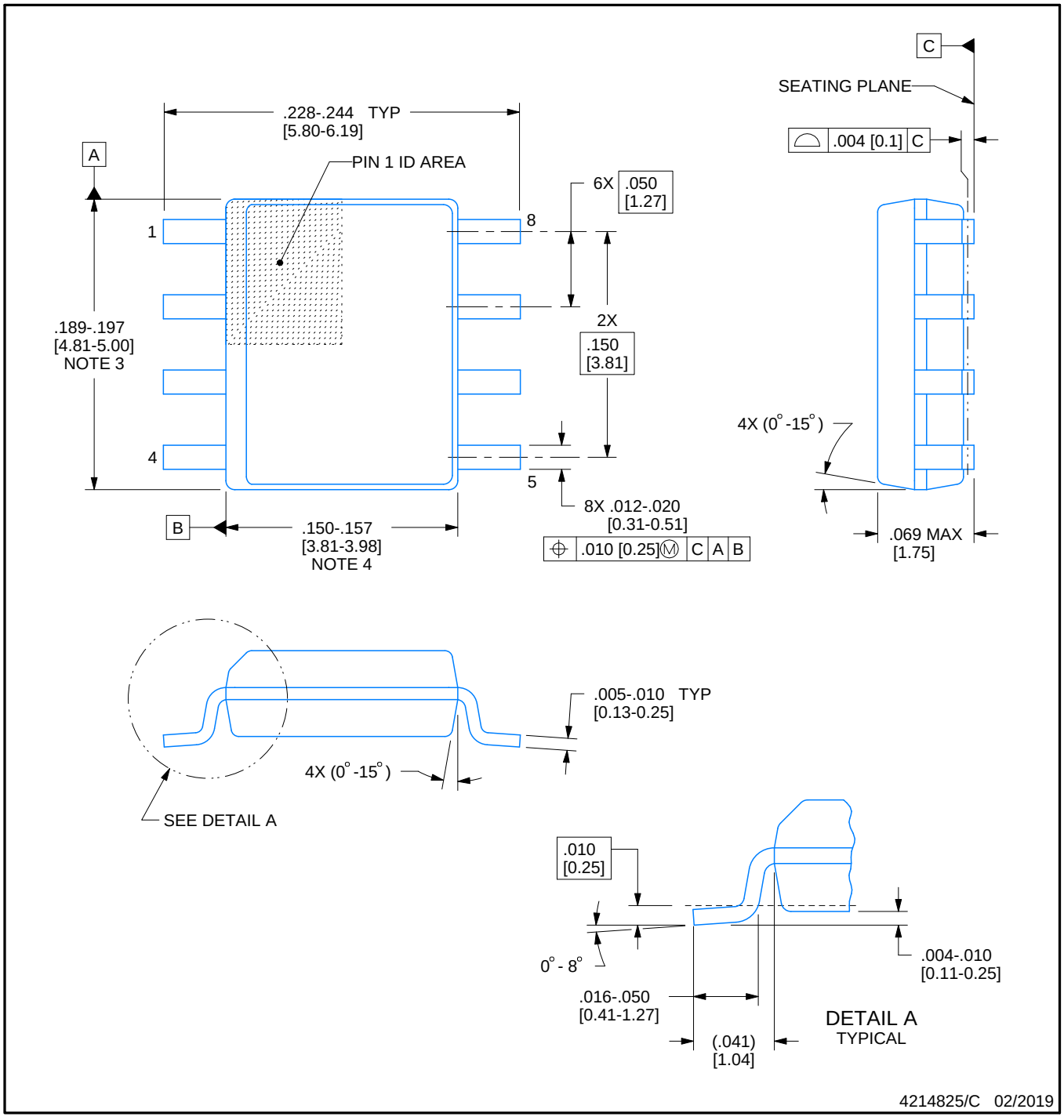


PACKAGE OUTLINE

D0008A

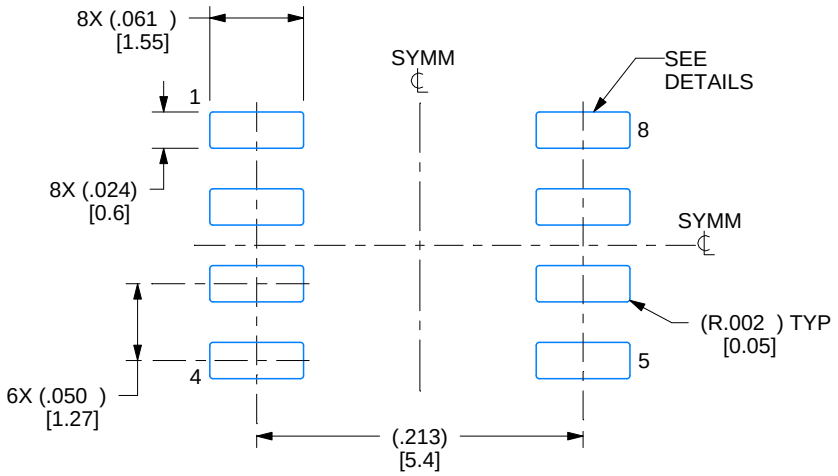
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

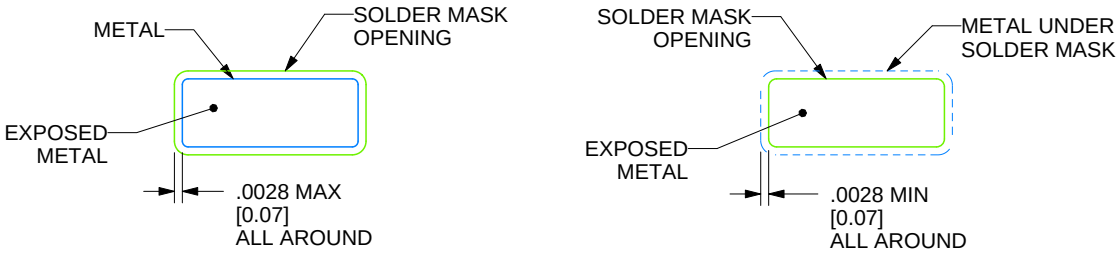


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

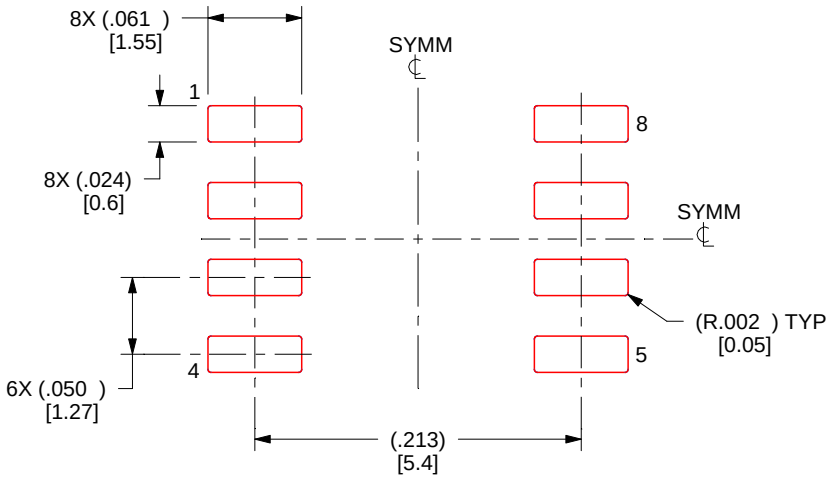
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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