WM8915

Ultra-Low Power Audio Hub CODEC

DESCRIPTION

The WM8915[1] is an ultra-low power mobile CODEC designed for music phones requiring high quality voice and music playback.

Four DAC channels and four ground-referenced Class W output drivers provide interfaces to a headset connector, earpiece or line output. Ground loop feedback is employed to reduce common mode noise on these outputs.

An advanced micro-power accessory interface provides plug-in / removal and hookswitch button press detection with support for up to seven buttons in parallel with the headset microphone. Load impedance sensing circuits provide support for a wide range of 3.5mm accessory types, including AV connectors.

The digital core is highly optimised to produce very high quality sidetones with low latency filters supporting both wideband and narrowband voice sample rates. Programmable filtering, equalisation and dynamic range control are also available in the record and playback paths. Flexible DAC mixing options are provided to all outputs.

The device integrates PDM interfaces for digital microphones and digital speaker amplifiers.

A MICBIAS with a dedicated LDO provides exceptionally high PSRR and low noise microphone amplifiers provide up to 30dB of gain in the ADC path.

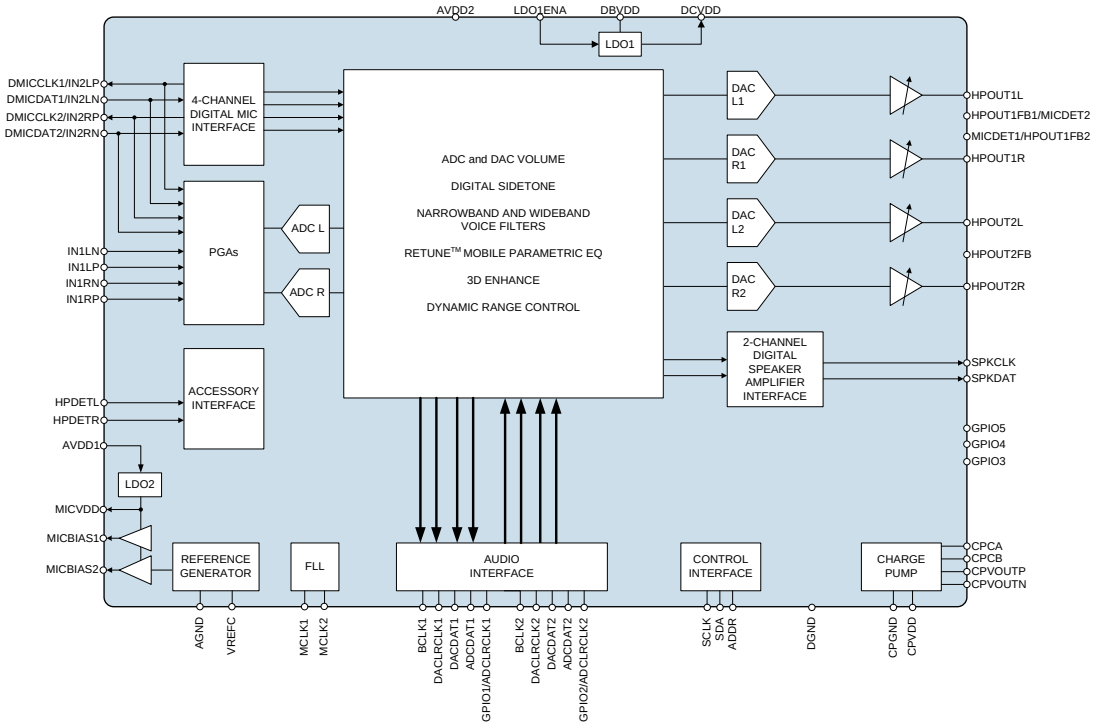
The WM8915 is supplied in a 3.24 x 3.56 x 0.7mm W-CSP package, ideal for portable systems.

FEATURES

- 4-channel DAC with 99dB SNR ('A' weighted)
- Four Class W ground-referenced headphone/line outputs
- 4-channel PDM digital inputs (digital microphone support)
- 2-channel PDM digital outputs (digital speaker amp support)
- Advanced 3.5mm accessory interface
  - Up to seven headset buttons supported
  - Accessory type detection and load impedance sense
  - Ultra-low power plug-in detect and button monitor
  - MICBIAS with dedicated LDO for ultra-high PSRR
- Programmable digital audio interface
  - All standard data formats supported
  - Multi-channel mixed rate TDM support
  - Standard sample rates up to 48kHz
  - Second interface to allow data pass-through
- 5mW total power consumption in playback mode
- Low power FLL
  - Provides all necessary internal clocks
  - 32kHz to 34MHz input frequency support
- 2-wire control interface
- 54-pin W-CSP package (3.24 x 3.56 x 0.58mm, 0.4mm pitch)

APPLICATIONS

- Music phones
- General purpose low power portable CODEC applications



[1] This product is protected by Patents US 7,622,984 and US 7,626,445.

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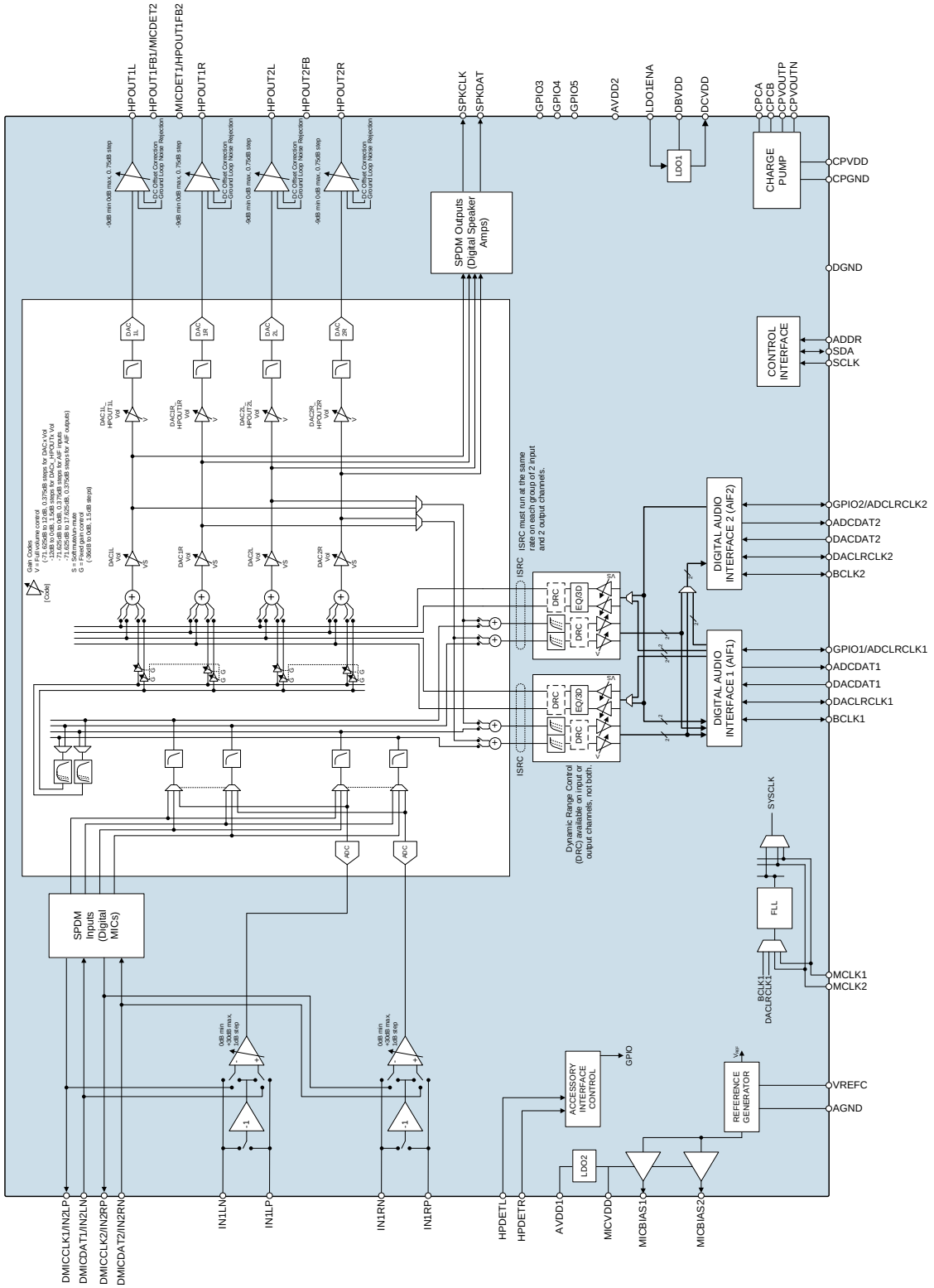
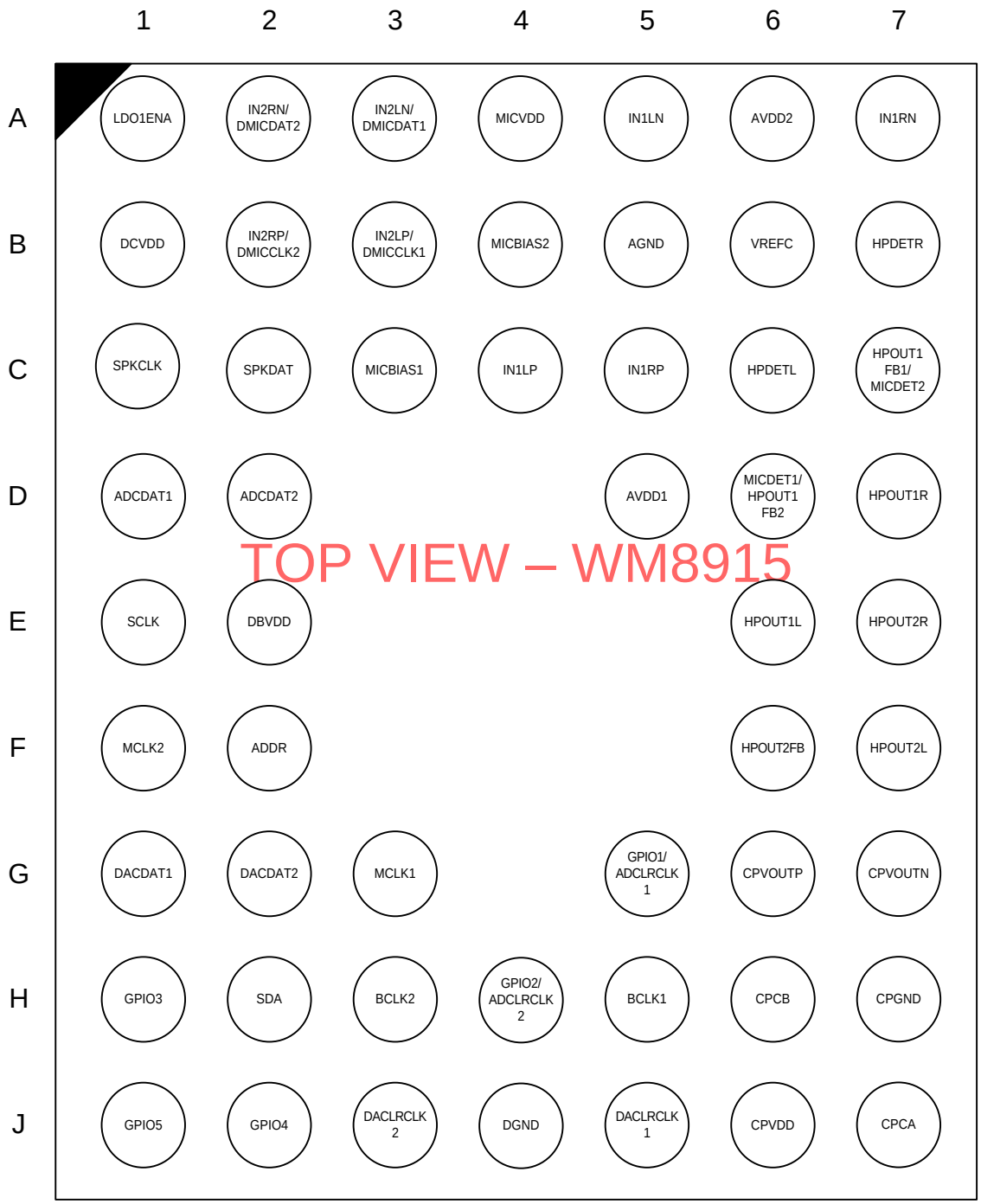
BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8915ECSN/R	-40°C to +85°C	54-ball W-CSP (pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 5,000

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	LDO1ENA	Digital Input	Enable pin for LDO1
A2	IN2RN/ DMICDAT2	Analogue Input / Digital Input	Right channel negative differential input 2 / Digital Microphone data input 2
A3	IN2LN/ DMICDAT1	Analogue Input / Digital Input	Left channel negative differential input 2 / Digital Microphone data input 1
A4	MICVDD	Supply / Analogue Output	Microphone supply / LDO2 output
A5	IN1LN	Analogue Input	Left channel inverting single-ended input 1 / Left channel negative differential input 1
A6	AVDD2	Supply	Analogue core supply
A7	IN1RN	Analogue Input	Right channel inverting single-ended input 1 / Right channel negative differential input 1
B1	DCVDD	Supply / Analogue Output	Digital core supply / LDO1 output
B2	IN2RP/ DMICCLK2	Analogue Input / Digital Output	Right channel positive differential input 2/ Digital Microphone clock output 2
B3	IN2LP/ DMICCLK1	Analogue Input / Digital Output	Left channel positive differential input 2/ Digital Microphone clock output 1
B4	MICBIAS2	Analogue Output	Microphone bias 2 (for microphone / accessory detection circuit)
B5	AGND	Supply	Analogue ground (Return path for AVDD1, AVDD2, MICVDD)
B6	VREFC	Analogue Output	Bandgap reference decoupling capacitor
B7	HPDETR	Analogue Input / Output	Headphone Right sense input
C1	SPKCLK	Digital Output	Digital Speaker (PDM) clock output
C2	SPKDAT	Digital Output	Digital Speaker (PDM) data output
C3	MICBIAS1	Analogue Output	Microphone bias 1 (digital microphone supply)
C4	IN1LP	Analogue Input	Left channel non-inverting single-ended input / Left channel positive differential input
C5	IN1RP	Analogue Input	Right channel non-inverting single-ended input / Right channel positive differential input
C6	HPDETL	Analogue Input / Output	Headphone Left sense input
C7	HPOUT1FB1/ MICDET2	Analogue Input	HPOUT1L and HPOUT1R ground feedback pin 1 Microphone & accessory sense input 2
D1	ADCDAT1	Digital Output	Audio interface 1 ADC digital audio data
D2	ADCDAT2	Digital Output	Audio interface 2 ADC digital audio data
D5	AVDD1	Supply	LDO2 input
D6	MICDET1/ HPOUT1FB2	Analogue Input	Microphone & accessory sense input 1 HPOUT1L and HPOUT1R ground feedback pin 2
D7	HPOUT1R	Analogue Output	Right headphone 1 output
E1	SCLK	Digital Input	Control interface clock input
E2	DBVDD	Supply	Digital buffer (I/O) supply / LDO1 input
E6	HPOUT1L	Analogue Output	Left headphone 1 output
E7	HPOUT2R	Analogue Output	Right headphone 2 output
F1	MCLK2	Digital Input	Master clock 2

PIN NO	NAME	TYPE	DESCRIPTION
F2	ADDR	Digital Input	Control interface 1 3-/4-wire (SPI) chip select or 2-wire (I2C) address select
F6	HPOUT2FB	Analogue Input	HPOUT2L and HPOUT2R ground loop noise rejection feedback
F7	HPOUT2L	Analogue Output	Left headphone 2 output
G1	DACDAT1	Digital Input	Audio interface 1 DAC digital audio data
G2	DACDAT2	Digital Input	Audio interface 2 DAC digital audio data
G3	MCLK1	Digital Input	Master clock 1
G5	GPIO1/ ADCLRCLK1	Digital Input / Output	General Purpose pin GPIO 1 / Audio interface 1 ADC (TX) left / right clock
G6	CPVOUTP	Analogue Output	Charge pump positive supply decoupling pin (HPOUT1 / HPOUT2)
G7	CPVOUTN	Analogue Output	Charge pump negative supply decoupling pin (HPOUT1 / HPOUT2)
H1	GPIO3	Digital Input / Output	General Purpose pin GPIO 3
H2	SDA	Digital Input / Output	Control interface data input and output / acknowledge output
H3	BCLK2	Digital Input / Output	Audio interface 2 bit clock
H4	GPIO2/ ADCLRCLK2	Digital Input / Output	General Purpose pin GPIO 2 / Audio interface 2 ADC (TX) left / right clock
H5	BCLK1	Digital Input / Output	Audio interface 1 bit clock
H6	CPCB	Analogue Output	Charge pump fly-back capacitor pin
H7	CPGND	Supply	Charge pump ground (Return path for CPVDD)
J1	GPIO5	Digital Input / Output	General Purpose pin GPIO 5
J2	GPIO4	Digital Input / Output	General Purpose pin GPIO 4
J3	DACLRCLK2	Digital Input / Output	Audio interface 2 DAC (RX) left / right clock (can also be used for ADC (TX) clock)
J4	DGND	Supply	Digital ground (Return path for DCVDD and DBVDD)
J5	DACLRCLK1	Digital Input / Output	Audio interface 1 DAC (RX) left / right clock (can also be used for ADC (TX) clock)
J6	CPVDD	Supply	Charge pump supply
J7	CPCA	Analogue Output	Charge pump fly-back capacitor pin

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
D1	ADCDAT1	DBVDD	DGND
D2	ADCDAT2	DBVDD	DGND
F2	ADDR	DBVDD	DGND
H5	BCLK1	DBVDD	DGND
H3	BCLK2	DBVDD	DGND
G1	DACDAT1	DBVDD	DGND
G2	DACDAT2	DBVDD	DGND
J5	DACLRCLK1	DBVDD	DGND
J3	DACLRCLK2	DBVDD	DGND
G5	GPIO1 / ADCLRCLK1	DBVDD	DGND
H4	GPIO2 / ADCLRCLK2	DBVDD	DGND
H1	GPIO3	DBVDD	DGND
J2	GPIO4	DBVDD	DGND
J1	GPIO5	DBVDD	DGND
A5	IN1LN	AVDD2	AGND
C4	IN1LP	AVDD2	AGND
A7	IN1RN	AVDD2	AGND
C5	IN1RP	AVDD2	AGND
A3	IN2LN / DMICDAT1	AVDD2 (IN2LN) or MICBIAS1 (DMICDAT1)	AGND (IN2LN) or DGND (DMICDAT1)
B3	IN2LP / DMICCLK1	AVDD2 (IN2LP) or MICBIAS1 (DMICCLK1)	AGND (IN2LP) or DGND (DMICCLK1)
A2	IN2RN / DMICDAT2	AVDD2 (IN2RN) or MICBIAS1 (DMICDAT2)	AGND (IN2RN) or DGND (DMICDAT2)
B2	IN2RP / DMICCLK2	AVDD2 (IN2RP) or MICBIAS1 (DMICCLK2)	AGND (IN2RP) or DGND (DMICCLK2)
A1	LDO1ENA	DBVDD	DGND
G3	MCLK1	DBVDD	DGND
F1	MCLK2	DBVDD	DGND
E1	SCLK	DBVDD	DGND
H2	SDA	DBVDD	DGND
C1	SPKCLK	DBVDD	DGND
C2	SPKDAT	DBVDD	DGND

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (AVDD1, MICVDD)	-0.3V	+4.5V
Supply voltages (AVDD2, DCVDD, DBVDD)	-0.3V	+2.5V
Supply voltages (CPVDD)	-0.3V	+2.2V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD2 +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_J	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See notes 3, 4	DCVDD	0.95	1.0	2.0	V
Digital supply range (I/O)	DBVDD	1.62	1.8	2.0	V
Analogue supply 1 range	AVDD1	1.71	3.0	3.6	V
Analogue supply 2 range	AVDD2	1.71	1.8	2.0	V
Charge Pump supply range	CPVDD	1.71	1.8	2.0	V
Microphone Bias supply See notes 5, 6	MICVDD	1.71	2.5	3.6	V
Ground	DGND, AGND, CPGND		0		V
Operating temperature range	T_A	-40		+85	ºC

Notes:

1. All digital and analogue grounds must always be within 0.3V of each other.
2. There is no power sequencing requirement; the supplies may be enabled in any order.
3. An internal LDO (powered by DBVDD) can be used to provide the DCVDD supply.
4. When DCVDD is supplied externally (not from LDO1), the DBVDD voltage must be greater than or equal to DCVDD.
5. An internal LDO (powered by AVDD1) can be used to provide the MICVDD supply.
6. When MICVDD is supplied externally (not from LDO2), the AVDD1 voltage must be greater than or equal to MICVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD=1.0V, AVDD2=DBVDD=CPVDD=1.8V, AVDD1=3.0V, MICVDD=2.5V, AGND=DGND=CPGND=0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (INxLN, INxLP, INxRN, INxRP)						
A1	Maximum Full-Scale PGA Input Signal Level. Note - for AVDD2<1.8V, the full scale input is reduced in proportion to AVDD2.	Single-ended PGA input (IN1LN, IN1LP, IN1RN, IN1RP)			0.5 -6.02	Vrms dBV
		Differential PGA input			1.0 0	Vrms dBV
B4	Input Resistance	Single-ended PGA input, gain = 0dB	5.25	7.5		kΩ
		Single-ended PGA input, gain = +31dB	1.33	1.9		
B5		Differential PGA input, gain = 0dB	42	60		
		Differential PGA input, gain = +31dB	2.31	3.3		
Input Programmable Gain Amplifiers (PGAs)						
B1	Minimum Programmable Gain			0		dB
B2	Maximum Programmable Gain			31		dB
B3	Programmable Gain Step Size	Guaranteed monotonic		1		dB
Output Programmable Gain Amplifiers (PGAs)						
C1	Minimum Programmable Gain			-9		dB
C2	Maximum Programmable Gain			0		dB
C3	Programmable Gain Step Size	Guaranteed monotonic		0.75		dB
ADC Input Path Performance (Differential Input from IN1LN/P or IN1RN/P)						
D1	SNR	A-weighted, ADC_OSR128=1	90	94		dB
D2	THD	-1dBV input		-83		dB
	THD+N	-1dBV input		-83	-75	dB
D3	Channel separation (L/R)	-1dBV input		-100		dB
D4	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		80		dB
		100mV pk-pk, 10kHz, any supply		70		
D5	Common Mode Rejection Ratio	0dBV input, 217Hz, PGA in differential mode, gain = 0dB		60		dB
		0dBV input, 217Hz, PGA in differential mode, gain = +30dB		70		
ADC Input Path Performance (Single-Ended Input from IN1LN, IN1LP, IN1RN or IN1RP)						
E1	SNR	A-weighted, ADC_OSR128=1	90	94		dB
E2	THD	-7dBV input		-83		dB
	THD+N	-7dBV input		-81	-72	dB
E3	Channel separation (L/R)	-7dBV input		-100		dB
E4	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		50		dB
		100mV pk-pk, 10kHz, any supply		50		
ADC Input Path Performance (Differential Input from IN2LN/P or IN2RN/P)						
F1	SNR	A-weighted, ADC_OSR128=1	90	94		dB
F2	THD	-1dBV input		-83		dB
	THD+N	-1dBV input		-83	-75	dB
F3	Channel separation (L/R)	-1dBV input		-100		dB
F4	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		80		dB
		100mV pk-pk, 10kHz, any supply		70		
F5	Common Mode Rejection Ratio	-20dBV input, 217Hz, PGA in differential mode, gain = 0dB		60		dB
		-20dBV input, 217Hz, PGA in differential mode, gain = +20dB		70		

Test Conditions

DCVDD=1.0V, AVDD2=DBVDD=CPVDD=1.8V, AVDD1=3.0V, MICVDD=2.5V, AGND=DGND=CPGND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

DAC Output Path (HPOUT1L, HPOUT1R, HPOUT2L, HPOUT2R), Line Load R_L = 10kΩ						
G1	SNR	A-weighted, DAC_OSR128=1	92	100		dB
G2	THD	1Vrms output		-81		dB
	THD+N	1Vrms output		-81		dB
G3	Channel Separation (L/R)	1Vrms output		-100		dB
G4	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		80		dB
		100mV pk-pk, 10kHz, any supply		65		
DAC Output Path (HPOUT1L, HPOUT1R, HPOUT2L, HPOUT2R), Headphone Load R_L = 32Ω						
G6	SNR	A-weighted, DAC_OSR128=1	92	99		dB
G7	THD	P_O = 20mW		-80		dB
	THD+N	P_O = 20mW		-78		dB
	THD	P_O = 5mW		-80		dB
	THD+N	P_O = 5mW		-79		dB
G8	Channel Separation (L/R)	P_O = 20mW		-98		dB
G9	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		80		dB
		100mV pk-pk, 10kHz, any supply		65		
DAC Output Path (HPOUT1L, HPOUT1R, HPOUT2L, HPOUT2R), Headphone Load R_L = 16Ω						
G11	SNR	A-weighted, DAC_OSR128=1	92	99		dB
G12	THD	P_O = 20mW		-76		dB
	THD+N	P_O = 20mW		-74		dB
	THD	P_O = 5mW		-80	-75	dB
	THD+N	P_O = 5mW		-79	-75	dB
G13	Channel Separation (L/R)	P_O = 20mW		-95		dB
G14	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		80		dB
		100mV pk-pk, 10kHz, any supply		65		
Headphone Output Driver (HPOUT1L, HPOUT1R, HPOUT2L, HPOUT2R)						
	Minimum output load resistance		15			Ω
	Maximum output load capacitance				2	nF

Test Conditions

DCVDD=1.0V, AVDD2=DBVDD=CPVDD=1.8V, AVDD1=3.0V, MICVDD=2.5V, AGND=DGND=CPGND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias (Note: No capacitor on MICBIAS)						
H1	Bias Voltage (Regulator mode) (MICBIAS1 or MICBIAS2, 1.0mA load current)	MICBx_LVL = 000b	-4%	1.5	+4%	V
		MICBx_LVL = 001b	-4%	1.8	+4%	
		MICBx_LVL = 010b	-4%	1.9	+4%	
		MICBx_LVL = 011b	-4%	2.0	+4%	
		MICBx_LVL = 100b	-4%	2.2	+4%	
		MICBx_LVL = 101b	-4%	2.4	+4%	
		MICBx_LVL = 110b	-4%	2.5	+4%	
		MICBx_LVL = 111b	-4%	2.6	+4%	
H2	Bias Voltage (Bypass mode) (MICBIAS1 or MICBIAS2, 1mA load current)		MICVDD - 80mV		MICVDD	V
H3	Bias Current (Regulator Mode)	MICVDD - MICBIASn >200mV			2.4	mA
H4	Bias Current (Bypass mode)				3.6	mA
H5	Output Noise Density @ 1kHz	MICBx_LVL = 100b, Output current = 1mA		60		nV/√Hz
H6	Integrated Noise Voltage (100Hz to 7kHz)	MICBx_LVL = 100b, Output current = 1mA		4.5		uVrms
H7	PSRR (100mV pk-pk on AVDD1)	217Hz		100		dB
		10kHz		80		dB
Digital Input / Output (except DMICDATn and DMICCLKn)						
J1	Input HIGH Level		0.7×DBVDD			V
J2	Input LOW Level				0.3×DBVDD	V
Note that digital input pins should not be left unconnected / floating. Internal pull-up/pull-down resistors may be enabled on GPIO pins if required.						
J3	Output HIGH Level	I_{OH} = 4mA	0.8×DBVDD			V
J4	Output LOW Level	I_{OL} = -4mA			0.2×DBVDD	V
J5	Pin capacitance			10		pF
J6	Pin leakage		-0.9		0.9	uA
Digital Microphone Input / Output (DMICDATn and DMICCLKn)						
J7	DMICDATn input HIGH Level	MICBIAS1 = MICVDD, MICB1_MODE = 1	0.7 × MICBIAS1			V
J8	DMICDATn input LOW Level	MICBIAS1 = MICVDD, MICB1_MODE = 1			0.3 x MICBIAS1	V
J11	Pin capacitance			10		pF
J12	Pin leakage		-0.9		0.9	µA
Note that digital input pins should not be left unconnected / floating. Internal pull-up/pull-down resistors may be enabled on GPIO pins if required.						
J9	DMICCLK output HIGH Level	MICBIAS1 = MICVDD, MICB1_MODE = 1	0.8 × MICBIAS1			V
J10	DMICCLK output LOW Level	MICBIAS1 = MICVDD, MICB1_MODE = 1			0.2 x MICBIAS1	V
Digital Pull-Up / Pull-Down						
	Pull-Up resistance	Measured at HIGH Level output condition	40	60	80	kΩ
	Pull-Down resistance	Measured at LOW Level output condition	40	60	80	kΩ

Test Conditions

DCVDD=1.0V, AVDD2=DBVDD=CPVDD=1.8V, AVDD1=3.0V, MICVDD=2.5V, AGND=DGND=CPGND=0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLL						
K4	Lock time	F_{REF} = 13MHz			0.3	ms
		F_{REF} = 32kHz			2	
K5	FLL Clock (GPIO output) duty cycle		45:55		55:45	%
LDO1 Regulator						
L3	Output voltage (DCVDD)		0.9		1.2	V
L1	Start-up Time (for LDO1 output to exceed 0.95V)	VREFC Cap = 1uF, DCVDD Cap = 4.7uF, LDO1 in Bypass Mode			5	ms
LDO2 Regulator						
M3	Output voltage (MICVDD)		1.7		2.8	V
M1	Start-up Time (for LDO2 output to reach 90% of final value)	VREFC Cap = 1uF, MICVDD Cap = 4.7uF, LDO2 in Normal Mode			1.5	ms
		VREFC Cap = 1uF, MICVDD Cap = 4.7uF, LDO2 in Bypass Mode			3	
Charge Pump						
N3	CPVOUTP (CP mode is controlled automatically)	Normal mode		CPVDD		V
		Low power mode		CPVDD/2		
N4	CPVOUTN (CP mode is controlled automatically)	Normal mode		-CPVDD		V
		Low power mode		-CPVDD/2		
N5	Maximum Total Output Power			100		mW
N1	Start-up Time				500	µs
Wired Accessory Interface						
P1	Load impedance detection ranges	HPDETL or HPDETR	-30%	8 to 128	+30%	Ω
	Load impedance ranges for valid button detection (pull-down resistor in headset) Measured on MICDET1 or MICDET2, 2.2kΩ (2%) MICBIAS resistor, MICBn_LVL = 100b (2.2V). Note these characteristics assume no other component is connected to MICDETn. See "Applications Information" for recommended external components when a typical microphone is present.	for MICD_LVL[0] = 1	0		3	Ω
		for MICD_LVL[1] = 1	13.33		15.27	
		for MICD_LVL[2] = 1	27.16		30.96	
		for MICD_LVL[3] = 1	42.48		49.47	
		for MICD_LVL[4] = 1	65		85	
		for MICD_LVL[5] = 1	114		155.24	
		for MICD_LVL[6] = 1	191		329.87	
		for MICD_LVL[8] = 1	475		30000	
P2	Programmable debounce time		0		0.5	s
P3	Programmable debounce step size			1		ms

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the measured signal level in the idle channel at the test signal frequency relative to the signal level at the output of the active channel. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
5. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
6. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCKS & FREQUENCY LOCKED LOOP (FLL)

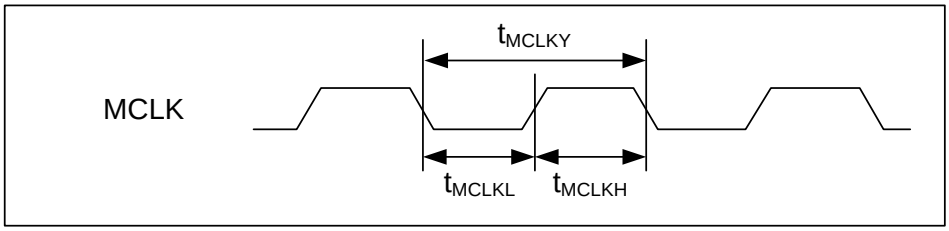


Figure 1 Master Clock Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing (MCLK1 and MCLK2)						
MCLK cycle time	T_{MCLKY}	MCLK as input to FLL, FLLn_REFCLK_DIV = 10	29.4			ns
		MCLK as input to FLL, FLLn_REFCLK_DIV = 01	37			
		MCLK as input to FLL, FLLn_REFCLK_DIV = 00	74			
		FLL not used, SYSCLK_DIV = 1	40			ns
		FLL not used, SYSCLK_DIV = 0	80			ns
MCLK duty cycle (= T_{MCLKH} : T_{MCLKL})			60:40		40:60	
Frequency Locked Loop (FLL)						
FLL input frequency		FLL_REFCLK_DIV = 00	0.032		13.5	MHz
		FLL_REFCLK_DIV = 01	0.064		27	
		FLL_REFCLK_DIV = 10	0.128		34	
Internal Clocking						
SYSCLK frequency		48kHz (and integer related) audio sample rates		12.288		MHz
		44.1kHz (and integer related) audio sample rates		11.2896		

AUDIO INTERFACE TIMING

DIGITAL MICROPHONE (DMIC) INTERFACE TIMING

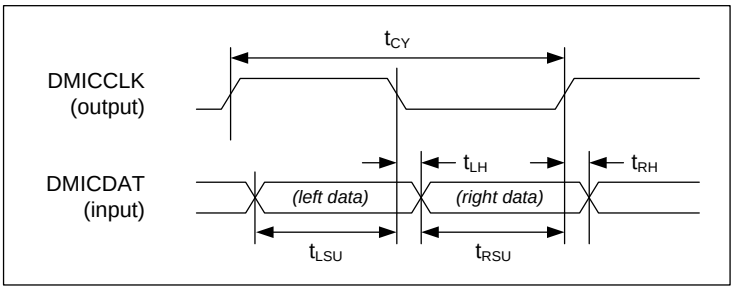


Figure 2 Digital Microphone Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Microphone Interface Timing					
DMICCLK cycle time	t_{CY}	325		651	ns
DMICDAT (Left) setup time to falling DMICCLK edge	t_{LSU}	15			ns
DMICDAT (Left) hold time from falling DMICCLK edge	t_{LH}	0			ns
DMICDAT (Right) setup time to rising DMICCLK edge	t_{RSU}	15			ns
DMICDAT (Right) hold time from rising DMICCLK edge	t_{RH}	0			ns

DIGITAL SPEAKER (PDM) INTERFACE TIMING

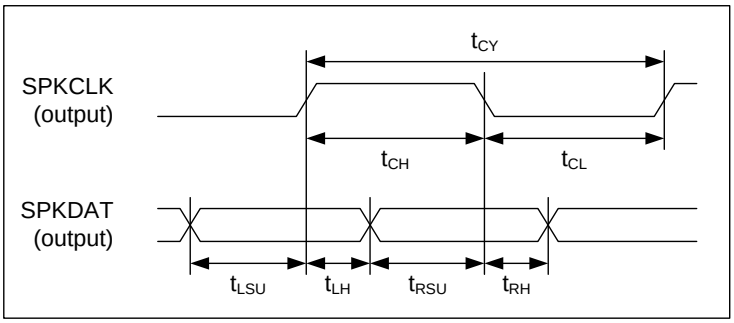


Figure 3 Digital Speaker (PDM) Interface Timing - Mode A

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PDM Audio Interface Timing					
SPKCLK cycle time	t_{CY}	160	163	340	ns
SPKCLK pulse width high	t_{CH}	70	80		ns
SPKCLK pulse width low	t_{CL}	70	80		ns
SPKDAT set-up time to SPKCLK rising edge (Left channel)	t_{LSU}	30			ns
SPKDAT hold time from SPKCLK rising edge (Left channel)	t_{LH}	30			ns
SPKDAT set-up time to SPKCLK falling edge (Right channel)	t_{RSU}	30			ns
SPKDAT hold time from SPKCLK falling edge (Right channel)	t_{RH}	30			ns

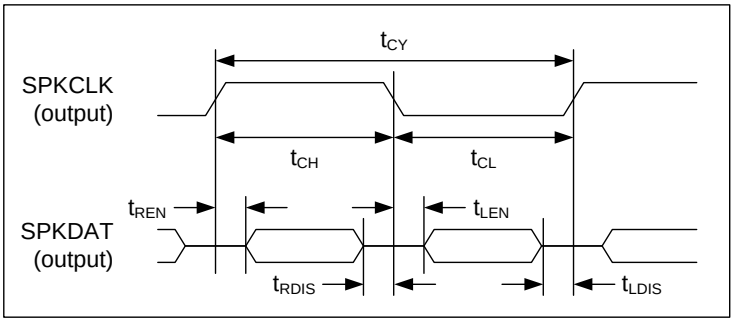


Figure 4 Digital Speaker (PDM) Interface Timing - Mode B

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PDM Audio Interface Timing					
SPKCLK cycle time	t_{CY}	160	163	340	ns
SPKCLK pulse width high	t_{CH}	70	80		ns
SPKCLK pulse width low	t_{CL}	70	80		ns
SPKDAT enable from SPKCLK rising edge (Right channel)	t_{REN}			15	ns
SPKDAT disable to SPKCLK falling edge (Right channel)	t_{RDIS}			5	ns
SPKDAT enable from SPKCLK falling edge (Left channel)	t_{LEN}			15	ns
SPKDAT disable to SPKCLK rising edge (Left channel)	t_{LDIS}			5	ns

AIF1 / AIF2 - MASTER MODE

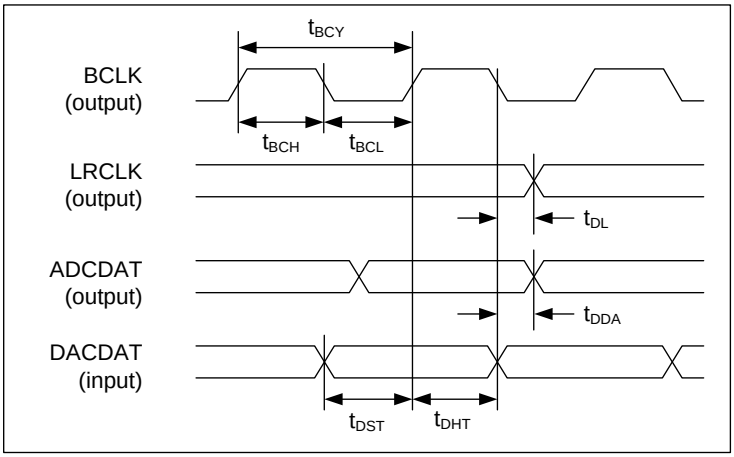


Figure 5 Audio Interface Timing - Master Mode

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
BCLK cycle time	t_{BCY}	160			ns
BCLK pulse width high (SYSCLK_RATE = 1)	t_{BCH}	64			ns
BCLK pulse width low (SYSCLK_RATE = 1)	t_{BCL}	64			ns
BCLK pulse width high (SYSCLK_RATE = 0)	t_{BCH}	72			ns
BCLK pulse width low (SYSCLK_RATE = 0)	t_{BCL}	72			ns
LRCLK propagation delay from BCLK falling edge	t_{DL}			20	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			20	ns
DACDAT setup time to BCLK rising edge	t_{DST}	20			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AIF1 / AIF2 - SLAVE MODE

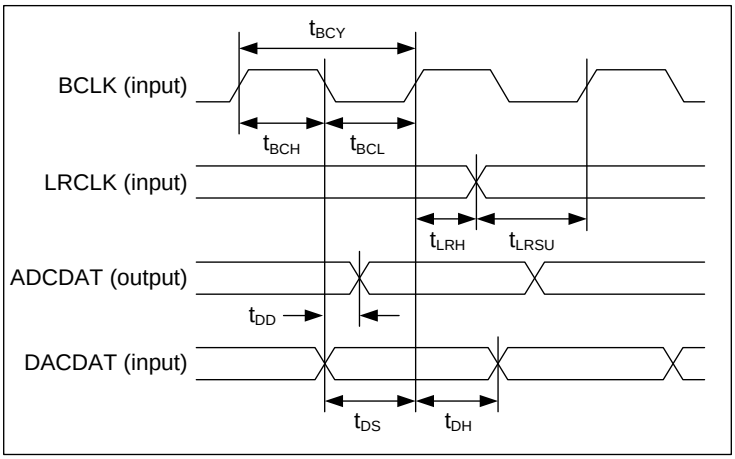


Figure 6 Audio Interface Timing – Slave Mode

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
BCLK cycle time	t_{BCY}	160			ns
BCLK pulse width high	t_{BCH}	64			ns
BCLK pulse width low	t_{BCL}	64			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	20			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns
DACDAT set-up time to BCLK rising edge	t_{DS}	20			ns

CONTROL INTERFACE TIMING

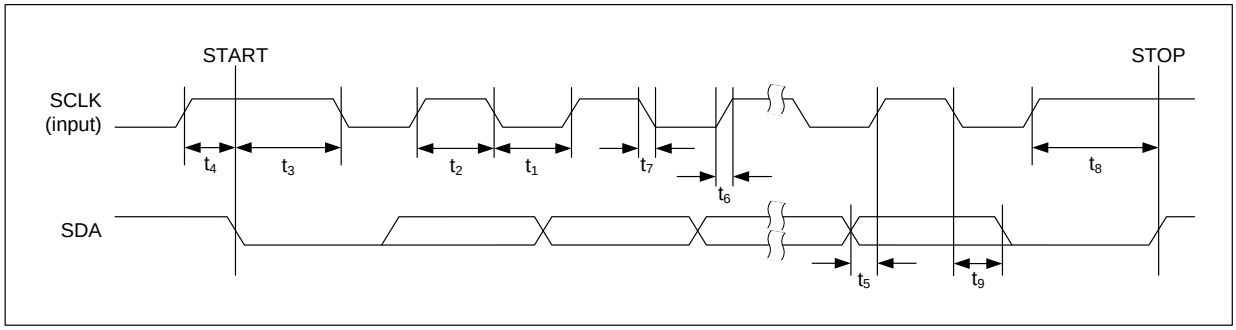


Figure 7 Control Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency				1000	kHz
SCLK Low Pulse-Width	t_1	500			ns
SCLK High Pulse-Width	t_2	260			ns
Hold Time (Start Condition)	t_3	260			ns
Setup Time (Start Condition)	t_4	260			ns
Data Setup Time	t_5	50			ns
SDA, SCLK Rise Time	t_6			120	ns
SDA, SCLK Fall Time	t_7			120	ns
Setup Time (Stop Condition)	t_8	260			ns
Data Hold Time	t_9			450	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		50	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8915 is a low power, high quality audio codec designed to interface with a wide range of processors and digital audio components. A high level of mixed-signal integration in a very small footprint makes it ideal for portable applications such as mobile phones.

Two separate audio interfaces are available in order to provide independent and fully asynchronous connections to multiple processors. These interfaces provide input and output paths to the ADCs, DACs and digital mixing functions on the WM8915. A flexible signal routing capability between the two interfaces is also provided.

Four digital microphone input channels are available to support advanced multi-microphone applications such as noise reduction. An integrated microphone activity monitor is available to enable the processor to sleep during periods of microphone inactivity, saving power.

Up to four analogue inputs can be connected, to allow interfacing to microphones or line level audio signals. The WM8915 supports single-ended and differential analogue input connections. Signal routing to the output mixers and within the CODEC has been designed for maximum flexibility to support a wide variety of usage modes.

Four DAC channels are available to support use cases requiring up to four headphone output channels. A stereo digital (SPDM) output is provided for connection to external speaker drivers; flexible signal routing is provided between the DACs and the SPDM outputs.

Two pairs of ground-referenced headphone outputs are provided; these are powered from an integrated Charge Pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. A DC Servo circuit is available for DC offset correction, suppressing pops and reducing power consumption. Ground loop feedback is available on the headphone outputs, providing rejection of noise on the ground connections. All outputs have integrated pop and click suppression features.

The ADCs and DACs are of hi-fi quality, using a 24-bit low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports mixed sample rates, whilst an integrated ultra-low power FLL provides additional flexibility. A configurable high pass filter is available in all ADC and digital MIC paths for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise. A digital mixing path from the ADC or digital MICs to the DAC provides a sidetone of enhanced quality during voice calls. DAC soft mute and un-mute is available for pop-free music playback.

The integrated Dynamic Range Controllers (DRC) and ReTune™ Mobile 5-band parametric equaliser (EQ) provide further processing capability of the digital audio paths. The DRC provides compression and signal level control to improve the handling of unpredictable signal levels. ‘Anti-clip’ and ‘quick release’ algorithms improve intelligibility in the presence of transients and impulsive noises. The EQ provides the capability to tailor the audio path according to the frequency characteristics of an earpiece or loudspeaker, and/or according to user preferences.

External accessory detection is provided to measure the impedance of headphones and to detect push-switch operation and microphone connection. These features enable intelligent signal path configuration to be implemented according to the status of any external accessory components.

The WM8915 has two highly flexible digital audio interfaces, supporting a number of protocols, including I^2S, DSP and Left-Justified formats, and can operate in master or slave modes. Each interface is independently configurable on the respective transmit and receive paths. Time division multiplexing (TDM) is supported on both interfaces to allow multiple devices to stream data simultaneously on the same bus, saving space and power.

Up to six digital input / output channels can be supported simultaneously via the TDM channels on digital audio interface 1 (AIF1). It is also possible to support different sample rates simultaneously on any of the input or output paths of AIF1.

A powerful digital mixing core allows data from each input channel and from the ADCs and digital MICs to be mixed and re-routed back to a different audio interface and to the 4 DAC output channels.

The system clock (SYSCLK) provides clocking for the ADCs, DACs, DSP core, digital audio interface and other circuits. SYSCLK can be derived directly from the MCLK1 or MCLK2 pins or from the integrated FLL, providing flexibility to support a wide range of clocking schemes. A wide range of typical portable system MCLK frequencies is supported.

The WM8915 uses a standard 2-wire control interface, providing full software control of all features, together with device register readback. An integrated Control Write Sequencer enables automatic scheduling of control sequences; commonly-used signal configurations may be selected using ready-programmed sequences, including time-optimised control of the WM8915 pop suppression features. It is an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

Versatile GPIO functionality is provided, with support for button/accessory detect inputs, or for clock, system status, or programmable logic level output for control of additional external circuitry. Interrupt logic, status readback and de-bouncing options are supported within this functionality.

ANALOGUE INPUT SIGNAL PATH

The WM8915 has four dedicated analogue input pins, which may be used to support connections to multiple microphone or line input sources. Analogue input is also supported using the digital microphone interface pins, which may also be configured as analogue inputs if required.

A maximum of two analogue input signal paths may be enabled at once. The left and right input PGAs can each be configured to select a single-ended or a differential input connection. The selected inputs are routed to the Analogue to Digital Converters (ADCs), and can be routed to the Digital Audio Interface output and/or mixed into the Output Signal Paths.

The Left Input PGA can select IN1LN or IN1LP as a single-ended input, or can select a differential input configuration on the IN1LP - IN1LN pins or a differential input on the IN2LP - IN2LN pins.

The Right Input PGA can select IN1RN or IN1RP as a single-ended input, or can select a differential input configuration on the IN1RP - IN1RN pins or a differential input on the IN2RP - IN2RN pins.

Input PGA gain from 0dB to +31dB is available on each input channel.

The WM8915 input signal paths and control registers are illustrated in Figure 8.

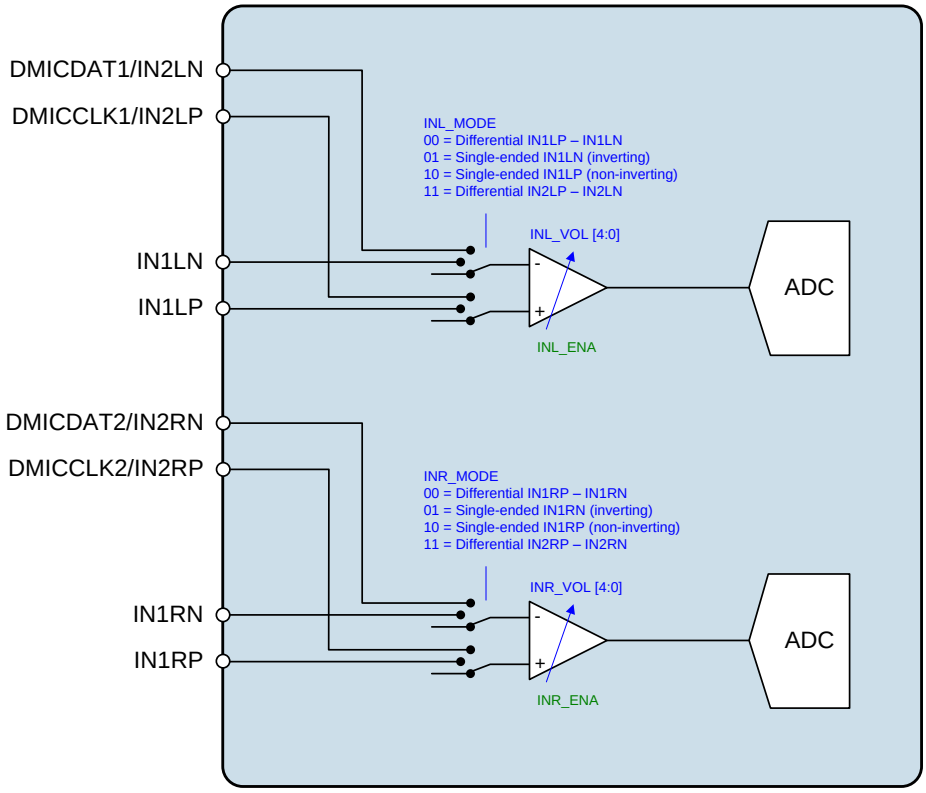


Figure 8 Control Registers for Input Signal Path

MICROPHONE BIAS CONTROL

There are two MICBIAS generators which provide low noise reference voltages suitable for biasing electret condenser (ECM) type microphones via an external resistor. Refer to the “Applications Information” section for recommended external components.

The MICBIAS outputs can be independently enabled using the MICB1_ENA and MICB2_ENA register bits. Under default conditions, a smooth pop-free profile of the MICBIAS outputs is implemented when MICB1_ENA or MICB2_ENA is enabled or disabled; a faster transition can be selected by setting the MICB1_RATE and MICB2_RATE registers as described in Table 1.

When a MICBIAS output is disabled, the output pin can be configured to be floating or to be actively discharged. This is selected using the MICB1_DISCH and MICB2_DISCH register bits.

The MICBIAS generators can each operate as a voltage regulator or in bypass mode.

In Regulator mode, the output voltage is selected using the MICB1_LVL and MICB2_LVL register bits. In this mode, MICVDD must be at least 200mV greater than the required MICBIAS output voltages. The MICBIAS outputs are powered from the MICVDD supply pin, and use the internal bandgap circuit as a reference.

Note that, in Regulator mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. It is important that parasitic capacitances on the MICBIAS1 or MICBIAS2 pins do not exceed 50pF in Regulator mode.

In Bypass mode, the output pin (MICBIAS1 or MICBIAS2) is connected directly to MICVDD. This enables a low power operating state. Note that, if a capacitive load is connected to MICBIAS1 or MICBIAS2 (eg. for a digital microphone supply), then the respective MICBIAS generator must be configured in Bypass mode.

The MICBIAS configuration is illustrated in Figure 9.

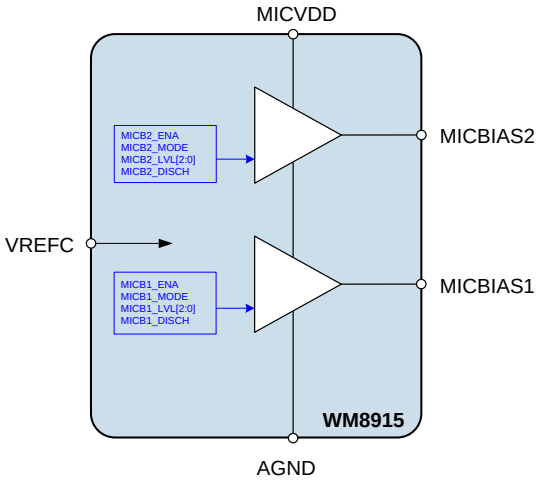


Figure 9 MICBIAS Generator

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (0001h) Power Management (1)	9	MICB2_ENA	0	Microphone Bias 2 Enable 0 = Disabled 1 = Enabled
	8	MICB1_ENA	0	Microphone Bias 1 Enable 0 = Disabled 1 = Enabled
R32 (0020h) MICBIAS (1)	5	MICB1_RATE	1	Microphone Bias 1 Rate 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down
	4	MICB1_MODE	0	Microphone Bias 1 Mode 0 = Regulator mode 1 = Bypass mode
	3:1	MICB1_LVL [2:0]	100	Microphone Bias 1 Voltage Control (when MICB1_MODE = 0) 000 = 1.5V 001 = 1.8V 010 = 1.9V 011 = 2.0V 100 = 2.2V 101 = 2.4V 110 = 2.5V 111 = 2.6V
	0	MICB1_DISCH	1	Microphone Bias 1 Discharge 0 = MICBIAS1 floating when disabled 1 = MICBIAS1 discharged when disabled
R33 (0021h) MICBIAS (2)	5	MICB2_RATE	1	Microphone Bias 2 Rate 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down
	4	MICB2_MODE	0	Microphone Bias 2 Mode 0 = Regulator mode 1 = Bypass mode
	3:1	MICB2_LVL [2:0]	100	Microphone Bias 2 Voltage Control (when MICB2_MODE = 0) 000 = 1.5V 001 = 1.8V 010 = 1.9V 011 = 2.0V 100 = 2.2V 101 = 2.4V 110 = 2.5V 111 = 2.6V
	0	MICB2_DISCH	1	Microphone Bias 2 Discharge 0 = MICBIAS2 floating when disabled 1 = MICBIAS2 discharged when disabled

Table 1 Microphone Bias Control

Note that the maximum source current capability for MICBIAS1 and MICBIAS2 is 2.4mA each in Regulator mode. The external biasing resistance must be large enough to limit each MICBIAS current to 2.4mA across the full microphone impedance range. The maximum source current for MICBIAS1 and MICBIAS2 is 3.6mA each in Bypass mode, as described in the “Electrical Characteristics”.

MICROPHONE ACCESSORY DETECT

The WM8915 provides a microphone detection function, which uses impedance measurement to detect one or more different external accessory connections. This feature is described in the “External Accessory Detection” section.

INPUT PGA ENABLE

The Input PGAs are enabled using register bits INL_ENA and INR_ENA, as described in Table 2. The PGAs must be enabled for microphone or line input on the respective input pins.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (0002h) Power Management (2)	5	INL_ENA	0	INL Input PGA Enable 0 = Disabled 1 = Enabled
	4	INR_ENA	0	INR Input PGA Enable 0 = Disabled 1 = Enabled

Table 2 Input PGA Enable

INPUT PGA CONFIGURATION

Each of the Input PGAs can operate in a single-ended or differential mode. In single-ended mode, a single pin is selected as the input source. In differential mode, a pair of input pins is connected to the Input PGA.

Configuration of the Input PGAs to the WM8915 input pins is controlled using the INL_MODE and INR_MODE register fields shown in Table 3.

Note that the IN2LN, IN2LP, IN2RN and IN2RP pins also support digital microphone interface functions. Analogue input is not possible on these pins when the digital microphone function is enabled on the same pin. See “Digital Microphone Interface” for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (0012h) Line Input Control	3:2	INL_MODE [1:0]	00	Left Input PGA Mode 00 = Differential (IN1LP - IN1LN) 01 = Single-ended inverting (IN1LN) 10 = Single-ended non-inverting (IN1LP) 11 = Differential (IN2LP - IN2LN) Note that IN2LN and IN2LP cannot support analogue input when DMIC1_FN is enabled.
	1:0	INR_MODE [1:0]	00	Right Input PGA Mode 00 = Differential (IN1RP - IN1RN) 01 = Single-ended inverting (IN1RN) 10 = Single-ended non-inverting (IN1RP) 11 = Differential (IN2RP - IN2RN) Note that IN2RN and IN2RP cannot support analogue input when DMIC2_FN is enabled.

Table 3 Input PGA Configuration

INPUT PGA VOLUME CONTROL

Each of the Input PGAs has an independently controlled gain range of 0dB to +31dB in 1dB steps.

To prevent "zipper noise", a zero-cross function is provided on the input PGAs. When this feature is enabled, volume updates will not take place until a zero-crossing is detected. In the case of a long period without zero-crossings, a timeout function is provided. When the zero-cross function is enabled, the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout clock is enabled using TOCLK_ENA, the timeout period is set by TOCLK_DIV. See “Clocking and Sample Rates” for more information on these fields.

The IN_VU bits control the loading of the input PGA volume data. When IN_VU is set to 0, the PGA volume data will be loaded into the respective control register, but will not actually change the gain setting. The INL and INR volume settings are both updated when a 1 is written to IN_VU; this makes it possible to update the gain of the left and right signal paths simultaneously.

The Input PGA Volume Control register fields are described in Table 4 and Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (0010h) Left Line Input Volume	7	IN_VU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause INL and INR input PGA volumes to be updated simultaneously
	5	INL_ZC	0	INL PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	INL_VOL [4:0]	00000	INL Volume 0dB to +31dB in 1dB steps 00h = 0dB 01h = 1dB … (1dB steps) 1Fh = 31dB (See Table 5 for volume range)
R17 (0011h) Right Line Input Volume	7	IN_VU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause INL and INR input PGA volumes to be updated simultaneously
	5	INR_ZC	0	INR PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	4:0	INR_VOL [4:0]	00000	INR Volume 0dB to +31dB in 1dB steps 00h = 0dB 01h = 1dB … (1dB steps) 1Fh = 31dB (See Table 5 for volume range)

Table 4 Input PGA Volume Control

INL_VOL [4:0], INR_VOL [4:0]	VOLUME (dB)	INL_VOL [4:0], INR_VOL [4:0]	VOLUME (dB)
00000	0	10000	16
00001	1	10001	17
00010	2	10010	18
00011	3	10011	19
00100	4	10100	20
00101	5	10101	21
00110	6	10110	22
00111	7	10111	23
01000	8	11000	24
01001	9	11001	25
01010	10	11010	26
01011	11	11011	27
01100	12	11100	28
01101	13	11101	29
01110	14	11110	30
01111	15	11111	31

Table 5 Input PGA Volume Range

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8915 uses stereo 24-bit sigma-delta ADCs. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC oversample rate can be adjusted, if required, to reduce power consumption - see “Clocking and Sample Rates” for details. The ADC full scale input level is proportional to AVDD2 - see “Electrical Characteristics”. Any input signal greater than full scale may overload the ADC and cause distortion.

The ADCs are enabled by the ADCL_ENA and ADCR_ENA register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (0003h) Power Management (3)	1	ADCL_ENA	0	Left ADC Enable 0 = ADC disabled 1 = ADC enabled
	0	ADCR_ENA	0	Right ADC Enable 0 = ADC disabled 1 = ADC enabled

Table 6 ADC Enable Control

The digital volume control between the ADCs and Audio Interface AIF1 is controlled by the DSP1TXL_VOL and DSP1TXR_VOL registers. The digital volume control between the ADCs and Audio Interface AIF2 is controlled by the DSP2TXL_VOL and DSP2TXR_VOL registers. See “Digital Mixing” for further details.

The digital microphone inputs and the ADC outputs are routed to the DSP1 and DSP2 output (transmit) paths via multiplexers. See “Digital Mixing” for further details.

The digital microphone inputs and the ADC outputs can also be routed, in a limited number of configurations, to the digital mixing output bus, via the digital sidetone signal paths. See “Digital Mixing” for further details.

DIGITAL MICROPHONE INTERFACE

The WM8915 supports a four-channel digital microphone interface. Up to two pairs of digital microphone inputs can be selected at once, routed to the DSP1 and DSP2 output (transmit) paths. The digital microphone inputs can also be routed to the digital mixing output bus, via the digital sidetone signal paths.

Two channels of audio data are multiplexed on each of the DMICDAT1 and DMICDAT2 pins. Each pair of audio channels is clocked using the respective output pin DMICCLK1 and DMICCLK2.

The DMICDAT1 and DMICCLK1 pins must be selected as digital microphone interface pins by setting DMIC1_FN=1. Note that these pins cannot be used as analogue inputs when DMIC1_FN=1.

The DMICDAT2 and DMICCLK2 pins must be selected as digital microphone interface pins by setting DMIC2_FN=1. Note that these pins cannot be used as analogue inputs when DMIC2_FN=1.

The digital microphone interface is referenced to the MICBIAS1 voltage domain; the MICBIAS1 output must be enabled (MICB1_ENA = 1) when using the digital microphone interface.

The MICBIAS1 generator is suitable for use as a low noise supply for the digital microphones. Note that, if the capacitive load on the MICBIAS1 generator exceeds 50pF (eg. due to a decoupling capacitor or long PCB trace), then the MICBIAS1 generator must be configured in Bypass mode. See "Analogue Input Signal Path" for details of the MICBIAS1 generator.

When digital microphone input is enabled, the WM8915 outputs a clock signal on the respective DMICCLK1 or DMICCLK2 pin. The DMICCLK frequency is dependent on the DMIC_OSR64 register, as described in Table 7. See "Clocking and Sample Rates" for details of the DMIC_OSR64 register.

CONDITION	DMICCLK FREQUENCY
DMICCLK_OSR64 = 1 (Default)	3.072MHz
DMICCLK_OSR64 = 0	1.536MHz
Note: The quoted DMICCLK frequency assumes SYSCLK frequency of 12.288MHz. The DMICCLK frequency scales proportionately for other SYSCLK frequencies (eg. 11.2896MHz).	

Table 7 DMICCLK Frequency

A pair of digital microphones is connected as illustrated in Figure 10. The microphones must be configured to ensure that the Left mic transmits a data bit when the respective DMICCLK is high, and the Right mic transmits a data bit when DMICCLK is low. The WM8915 samples the digital microphone data at the end of each DMICCLK phase. Each microphone must tri-state its data output when the other microphone is transmitting.

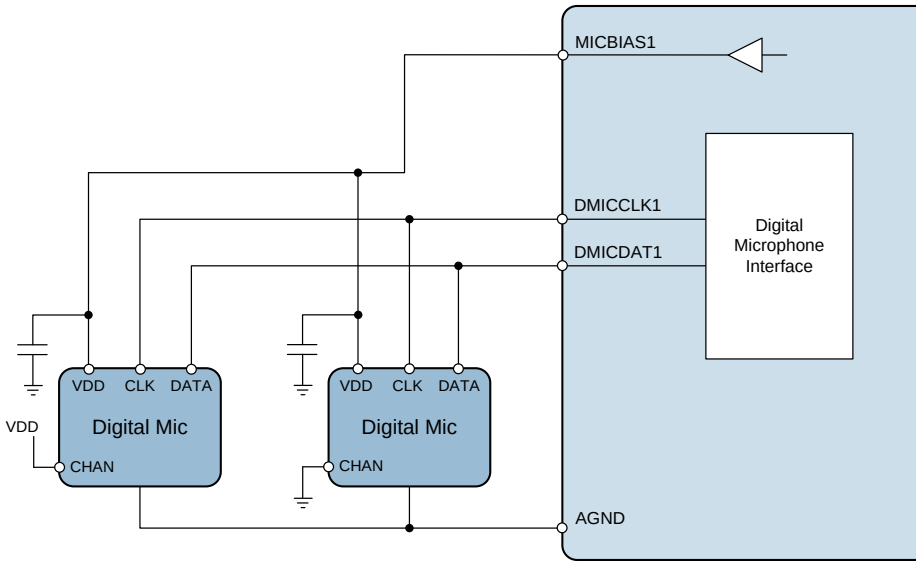


Figure 10 Digital Microphone Input

Each of the four digital microphone channels is enabled using the control bits in Register R0003, as described in Table 8.

Two microphone channels are interleaved on each of DMICDAT1 and DMICDAT2. The timing is illustrated in Figure 11.

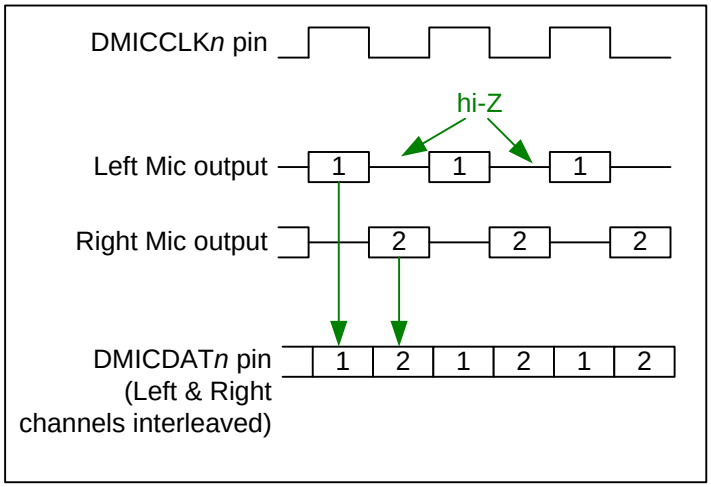


Figure 11 Digital Microphone Interface Timing

The four digital microphone channels can be routed to the output paths of AIF1 and AIF2. They can also be routed, in a limited number of configurations, to the digital mixing output bus, via the digital sidetone signal paths. See “Digital Mixing” for further details.

The digital microphone interface control fields are described in Table 8.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (0003h) Power Management (3)	5	DMIC2L_ENA	0	Digital microphone DMICDAT2 Left channel enable 0 = Disabled 1 = Enabled
	4	DMIC2R_ENA	0	Digital microphone DMICDAT2 Right channel enable 0 = Disabled 1 = Enabled
	3	DMIC1L_ENA	0	Digital microphone DMICDAT1 Left channel enable 0 = Disabled 1 = Enabled
	2	DMIC1R_ENA	0	Digital microphone DMICDAT1 Right channel enable 0 = Disabled 1 = Enabled
R7 (0007h) Power Management (7)	9	DMIC2_FN	0	DMICCLK2 and DMICDAT2 function 0 = Disabled 1 = Digital microphone enabled on DMICLK2 / DMICDAT2. Note that IN2RN and IN2RP cannot support analogue input when DMIC2_FN is enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8	DMIC1_FN	0	DMICCLK1 and DMICDAT1 function 0 = Disabled 1 = Digital microphone interface on DMICLK1 / DMICDAT1. Note that IN2LN and IN2LP cannot support analogue input when DMIC1_FN is enabled.

Table 8 Digital Microphone Interface Control

The digital microphone inputs and the ADC outputs are routed to the DSP1 and DSP2 output (transmit) paths via multiplexers. See “Digital Mixing” for further details.

The digital microphone inputs and the ADC outputs can also be routed, in a limited number of configurations, to the digital mixing output bus, via the digital sidetone signal paths. See “Digital Mixing” for further details.

DIGITAL PULL-UP AND PULL-DOWN

The WM8915 provides integrated pull-down resistors on the DMICDAT1 and DMICDAT2 pins. This provides a flexible capability for interfacing with other devices. Each of the pull-down resistors can be configured independently using the register bits described in Table 9.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1824 (0720h) Pull Control (1)	12	DMICDAT2_PD	0	DMICDAT2 Pull-Down enable 0 = Disabled 1 = Enabled
	10	DMICDAT1_PD	0	DMICDAT1 Pull-Down enable 0 = Disabled 1 = Enabled

Table 9 Digital Pull-Up and Pull-Down Control

DIGITAL CORE ARCHITECTURE

The WM8915 Digital Core provides an extensive set of mixing and digital signal processing (DSP) features. The Digital Core Architecture is illustrated in Figure 12, which also identifies the datasheet sections applicable to each portion of the Digital Core.

The digital audio interfaces AIF1 and AIF2 each support one stereo pair of input and output signal paths through the WM8915 DSP functions. (Note that AIF1 supports a total of three stereo pairs of signal paths, providing additional capability for audio paths between the two audio interfaces.) The mixer configuration for the DSP output signal paths is described in “DSP Output Signal Mixing”.

A digital mixing path from the ADCs or Digital Microphones to the DAC output paths provides a high quality sidetone for voice calls or other applications. The sidetone configuration is described in “Digital Sidetone Mixing”; the associated filter and volume control is described in “Digital Sidetone Volume and Filter Control”.

Each of the four hi-fi DACs has a dedicated mixer for controlling the signal paths to that DAC. The configuration of these signal paths is described in “DAC Output Digital Mixing”.

Each DAC output signal path is provided with digital volume control, soft mute / un-mute and a low pass filter. The associated controls are defined in the “Output Signal Path” section.

Digital signal processing can be applied to the input and output signal paths. The available features include 5-band equalization (EQ), 3D stereo expansion and dynamic range control (DRC).

The EQ provides the capability to tailor the audio path according to the frequency characteristics of an earpiece or loudspeaker, and/or according to user preferences. The EQ controls are described in “ReTuneTM Mobile Parametric Equalizer (EQ)”. The DRC provides adaptive signal level control to improve the handling of unpredictable signal levels and to improve intelligibility in the presence of transients and impulsive noises. The DRC controls are described in “Dynamic Range Control (DRC)”. 3D stereo expansion provides a stereo enhancement effect; the depth of the effect is programmable, as described in “3D Stereo Expansion”.

The input signal paths are also equipped with digital volume control, soft mute / un-mute and mono mix functions; see “Digital Volume and Filter Control” for details of these features.

The output signal paths are equipped with digital volume control, programmable high-pass filter (HPF) and a notch filter. The Dynamic Range Control (DRC) circuit can also be applied here, with the restriction that a DRC cannot be enabled in the input and output path of one AIF channel at the same time. The AIF output volume and filter controls are described in “Digital Volume and Filter Control”.

The WM8915 provides two full audio interfaces, AIF1 and AIF2. Each interface supports a number of protocols, including I^2S, DSP and Left-Justified formats, and can operate in master or slave modes. Each interface is independently configurable on the respective transmit and receive paths. Time division multiplexing (TDM) is supported on both interfaces to allow multiple devices to stream data simultaneously on the same bus, saving space and power.

Up to six digital input / output channels can be supported simultaneously via the TDM channels on digital audio interface 1 (AIF1). It is also possible to support different sample rates simultaneously on any of the input or output paths of AIF1.

Signal mixing between audio interfaces is possible. The WM8915 performs stereo full-duplex sample rate conversion between the audio interfaces as required.

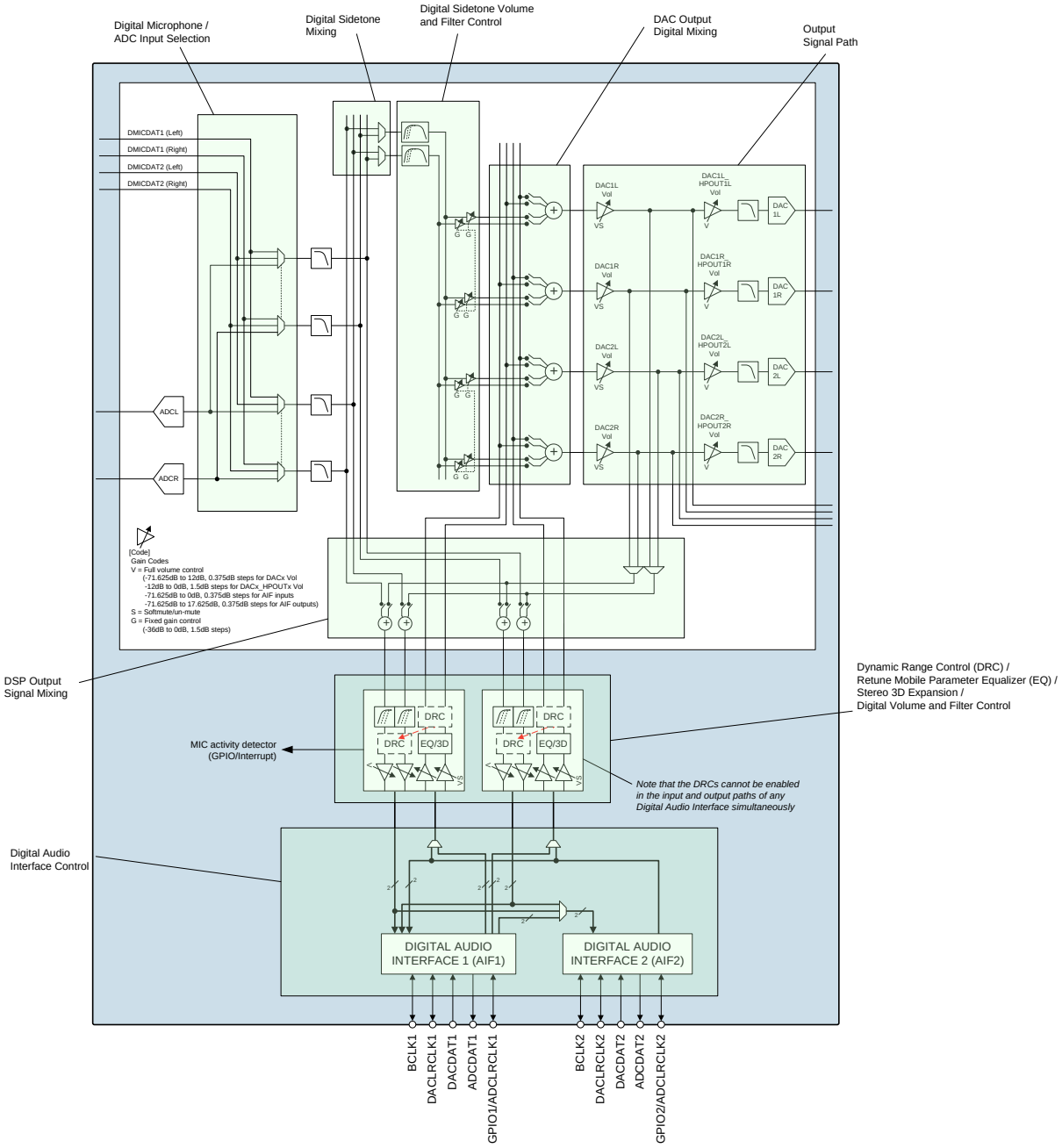


Figure 12 Digital Core Architecture

DIGITAL MIXING

This section describes the digital mixing functions of the WM8915.

Digital audio mixing is provided on the Digital microphone / ADC input paths, DSP1 / DSP2 output paths, digital sidetone paths, and on the inputs to four Digital to Analogue converters (DACs).

The digital mixing functions and associated control registers are illustrated in Figure 13. Details of the output signal path volume controls are provided in the “Output Signal Path” section.

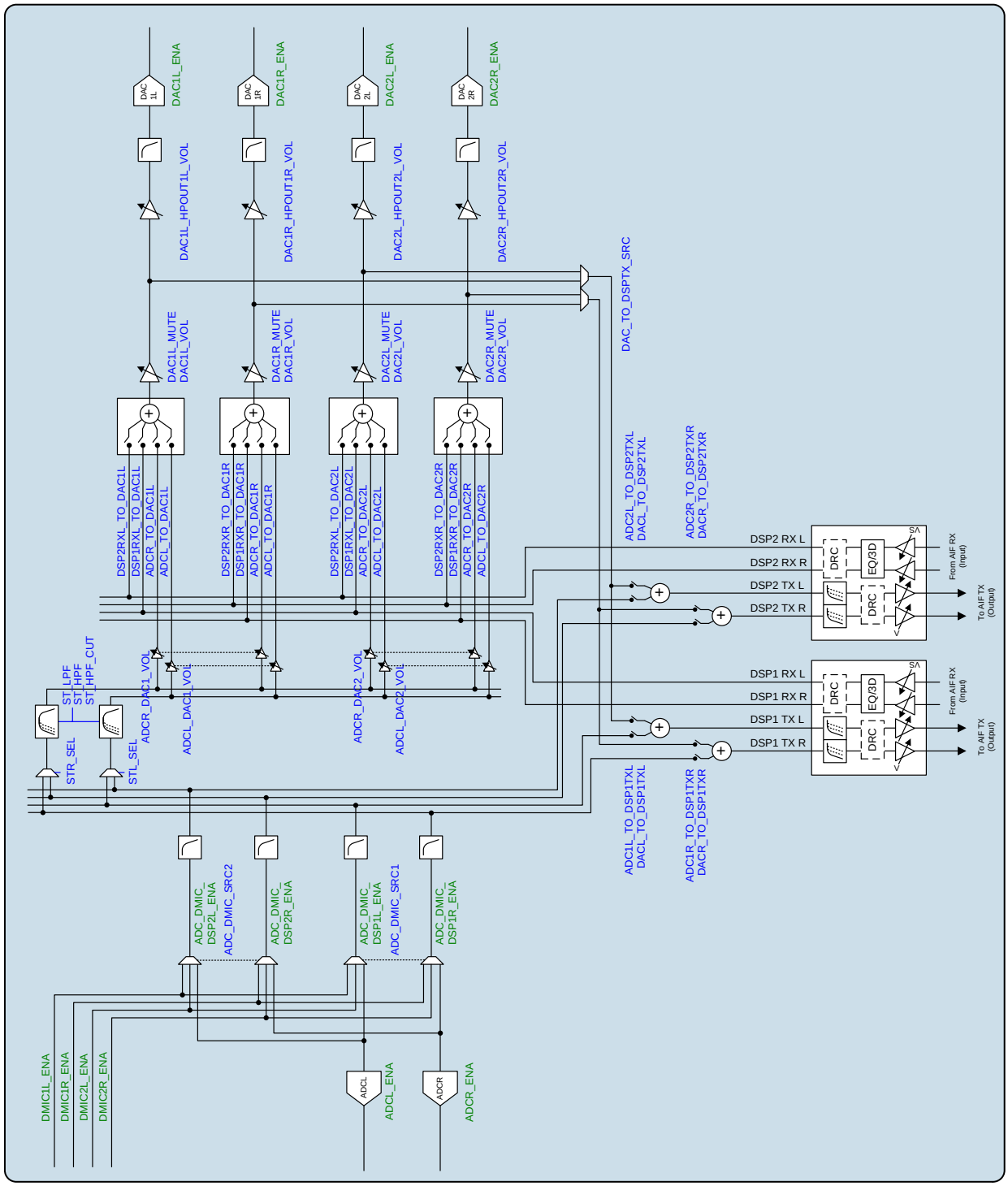


Figure 13 Digital Mixing Block Diagram

DIGITAL MICROPHONE / ADC INPUT SELECTION

The digital microphone inputs and the ADC outputs are routed to the DSP1 and DSP2 output (TX) paths via multiplexers.

The source for input paths 1L and 1R is selected using ADC_DMIC_SRC1. The available inputs are ADC, DMICDAT1 or DMICDAT2. The left and right channels are selected together using a single register. The left and right channels can be enabled independently using the register bits described in Table 11.

The source for input paths 2L and 2R is selected using ADC_DMIC_SRC2. The available inputs are ADC, DMICDAT1 or DMICDAT2. The left and right channels are selected together using a single register. The left and right channels can be enabled independently using the register bits described in Table 11.

A digital low pass filter is provided in each of these signal paths.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (0007h) Power Management (7)	7	ADC_DMIC_DSP2R_ENA	0	Input path 2R enable 0 = Disabled 1 = Enabled
	6	ADC_DMIC_DSP2L_ENA	0	Input path 2L enable 0 = Disabled 1 = Enabled
	5:4	ADC_DMIC_SRC2	01	Input path 2L and 2R select 00 = ADC 01 = DMICDAT1 10 = DMICDAT2 11 = Reserved
	3	ADC_DMIC_DSP1R_ENA	0	Input path 1R enable 0 = Disabled 1 = Enabled
	2	ADC_DMIC_DSP1L_ENA	0	Input path 1L enable 0 = Disabled 1 = Enabled
	1:0	ADC_DMIC_SRC1	00	Input path 1L and 1R select 00 = ADC 01 = DMICDAT1 10 = DMICDAT2 11 = Reserved

Table 10 Digital Microphone / ADC Input Selection

DSP OUTPUT SIGNAL MIXING

There are two digital mixers associated with the DSP1 output (TX) paths, and two digital mixers associated with the DSP2 output (TX) paths. The inputs to each mixer comprise the input signal paths IL, IR, 2L and 2R (from the ADCs and Digital Microphone inputs) and signals from the DAC output paths.

The signal source for input signal paths 1L and 1R are set by ADC_DMIC_SRC1. The source for input signal paths 2L and 2R are set by ADC_DMIC_SRC2. These registers are described in Table 11.

The DAC input source for all of the DSP mixers is selected by DAC_TO_DSPTX_SRC.

The DSP output mixers provide input to the DSP1 and DSP2 output (TX) paths, which form part of the signal paths to the digital audio interfaces AIF1 and AIF2. The DSP output paths are described in the “Dynamic Range Control (DRC)” and “Digital Volume and Filter Control” sections.

The DSP output mixer controls are defined in Table 11.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1542 (0606h) DSP1TX Left Mixer Routing	1	ADC1L_TO_DSP1TXL	0	Enable Input path 1L to DSP1 TX (Left) output 0 = Disabled 1 = Enabled Note that the ADC / DMIC input source is set by ADC_DMIC_SRC1.
	0	DACL_TO_DSP1TXL	0	Enable DAC path (Left) to DSP1 TX (Left) output 0 = Disabled 1 = Enabled Note that the DAC input source is set by DAC_TO_DSPTX_SRC.
R1543 (0607h) DSP1TX Right Mixer Routing	1	ADC1R_TO_DSP1TXR	0	Enable Input path 1R to DSP1 TX (Right) output 0 = Disabled 1 = Enabled Note that the ADC / DMIC input source is set by ADC_DMIC_SRC1.
	0	DACR_TO_DSP1TXR	0	Enable DAC path (Right) to DSP1 TX (Right) output 0 = Disabled 1 = Enabled Note that the DAC input source is set by DAC_TO_DSPTX_SRC.
R1544 (0608h) DSP2TX Left Mixer Routing	1	ADC2L_TO_DSP2TXL	0	Enable Input path 2L to DSP2 TX (Left) output 0 = Disabled 1 = Enabled Note that the ADC / DMIC input source is set by ADC_DMIC_SRC2.
	0	DACL_TO_DSP2TXL	0	Enable DAC path (Left) to DSP2 TX (Left) output 0 = Disabled 1 = Enabled Note that the DAC input source is set by DAC_TO_DSPTX_SRC.
R1545 (0609h) DSP2TX Right Mixer Routing	1	ADC2R_TO_DSP2TXR	0	Enable Input path 2R to DSP2 TX (Right) output 0 = Disabled 1 = Enabled Note that the ADC / DMIC input source is set by ADC_DMIC_SRC2.
	0	DACR_TO_DSP2TXR	0	Enable DAC path (Right) to DSP2 TX (Right) output 0 = Disabled 1 = Enabled Note that the DAC input source is set by DAC_TO_DSPTX_SRC.
R1546 (060Ah) DSP TX Mixer Select	0	DAC_TO_DSPTX_SRC	0	DAC path select for DSP TX output 0 = DACL1 and DACR1 1 = DACL2 and DACR2

Table 11 DSP Output Signal Mixing

DIGITAL SIDETONE MIXING

There are two digital sidetone signal paths, STL and STR. The sidetone sources are selectable for each path. The sidetone mixer outputs are inputs to the DAC signal mixers.

The following sources can be selected for sidetone path STL.

- Input path 1L (Left channel ADC, DMICDAT1 or DMICDAT2, selected by ADC_DMIC_SRC1)
- Input path 2L (Left channel ADC, DMICDAT1 or DMICDAT2, selected by ADC_DMIC_SRC2)

The following sources can be selected for sidetone path STR.

- Input path 1R (Right channel ADC, DMICDAT1 or DMICDAT2, selected by ADC_DMIC_SRC1)
- Input path 2R (Right channel ADC, DMICDAT1 or DMICDAT2, selected by ADC_DMIC_SRC2)

The sidetone signal sources are selected using STR_SEL and STL_SEL as described in Table 12.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1569 (0621h) Sidetone	1	STR_SEL	0	Select source for sidetone STR path 0 = Input path 1R (set by ADC_DMIC_SRC1) 1 = Input path 2R (set by ADC_DMIC_SRC2)
	0	STL_SEL	0	Select source for sidetone STL path 0 = Input path 1L (set by ADC_DMIC_SRC1) 1 = Input path 2L (set by ADC_DMIC_SRC2)

Table 12 Digital Sidetone Mixing

DIGITAL SIDETONE VOLUME AND FILTER CONTROL

A digital volume control is provided for the digital sidetone paths. The associated register controls are described in Table 13.

A digital high-pass filter can be enabled in the sidetone paths to remove DC offsets. This filter is enabled using the ST_HPF register bit; the cut-off frequency is configured using ST_HPF_CUT. When the filter is enabled, it is enabled in both digital sidetone paths.

A first-order digital low-pass filter is enabled by default in the sidetone paths. This filter is controlled using the ST_LPF register bit; the cut-off frequency is 3.3kHz (assuming SYSCLK frequency of 12.288MHz).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1536 (0600h) DAC1 Mixer Volumes	9:5	ADCR_DAC1_VOL [4:0]	00000	Sidetone STR to DAC1L and DAC1R Volume 00000 = -36dB 00001 = -34.5dB 00010 = -33dB …. (1.5dB steps) 10111 = -1.5dB 11000 = 0dB (see Table 14 for gain range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4:0	ADCL_DAC1_VOL [4:0]	00000	Sidetone STL to DAC1L and DAC1R Volume 00000 = -36dB 00001 = -34.5dB 00010 = -33dB …. (1.5dB steps) 10111 = -1.5dB 11000 = 0dB (see Table 14 for gain range)
R1539 (0603h) DAC2 Mixer Volumes	9:5	ADCR_DAC2_VOL [4:0]	00000	Sidetone STR to DAC2L and DAC2R Volume 00000 = -36dB 00001 = -34.5dB 00010 = -33dB …. (1.5dB steps) 10111 = -1.5dB 11000 = 0dB (see Table 14 for gain range)
	4:0	ADCL_DAC2_VOL [4:0]	00000	Sidetone STL to DAC2L and DAC2R Volume 00000 = -36dB 00001 = -34.5dB 00010 = -33dB …. (1.5dB steps) 10111 = -1.5dB 11000 = 0dB (see Table 14 for gain range)
R1569 (0621h) Sidetone	12	ST_LPF	1	Digital Sidetone LPF Select (Cut-off frequency is 3.3kHz) 0 = Disabled 1 = Enabled
	9:7	ST_HPF_CUT [2:0]	000	Sidetone HPF cut-off frequency 000 = 2.9kHz 001 = 1.5kHz 010 = 735Hz 011 = 403Hz 100 = 196Hz 101 = 98Hz 110 = 49Hz 111 = Reserved
	6	ST_HPF	0	Digital Sidetone HPF Select 0 = Disabled 1 = Enabled

Table 13 Digital Sidetone Volume Control

ADCR_DAC1_VOL, ADCL_DAC2_VOL, ADCR_DAC1_VOL or ADCL_DAC2_VOL	SIDETONE GAIN (dB)	ADCR_DAC1_VOL, ADCL_DAC2_VOL, ADCR_DAC1_VOL or ADCL_DAC2_VOL	SIDETONE GAIN (dB)
00000	-36	10000	-12
00001	-34.5	10001	-10.5
00010	-33	10010	-9
00011	-31.5	10011	-7.5
00100	-30	10100	-6
00101	-28.5	10101	-4.5
00110	-27	10110	-3
00111	-25.5	10111	-1.5
01000	-24	11000	0
01001	-22.5	11001	0
01010	-21	11010	0
01011	-19.5	11011	0
01100	-18	11100	0
01101	-16.5	11101	0
01110	-15	11110	0
01111	-13.5	11111	0

Table 14 Digital Sidetone Volume Range

DAC OUTPUT DIGITAL MIXING

There are four DAC output mixers, one for each DAC. The inputs to each DAC mixer comprise the digital sidetone paths (STL and STR) and the receive (RX) path signals from DSP1 and DSP2.

The DAC output mixers provide input to the DACs, which form part of the signal paths to the analogue headphone outputs and the SPDM digital audio outputs.

The DAC output mixer controls are defined in Table 15.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1537 (0601h) DAC1 Left Mixer Routing	5	ADCR_TO_DAC 1L	0	Enable Sidetone STR to DAC1L 0 = Disabled 1 = Enabled
	4	ADCL_TO_DAC 1L	0	Enable Sidetone STL to DAC1L 0 = Disabled 1 = Enabled
	1	DSP2RXL_TO_ DAC1L	0	Enable DSP2 RX (Left) input to DAC1L 0 = Disabled 1 = Enabled
	0	DSP1RXL_TO_ DAC1L	0	Enable DSP1 RX (Left) input to DAC1L 0 = Disabled 1 = Enabled
R1538 (0602h) DAC1 Right Mixer Routing	5	ADCR_TO_DAC 1R	0	Enable Sidetone STR to DAC1R 0 = Disabled 1 = Enabled
	4	ADCL_TO_DAC 1R	0	Enable Sidetone STL to DAC1R 0 = Disabled 1 = Enabled
	1	DSP2RXR_TO_ DAC1R	0	Enable DSP2 RX (Right) input to DAC1R 0 = Disabled 1 = Enabled
	0	DSP1RXR_TO_	0	Enable DSP1 RX (Right) input to

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
		DAC1R		DAC1R 0 = Disabled 1 = Enabled
R1540 (0604h) DAC2 Left Mixer Routing	5	ADCR_TO_DAC 2L	0	Enable Sidetone STR to DAC2L 0 = Disabled 1 = Enabled
	4	ADCL_TO_DAC 2L	0	Enable Sidetone STL to DAC2L 0 = Disabled 1 = Enabled
	1	DSP2RXL_TO_ DAC2L	0	Enable DSP2 RX (Left) input to DAC2L 0 = Disabled 1 = Enabled
	0	DSP1RXL_TO_ DAC2L	0	Enable DSP1 RX (Left) input to DAC2L 0 = Disabled 1 = Enabled
R1541 (0605h) DAC2 Right Mixer Routing	5	ADCR_TO_DAC 2R	0	Enable Sidetone STR to DAC2R 0 = Disabled 1 = Enabled
	4	ADCL_TO_DAC 2R	0	Enable Sidetone STL to DAC2R 0 = Disabled 1 = Enabled
	1	DSP2RXR_TO_ DAC2R	0	Enable DSP2 RX (Right) input to DAC2R 0 = Disabled 1 = Enabled
	0	DSP1RXR_TO_ DAC2R	0	Enable DSP1 RX (Right) input to DAC2R 0 = Disabled 1 = Enabled

Table 15 DAC Output Digital Mixing

DYNAMIC RANGE CONTROL (DRC)

The Dynamic Range Control (DRC) is a circuit which can be enabled in the digital playback or digital record paths of the WM8915. The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range, e.g. when recording from microphones built into a handheld system. The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates 'anti-clip' and 'quick release' features for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates 'anti-clip' and 'quick release' features for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

The DRC also incorporates a Noise Gate function, which provides additional attenuation of very low-level input signals. This means that the signal path is quiet when no signal is present, giving an improvement in background noise level under these conditions.

The WM8915 provides two stereo Dynamic Range Controllers (DRCs); one is associated with the DSP1 signal paths, the other is assocated with the DSP2 signal paths. Each DRC can be enabled either in the digital playback (DSP RX/input) path or in the digital record (DSP TX/output) path, as described in the "Digital Core Architecture" section.

The DRCs are enabled in the TX or RX audio signal paths using the register bits described in Table 16. Note that enabling any DRC in the TX and RX paths simultaneously is an invalid selection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1088 (0440h) DSP1 DRC (1)	2	DSP1RX_DRC_ENA	0	Enable DRC in DSP1 RX input path 0 = Disabled 1 = Enabled
	1	DSP1TXL_DRC_ENA	0	Enable DRC in DSP1 TX (Left) output path 0 = Disabled 1 = Enabled
	0	DSP1TXR_DRC_ENA	0	Enable DRC in DSP1 TX (Right) output path 0 = Disabled 1 = Enabled
R1344 (0550h) DSP2 DRC (1)	2	DSP2RX_DRC_ENA	0	Enable DRC in DSP2 RX input path 0 = Disabled 1 = Enabled
	1	DSP2TXL_DRC_ENA	0	Enable DRC in DSP2 TX (Left) output path 0 = Disabled 1 = Enabled
	0	DSP2TXR_DRC_ENA	0	Enable DRC in DSP2 TX (Right) output path 0 = Disabled 1 = Enabled

Table 16 DRC Enable

The following description of the DRC is applicable to both DSP paths. The DRC register control fields are referred to DSP*n*, where *n* = 1 or 2 according to the applicable DSP path.

The DRC register control fields are described in Table 18 and Table 19 for the DSP1 and DSP2 DRCs respectively.

DRC COMPRESSION / EXPANSION / LIMITING

The DRC supports two different compression regions, separated by a “Knee” at a specific input amplitude. In the region above the knee, the compression slope DSP*n*DRC_HI_COMP applies; in the region below the knee, the compression slope DSP*n*DRC_LO_COMP applies.

The DRC also supports a noise gate region, where low-level input signals are heavily attenuated. This function can be enabled or disabled according to the application requirements. The DRC response in this region is defined by the expansion slope DSP*n*DRC_NG_EXP.

For additional attenuation of signals in the noise gate region, an additional “knee” can be defined (shown as “Knee2” in Figure 14). When this knee is enabled, this introduces an infinitely steep drop-off in the DRC response pattern between the DSP*n*DRC_LO_COMP and DSP*n*DRC_NG_EXP regions.

The overall DRC compression characteristic in “steady state” (i.e. where the input amplitude is near-constant) is illustrated in Figure 14.

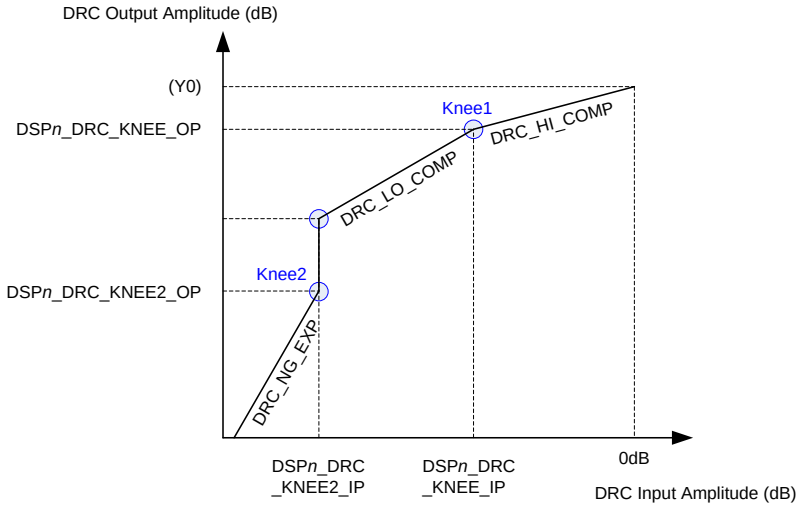


Figure 14 DRC Response Characteristic

The slope of the DRC response is determined by register fields DSP*n*DRC_HI_COMP and DSP*n*DRC_LO_COMP. A slope of 1 indicates constant gain in this region. A slope less than 1 represents compression (i.e. a change in input amplitude produces only a smaller change in output amplitude). A slope of 0 indicates that the target output amplitude is the same across a range of input amplitudes; this is infinite compression.

When the noise gate is enabled, the DRC response in this region is determined by the DSP*n*DRC_NG_EXP register. A slope of 1 indicates constant gain in this region. A slope greater than 1 represents expansion (ie. a change in input amplitude produces a larger change in output amplitude).

When the DRC_KNEE2_OP knee is enabled (“Knee2” in Figure 14), this introduces the vertical line in the response pattern illustrated, resulting in infinitely steep attenuation at this point in the response.

The DRC parameters are listed in Table 17.

REF	PARAMETER	DESCRIPTION
1	DSP*n*DRC_KNEE_IP	Input level at Knee1 (dB)
2	DSP*n*DRC_KNEE_OP	Output level at Knee2 (dB)
3	DSP*n*DRC_HI_COMP	Compression ratio above Knee1
4	DSP*n*DRC_LO_COMP	Compression ratio below Knee1
5	DSP*n*DRC_KNEE2_IP	Input level at Knee2 (dB)
6	DSP*n*DRC_NG_EXP	Expansion ratio below Knee2
7	DSP*n*DRC_KNEE2_OP	Output level at Knee2 (dB)

Table 17 DRC Response Parameters

The noise gate is enabled when the DSP*n*DRC_NG_ENA register is set. When the noise gate is not enabled, parameters 5, 6, 7 above are ignored, and the DSP*n*DRC_LO_COMP slope applies to all input signal levels below Knee1.

The DRC_KNEE2_OP knee is enabled when the DSP*n*DRC_KNEE2_OP_ENA register is set. When this bit is not set, then parameter 7 above is ignored, and the Knee2 position always coincides with the low end of the DSP*n*DRC_LO_COMP region.

The “Knee1” point in Figure 14 is determined by register fields DSPnDRC_KNEE_IP and DSPnDRC_KNEE_OP.

Parameter Y0, the output level for a 0dB input, is not specified directly, but can be calculated from the other parameters, using the equation:

$$Y0 = DSPnDRC\_KNEE\_OP - (DSPnDRC\_KNEE\_IP \times DSPnDRC\_HI\_COMP)$$

GAIN LIMITS

The minimum and maximum gain applied by the DRC is set by register fields DSP*n*DRC_MINGAIN, DSP*n*DRC_MAXGAIN and DSP*n*DRC_NG_MINGAIN. These limits can be used to alter the DRC response from that illustrated in Figure 14. If the range between maximum and minimum gain is reduced, then the extent of the dynamic range control is reduced.

The minimum gain in the Compression regions of the DRC response is set by DSP*n*DRC_MINGAIN. The mimimum gain in the Noise Gate region is set by DSP*n*DRC_NG_MINGAIN. The minimum gain limit prevents excessive attenuation of the signal path.

The maximum gain limit set by DSP*n*DRC_MAXGAIN prevents quiet signals (or silence) from being excessively amplified.

DYNAMIC CHARACTERISTICS

The dynamic behaviour determines how quickly the DRC responds to changing signal levels. Note that the DRC responds to the average (RMS) signal amplitude over a period of time.

The DSP*n*DRC_ATK determines how quickly the DRC gain decreases when the signal amplitude is high. The DSP*n*DRC_DCY determines how quickly the DRC gain increases when the signal amplitude is low.

These register fields are described in Table 18 and Table 19. Note that the register defaults are suitable for general purpose microphone use.

ANTI-CLIP CONTROL

The DRC includes an Anti-Clip feature to avoid signal clipping when the input amplitude rises very quickly. This feature uses a feed-forward technique for early detection of a rising signal level. Signal clipping is avoided by dynamically increasing the gain attack rate when required. The Anti-Clip feature is enabled using the DSP*n*DRC_ANTICLIP bit.

Note that the feed-forward processing increases the latency in the input signal path.

Note that the Anti-Clip feature operates entirely in the digital domain. It cannot be used to prevent signal clipping in the analogue domain nor in the source signal. Analogue clipping can only be prevented by reducing the analogue signal gain or by adjusting the source signal.

Note that the Anti-Clip feature should not be enabled at the same time as the Quick Release feature (described below) on the same DRC.

QUICK RELEASE CONTROL

The DRC includes a Quick-Release feature to handle short transient peaks that are not related to the intended source signal. For example, in handheld microphone recording, transient signal peaks sometimes occur due to user handling, key presses or accidental tapping against the microphone. The Quick Release feature ensures that these transients do not cause the intended signal to be masked by the longer time constants of DSP*n*DRC_DCY.

The Quick-Release feature is enabled by setting the DSP*n*DRC_QR bit. When this bit is enabled, the DRC measures the crest factor (peak to RMS ratio) of the input signal. A high crest factor is indicative of a transient peak that may not be related to the intended source signal. If the crest factor exceeds the level set by DSP*n*DRC_QR_THR, then the normal decay rate (DSP*n*DRC_DCY) is ignored and a faster decay rate (DSP*n*DRC_QR_DCY) is used instead.

Note that the Quick Release feature should not be enabled at the same time as the Anti-Clip feature (described above) on the same DRC.

SIGNAL ACTIVITY DETECT

The DRC incorporates a configurable signal detect function, allowing the signal level at the DRC input to be monitored and to be used to trigger other events. This can be used to detect the presence of a microphone signal on an ADC or digital mic channel, or can be used to detect an audio signal received over the digital audio interface.

The Peak signal level or the RMS signal level of the DRC input can be selected as the detection threshold. When the threshold condition is exceeded, an interrupt or GPIO output can be generated. See “General Purpose Input/Output” for a full description of the applicable control fields.

DRC REGISTER CONTROLS

The DSP1 DRC control registers are described in Table 18. The DSP2 DRC control registers are described in Table 19.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1088 (0440h) DSP1 DRC (1)	8	DSP1DRC_NG_ENA	0	DSP1 DRC Noise Gate Enable 0 = Disabled 1 = Enabled
	5	DSP1DRC_KNEE2_OP_ENA	0	DSP1 DRC KNEE2_OP Enable 0 = Disabled 1 = Enabled
	4	DSP1DRC_QR	1	DSP1 DRC Quick-release Enable 0 = Disabled 1 = Enabled
	3	DSP1DRC_ANTICLIP	1	DSP1 DRC Anti-clip Enable 0 = Disabled 1 = Enabled
R1089 (0441h) DSP1 DRC (2)	12:9	DSP1DRC_ATK [3:0]	0100	DSP1 DRC Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved
	8:5	DSP1DRC_DCY [3:0]	0010	DSP1 DRC Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved
	4:2	DSP1DRC_MINGAIN [2:0]	001	DSP1 DRC Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	DSP1DRC_MAX GAIN [1:0]	01	DSP1 DRC Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB
R1090 (0442h) DSP1 DRC (3)	15:12	DSP1DRC_NG_ MINGAIN [3:0]	0000	DSP1 DRC Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	11:10	DSP1DRC_NG_ EXP [1:0]	00	DSP1 DRC Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	9:8	DSP1DRC_QR_ THR [1:0]	00	DSP1 DRC Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7:6	DSP1DRC_QR_ DCY [1:0]	00	DSP1 DRC Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = Reserved
	5:3	DSP1DRC_HI_C OMP [2:0]	000	DSP1 DRC Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:0	DSP1DRC_LO_COMP [2:0]	000	DSP1 DRC Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved
R1092 (0443h) DSP1 DRC (4)	10:5	DSP1DRC_KNEE_IP [5:0]	000000	DSP1 DRC Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
	4:0	DSP1DRC_KNEE_OP [4:0]	00000	DSP1 DRC Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R1093 (0444h) DSP1 DRC (5)	9:5	DSP1DRC_KNEE2_IP [4:0]	00000	DSP1 DRC Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DSP1DRC_NG_ENA = 1.
	4:0	DSP1DRC_KNEE2_OP [4:0]	00000	DSP1 DRC Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DSP1DRC_KNEE2_OP_ENA = 1.

Table 18 DSP1 Dyanamic Range Control (DRC) Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1344 (0540h) DSP2 DRC (1)	8	DSP2DRC_NG_ENA	0	DSP2 DRC Noise Gate Enable 0 = Disabled 1 = Enabled
	5	DSP2DRC_KNEE2_OP_ENA	0	DSP2 DRC KNEE2_OP Enable 0 = Disabled 1 = Enabled
	4	DSP2DRC_QR	1	DSP2 DRC Quick-release Enable 0 = Disabled 1 = Enabled
	3	DSP2DRC_ANTICLIP	1	DSP2 DRC Anti-clip Enable 0 = Disabled 1 = Enabled
R1345 (0541h) DSP2 DRC (2)	12:9	DSP2DRC_ATK [3:0]	0100	DSP2 DRC Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved
	8:5	DSP2DRC_DCY [3:0]	0010	DSP2 DRC Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved
	4:2	DSP2DRC_MINGAIN [2:0]	001	DSP2 DRC Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	DSP2DRC_MAX GAIN [1:0]	01	DSP2 DRC Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB
R1346 (0542h) DSP2 DRC (3)	15:12	DSP2DRC_NG_ MINGAIN [3:0]	0000	DSP2 DRC Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	11:10	DSP2DRC_NG_ EXP [1:0]	00	DSP2 DRC Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	9:8	DSP2DRC_QR_ THR [1:0]	00	DSP2 DRC Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7:6	DSP2DRC_QR_ DCY [1:0]	00	DSP2 DRC Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = Reserved
	5:3	DSP2DRC_HI_C OMP [2:0]	000	DSP2 DRC Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:0	DSP2DRC_LO_COMP [2:0]	000	DSP2 DRC Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved
R1347 (0543h) DSP2 DRC (4)	10:5	DSP2DRC_KNEE_IP [5:0]	000000	DSP2 DRC Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
	4:0	DSP2DRC_KNEE_OP [4:0]	00000	DSP2 DRC Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R1348 (0544h) DSP2 DRC (5)	9:5	DSP2DRC_KNEE2_IP [4:0]	00000	DSP2 DRC Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DSP2DRC_NG_ENA = 1.
	4:0	DSP2DRC_KNEE2_OP [4:0]	00000	DSP2 DRC Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DSP2DRC_KNEE2_OP_ENA = 1.

Table 19 DSP2 Dynamic Range Control (DRC) Registers

RETUNE™ MOBILE PARAMETRIC EQUALIZER (EQ)

The ReTune™ Mobile Parametric EQ is a circuit which can be enabled in the digital playback paths of the WM8915. The function of the EQ is to adjust the frequency characteristic of the output in order to compensate for unwanted frequency characteristics in the loudspeaker (or other output transducer). It can also be used to tailor the response according to user preferences, for example to accentuate or attenuate specific frequency bands to emulate different sound profiles or environments e.g. concert hall, rock etc.

The WM8915 provides two stereo EQ circuits; one is associated with the DSP1 RX/input path, the other is associated with the DSP2 RX/input path. The EQ is enabled in these signal paths using the register bits described in Table 20.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1152 (0480h) DSP1 RX EQ Gains (1)	0	DSP1RX_EQ_ENA	0	Enable EQ in DSP1 RX input path 0 = Disabled 1 = Enabled
R1408 (0580h) DSP2 RX EQ Gains (1)	0	DSP2RX_EQ_ENA	0	Enable EQ in DSP2 RX input path 0 = Disabled 1 = Enabled

Table 20 ReTune™ Mobile Parametric EQ Enable

The following description of the EQ is applicable to both DSP paths. The EQ register control fields are described in Table 22 and Table 23 for the DSP1 and DSP2 EQs respectively.

The EQ can be configured to operate in two modes - "Default" mode or "ReTune™ Mobile" mode.

DEFAULT MODE (5-BAND PARAMETRIC EQ)

In default mode, the cut-off / centre frequencies are fixed as per Table 21. The filter bandwidths are also fixed in default mode. The gain of the individual bands (-12dB to +12dB) can be controlled as described in Table 22.

The cut-off / centre frequencies noted in Table 21 are applicable to a sample rate of 48kHz. These frequencies will be scaled when using other sample rates for either of the DSP signal paths.

The audio sample rates for the DSP1 and DSP2 signal paths are set by DSP1_DIV and DSP2_DIV respectively. The supported sample rates are 48kHz, 32kHz, 16kHz and 8kHz (assuming a SYSCLK frequency of 12.288MHz). See "Clocking and Sample Rates" for further details.

If DSP1 and DSP2 are operating at different sample rates, then the cut-off / centre frequencies will be different for the two paths. Note that the frequencies can be set to other values by using the features described in "ReTuneTM Mobile Mode".

EQ BAND	CUT-OFF/CENTRE FREQUENCY
1	100 Hz
2	300 Hz
3	875 Hz
4	2400 Hz
5	6900 Hz

Table 21 EQ Band Cut-off / Centre Frequencies

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1152 (0480h) DSP1 RX EQ Gains (1)	15:11	DSP1RX_EQ_B1_GAIN [4:0]	01100 (0dB)	DSP1 EQ Band 1 Gain -12dB to +12dB in 1dB steps (see Table 24 for gain range)
	10:6	DSP1RX_EQ_B2_GAIN [4:0]	01100 (0dB)	DSP1 EQ Band 2 Gain -12dB to +12dB in 1dB steps (see Table 24 for gain range)
	5:1	DSP1RX_EQ_B3_GAIN [4:0]	01100 (0dB)	DSP1 EQ Band 3 Gain -12dB to +12dB in 1dB steps (see Table 24 for gain range)
R1153 (0481h) DSP1 RX EQ Gains (2)	15:11	DSP1RX_EQ_B4_GAIN [4:0]	01100 (0dB)	DSP1 EQ Band 4 Gain -12dB to +12dB in 1dB steps (see Table 24 for gain range)
	10:6	DSP1RX_EQ_B5_GAIN [4:0]	01100 (0dB)	DSP1 EQ Band 5 Gain -12dB to +12dB in 1dB steps (see Table 24 for gain range)

Table 22 DSP1 EQ Control Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1408 (0580h) DSP2 RX EQ Gains (1)	15:11	DSP2RX_EQ_B1_GAIN [4:0]	01100 (0dB)	DSP2 EQ Band 1 Gain -12dB to +12dB in 1dB steps (see Table 24 for gain range)
	10:6	DSP2RX_EQ_B2_GAIN [4:0]	01100 (0dB)	DSP2 EQ Band 2 Gain -12dB to +12dB in 1dB steps (see Table 24 for gain range)
	5:1	DSP2RX_EQ_B3_GAIN [4:0]	01100 (0dB)	DSP2 EQ Band 3 Gain -12dB to +12dB in 1dB steps (see Table 24 for gain range)
R1409 (0581h) DSP2 RX EQ Gains (2)	15:11	DSP2RX_EQ_B4_GAIN [4:0]	01100 (0dB)	DSP2 EQ Band 4 Gain -12dB to +12dB in 1dB steps (see Table 24 for gain range)
	10:6	DSP2RX_EQ_B5_GAIN [4:0]	01100 (0dB)	DSP2 EQ Band 5 Gain -12dB to +12dB in 1dB steps (see Table 24 for gain range)

Table 23 DSP2 EQ Control Registers

EQ GAIN SETTING	Gain (dB)
00000	-12
00001	-11
00010	-10
00011	-9
00100	-8
00101	-7
00110	-6
00111	-5
01000	-4
01001	-3
01010	-2
01011	-1
01100	0
01101	+1
01110	+2
01111	+3
10000	+4
10001	+5
10010	+6
10011	+7
10100	+8
10101	+9
10110	+10
10111	+11
11000	+12
11001 to 11111	Reserved

Table 24 EQ Gain Control Range

RETUNE™ MOBILE MODE

ReTune™ Mobile mode provides a comprehensive facility for the user to define the cut-off/centre frequencies and filter bandwidth for each EQ band, in addition to the gain controls already described. This enables the EQ to be accurately customised for a specific transducer characteristic or desired sound profile.

The EQ enable and EQ gain controls are the same as defined for the default mode. The additional coefficients used in ReTune™ Mobile mode are held in registers R1154 to R1171 for DSP1, and registers R1410 to R1427 for DSP2. These coefficients are derived using tools provided in Cirrus's WISCE™ evaluation board control software.

Please contact your local Cirrus representative for more details.

Note that the DSP1 and DSP2 signal paths can operate at different sample rates concurrently. The EQ settings for each interface must be programmed relative to the applicable sample rate of the corresponding audio interface path. If the audio interface sample rate is changed, then different EQ register settings will be required to achieve a given EQ response.

EQ FILTER CHARACTERISTICS

The filter characteristics for each frequency band are shown in Figure 15 to Figure 19. These figures show the frequency response for all available gain settings, using default cut-off/centre frequencies and bandwidth.

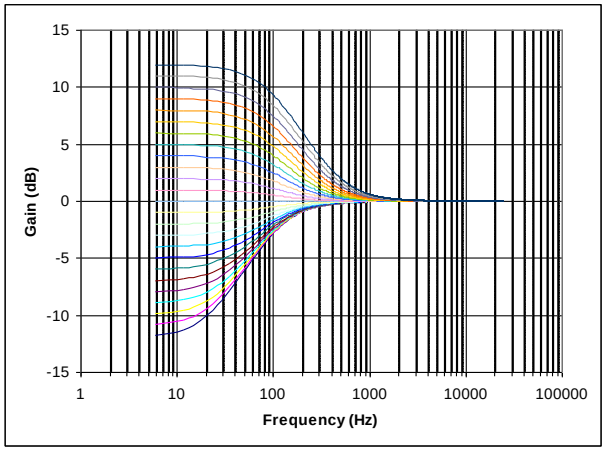


Figure 15 EQ Band 1 – Low Freq Shelf Filter Response

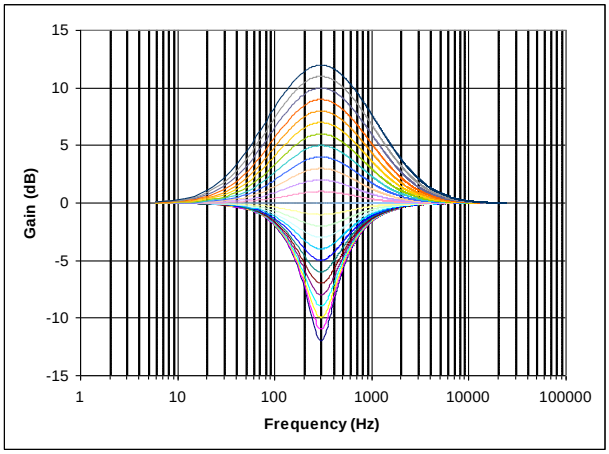


Figure 16 EQ Band 2 – Peak Filter Response

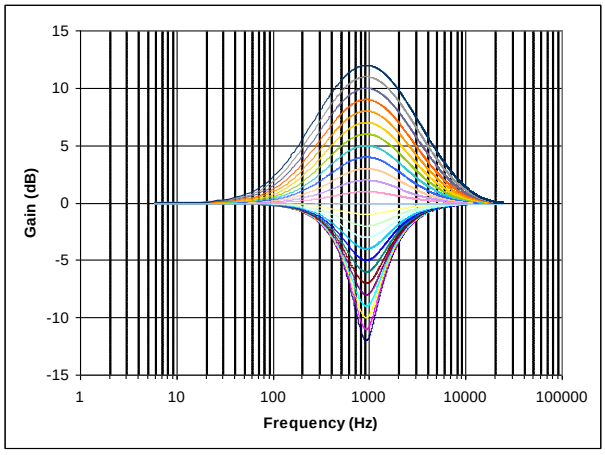


Figure 17 EQ Band 3 – Peak Filter Response

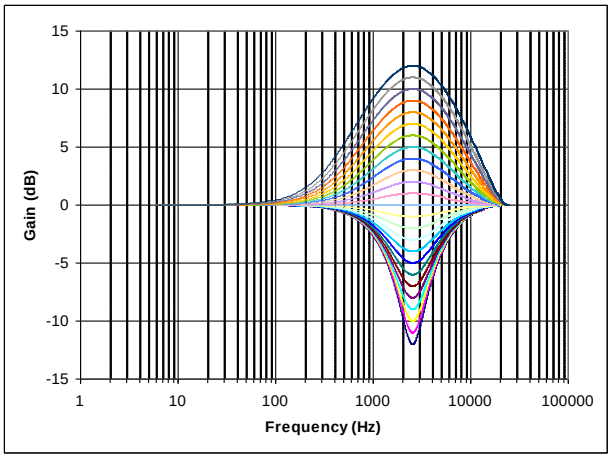


Figure 18 EQ Band 4 – Peak Filter Response

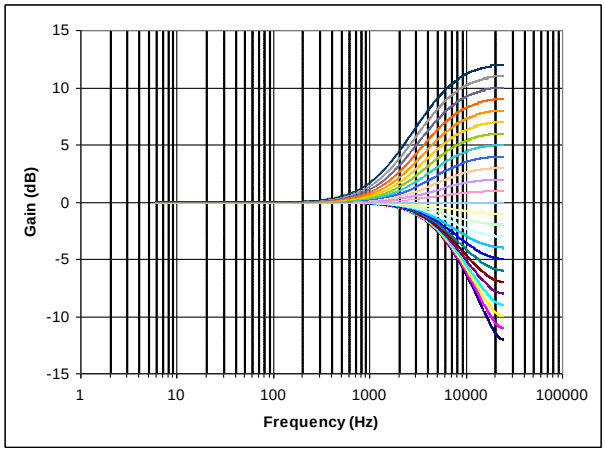


Figure 19 EQ Band 5 – High Freq Shelf Filter Response

3D STEREO EXPANSION

The 3D Stereo Expansion is an audio enhancement feature which can be enabled in the digital playback paths of the WM8915. This feature uses configurable cross-talk mechanisms to adjust the depth or width of the stereo audio.

The WM8915 provides two 3D Stereo Expansion circuits; one is associated with the DSP1 RX/input path, the other is associated with the DSP2 RX/input path. The 3D Stereo Expansion is enabled and controlled in these signal paths using the register bits described in Table 25.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1057 (0421h) DSP1 RX Filters (2)	13:9	DSP1RX_3D_GAIN	00000	DSP1 3D Stereo depth 00000 = Off 00001 = Minimum (-16dB) …(0.915dB steps) 11111 = Maximum (+11.5dB)
	8	DSP1RX_3D_ENA	0	Enable 3D Stereo in DSP1 RX input path 0 = Disabled 1 = Enabled
R1313 (0521h) DSP2 RX Filters (2)	13:9	DSP2RX_3D_GAIN	00000	DSP2 3D Stereo depth 00000 = Off 00001 = Minimum (-16dB) …(0.915dB steps) 11111 = Maximum (+11.5dB)
	8	DSPRX2_3D_ENA	0	Enable 3D Stereo in DSP2 RX input path 0 = Disabled 1 = Enabled

Table 25 3D Stereo Expansion Control

DIGITAL VOLUME AND FILTER CONTROL

This section describes the digital volume and filter controls of the WM8915 DSP paths.

There is a stereo output signal path associated with each of DSP1 and DSP2. These paths support digital output or record functions to the digital audio interfaces. Digital volume control and High Pass Filter (HPF) control is provided on the DSP TX/output paths. In 8kHz or 16kHz modes, an additional notch filter is provided.

There is a stereo input signal path associated with each of DSP1 and DSP2. These paths support digital playback functions from the digital audio interfaces. Digital volume control, soft-mute control, mono mix and de-emphasis filter control is provided on the DSP RX/input paths.

DSP OUTPUT (TX) VOLUME CONTROL

A digital volume control is provided on the DSP1 TX and DSP2 TX output signal paths, allowing attenuation in the range -71.625dB to +17.625dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 239$; MUTE for $X = 0$ +17.625dB for $239 \leq X \leq 255$

The DSP1TX_VU and DSP2TX_VU bits control the loading of digital volume control data. When the volume update bit is set to 0, the associated volume control data will be loaded into the respective control register, but will not actually change the digital gain setting.

The DSP1TXL and DSP1TXR gain settings are updated when a 1 is written to DSP1TX_VU. The DSP2TXL and DSP2TXR gain settings are updated when a 1 is written to DSP2TX_VU. This makes it possible to update the gain of left and right channels simultaneously in either of the DSP blocks.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1024 (0400h) DSP1 TX Left Volume	8	DSP1TX_VU	N/A	DSP1 TX output path Volume Update Writing a 1 to this bit will cause the DSP1TXL and DSP1TXR volume to be updated simultaneously
	7:0	DSP1TXL_VOL [7:0]	C0h (0dB)	DSP1 TX (Left) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB (See Table 27 for volume range)
R1025 (0401h) DSP1 TX Right Volume	8	DSP1TX_VU	N/A	DSP1 TX output path Volume Update Writing a 1 to this bit will cause the DSP1TXL and DSP1TXR volume to be updated simultaneously
	7:0	DSP1TXR_VOL [7:0]	C0h (0dB)	DSP1 TX (Right) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB (See Table 27 for volume range)
R1280 (0500h) DSP2 TX Left Volume	8	DSP2TX_VU	N/A	DSP2 TX output path Volume Update Writing a 1 to this bit will cause the DSP2TXL and DSP2TXR volume to be updated simultaneously
	7:0	DSP2TXL_VOL [7:0]	C0h (0dB)	DSP2 TX (Left) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB (See Table 27 for volume range)
R1281 (0501h) DSP2 TX Right Volume	8	DSP2TX_VU	N/A	DSP2 TX output path Volume Update Writing a 1 to this bit will cause the DSP2TXL and DSP2TXR volume to be updated simultaneously
	7:0	DSP2TXR_VOL [7:0]	C0h (0dB)	DSP2 TX (Right) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB (See Table 27 for volume range)

Table 26 DSP Output (TX) Volume Control

DSP1/DSP2 Output Volume	Volume (dB)	DSP1/DSP2 Output Volume	Volume (dB)	DSP1/DSP2 Output Volume	Volume (dB)	DSP1/DSP2 Output Volume	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.375
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.750
3h	-70.875	43h	-46.875	83h	-22.875	C3h	1.125
4h	-70.500	44h	-46.500	84h	-22.500	C4h	1.500
5h	-70.125	45h	-46.125	85h	-22.125	C5h	1.875
6h	-69.750	46h	-45.750	86h	-21.750	C6h	2.250
7h	-69.375	47h	-45.375	87h	-21.375	C7h	2.625
8h	-69.000	48h	-45.000	88h	-21.000	C8h	3.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	3.375
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	3.750
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	4.125
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	4.500
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	4.875
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	5.250
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	5.625
10h	-66.000	50h	-42.000	90h	-18.000	D0h	6.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	6.375
12h	-65.250	52h	-41.250	92h	-17.250	D2h	6.750
13h	-64.875	53h	-40.875	93h	-16.875	D3h	7.125
14h	-64.500	54h	-40.500	94h	-16.500	D4h	7.500
15h	-64.125	55h	-40.125	95h	-16.125	D5h	7.875
16h	-63.750	56h	-39.750	96h	-15.750	D6h	8.250
17h	-63.375	57h	-39.375	97h	-15.375	D7h	8.625
18h	-63.000	58h	-39.000	98h	-15.000	D8h	9.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	9.375
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	9.750
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	10.125
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	10.500
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	10.875
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	11.250
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	11.625
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	12.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	12.375
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	12.750
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	13.125
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	13.500
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	13.875
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	14.250
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	14.625
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	15.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	15.375
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	15.750
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	16.125
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	16.500
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	16.875
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	17.250
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	17.625
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	17.625
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	17.625
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	17.625
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	17.625
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	17.625
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	17.625
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	17.625
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	17.625
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	17.625
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	17.625
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	17.625
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	17.625
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	17.625
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	17.625
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	17.625
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	17.625

Table 27 DSP Output (TX) Digital Volume Range

DSP OUTPUT (TX) HIGH PASS FILTER AND NOTCH FILTER

A digital high-pass filter can be enabled on the DSP1 TX and DSP2 TX output signal paths to remove DC offsets. This filter is enabled independently on each of the DSP TX output channels using the register bits described in Table 28.

The filter operates in one of three modes, selected by DSP1TX_HPF_MODE (for the DSP1 paths) and DSP2TX_HPF_MODE (for the DSP2 paths).

In Hi-Fi mode, the high pass filter is optimised for removing DC offsets without degrading the bass response. This mode provides a first-order filter, with a cut-off frequency of 3.7Hz.

In Application mode, the HPF cut-off frequency is set using DSP1TX_HPF_CUT (for the DSP1 paths) and DSP2TX_HPF_CUT (for the DSP2 paths). The application mode filter is a second-order filter.

In Voice mode, the high pass filter is optimised for voice communications and has a cut-off frequency of 260Hz. Note that this mode is only supported for 8kHz or 16kHz audio sample rates.

The quoted cut-off frequencies assume SYSCLK frequency of 12.288MHz. The cut-off frequencies scale proportionately for other SYSCLK frequencies (eg. 11.2896MHz).

A digital notch filter is also provided on the DSP1 TX and DSP2 TX output signals paths to improve stopband attenuation in 8kHz or 16kHz modes. These filters are enabled using the DSP1TX_NF and DSP2TX_NF registers. Note that this filter is only supported for 8kHz or 16kHz audio sample rates.

The audio sample rates for the DSP1 and DSP2 signal paths are set by DSP1_DIV and DSP2_DIV respectively. See “Clocking and Sample Rates” for further details of these registers.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1040 (0410h) DSP1 TX Filters	13	DSP1TX_NF	1	DSP1 TX output path Digital Notch Filter Enable 0 = Disabled at all times 1 = Enabled in 8kHz and 16kHz modes
	12	DSP1TXL_HPF	0	DSP1 TX (Left) output path Digital HPF Enable 0 = Disabled 1 = Enabled
	11	DSP1TXR_HPF	0	DSP1 TX (Right) output path Digital HPF Enable 0 = Disabled 1 = Enabled
	4:3	DSP1TX_HPF_MODE	00	DSP1 TX output path Digital HPF Mode 00 = Hi-Fi mode (cut-off is 3.7Hz) 01 = Application mode (cut-off is set by DSP1TX_HPF_CUT) 10 = Voice mode (cut-off is 260Hz) 11 = Reserved Note that Voice mode is only supported for 8kHz and 16kHz sample rates
	2:0	DSP1TX_HPF_CUT [2:0]	000	DSP1 TX output path Digital HPF cut-off frequency 000 = 50Hz 001 = 75Hz 010 = 100Hz 011 = 150Hz 100 = 200Hz 101 = 300Hz 110 = 400Hz 111 = Reserved Frequencies are correct for 12.288MHz SYSCLK. The cut-off frequencies scale proportionately for other SYSCLK frequencies (eg. 11.2896MHz).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1296 (0510h) DSP2 TX Filters	13	DSP1TX_NF	1	DSP2 TX output path Digital Notch Filter Enable 0 = Disabled at all times 1 = Enabled in 8kHz and 16kHz modes
	12	DSP2TXL_HPF	0	DSP2 TX (Left) output path Digital HPF Enable 0 = Disabled 1 = Enabled
	11	DSP2TXR_HPF	0	DSP2 TX (Right) output path Digital HPF Enable 0 = Disabled 1 = Enabled
	4:3	DSP2TX_HPF_MODE	00	DSP2 TX output path Digital HPF Mode 00 = Hi-Fi mode (cut-off is 3.7Hz) 01 = Application mode (cut-off is set by DSP2TX_HPF_CUT) 10 = Voice mode (cut-off is 260Hz) 11 = Reserved Note that Voice mode is only supported for 8kHz and 16kHz sample rates
	2:0	DSP2TX_HPF_CUT [2:0]	000	DSP2 TX output path Digital HPF cut-off frequency 000 = 50Hz 001 = 75Hz 010 = 100Hz 011 = 150Hz 100 = 200Hz 101 = 300Hz 110 = 400Hz 111 = Reserved Frequencies are correct for 12.288MHz SYSCLK. The cut-off frequencies scale proportionately for other SYSCLK frequencies (eg. 11.2896MHz).

Table 28 DSP Output (TX) High Pass Filter Control

DSP INPUT (RX) VOLUME CONTROL

A digital volume control is provided on the DSP1 RX and DSP2 RX input signal paths, allowing attenuation in the range -71.625dB to 0dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 192$; MUTE for $X = 0$ 0dB for $192 \leq X \leq 255$

The DSP1RX_VU and DSP2RX_VU bits control the loading of digital volume control data. When the volume update bit is set to 0, the associated volume control data will be loaded into the respective control register, but will not actually change the digital gain setting.

The DSP1RXL and DSP1RXR gain settings are updated when a 1 is written to DSP1RX_VU. The DSP2RXL and DSP2RXR gain settings are updated when a 1 is written to DSP2RX_VU. This makes it possible to update the gain of left and right channels simultaneously in either of the DSP blocks.

Note that digital volume control is also possible at the DAC output signal paths. See “Digital to Analogue Converter (DAC)” for further details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1026 (0402h) DSP1 RX Left Volume	8	DSP1RX_VU	N/A	DSP1 RX input path Volume Update Writing a 1 to this bit will cause the DSP1RXL and DSP1RXR volume to be updated simultaneously
	7:0	DSP1RXL_VOL [7:0]	C0h (0dB)	DSP1 RX (Left) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 30 for volume range)
R1027 (0403h) DSP1 RX Right Volume	8	DSP1RX_VU	N/A	DSP1 RX input path Volume Update Writing a 1 to this bit will cause the DSP1RXL and DSP1RXR volume to be updated simultaneously
	7:0	DSP1RXR_VOL [7:0]	C0h (0dB)	DSP1 RX (Right) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 30 for volume range)
R1282 (0502h) AIF2 DAC Left Volume	8	DSP2RX_VU	N/A	DSP2 RX input path Volume Update Writing a 1 to this bit will cause the DSP2RXL and DSP2RXR volume to be updated simultaneously
	7:0	DSP2RXL_VOL [7:0]	C0h (0dB)	DSP2 RX (Left) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 30 for volume range)
R1283 (0503h) AIF2 DAC Right Volume	8	DSP2RX_VU	N/A	DSP2 RX input path Volume Update Writing a 1 to this bit will cause the DSP2RXL and DSP2RXR volume to be updated simultaneously
	7:0	DSP2RXR_VOL [7:0]	C0h (0dB)	DSP2 RX (Right) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB (See Table 30 for volume range)

Table 29 DSP Input (RX) Volume Control

DSP1/DSP2 Input Volume	Volume (dB)	DSP1/DSP2 Input Volume	Volume (dB)	DSP1/DSP2 Input Volume	Volume (dB)	DSP1/DSP2 Input Volume	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.000
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.000
3h	-70.875	43h	-46.875	83h	-22.875	C3h	0.000
4h	-70.500	44h	-46.500	84h	-22.500	C4h	0.000
5h	-70.125	45h	-46.125	85h	-22.125	C5h	0.000
6h	-69.750	46h	-45.750	86h	-21.750	C6h	0.000
7h	-69.375	47h	-45.375	87h	-21.375	C7h	0.000
8h	-69.000	48h	-45.000	88h	-21.000	C8h	0.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	0.000
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	0.000
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	0.000
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	0.000
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	0.000
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	0.000
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	0.000
10h	-66.000	50h	-42.000	90h	-18.000	D0h	0.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	0.000
12h	-65.250	52h	-41.250	92h	-17.250	D2h	0.000
13h	-64.875	53h	-40.875	93h	-16.875	D3h	0.000
14h	-64.500	54h	-40.500	94h	-16.500	D4h	0.000
15h	-64.125	55h	-40.125	95h	-16.125	D5h	0.000
16h	-63.750	56h	-39.750	96h	-15.750	D6h	0.000
17h	-63.375	57h	-39.375	97h	-15.375	D7h	0.000
18h	-63.000	58h	-39.000	98h	-15.000	D8h	0.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	0.000
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	0.000
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	0.000
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	0.000
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	0.000
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	0.000
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	0.000
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	0.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	0.000
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	0.000
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	0.000
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	0.000
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	0.000
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	0.000
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	0.000
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	0.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	0.000
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	0.000
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	0.000
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	0.000
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	0.000
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	0.000
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	0.000
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	0.000
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	0.000
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	0.000
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	0.000
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	0.000
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	0.000
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	0.000
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	0.000
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	0.000
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	0.000
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	0.000
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	0.000
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	0.000
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	0.000
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	0.000
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	0.000

Table 30 DSP Input (RX) Digital Volume Range

DSP INPUT (RX) SOFT MUTE CONTROL

A soft mute function is provided on the DSP1 RX and DSP2 RX input signal paths. When the soft-mute function is selected, the WM8915 gradually attenuates the associated signal paths until the path is entirely muted.

When the soft-mute function is de-selected, the gain will either return instantly to the digital gain setting, or will gradually ramp back to the digital gain setting, depending on the applicable _UNMUTE_RAMP register field.

The mute and un-mute ramp rate is selectable between two different rates.

The DSP1 and DSP2 RX/input paths are soft-muted by default. To play back an audio signal, the soft-mute must first be de-selected by setting the applicable Mute bit to 0.

The soft un-mute would typically be used during playback of audio data so that when the Mute is subsequently disabled, a smooth transition is scheduled to the previous volume level and pop noise is avoided. This is desirable when resuming playback after pausing during a track.

The soft un-mute would typically not be required when un-muting at the start of a music file, in order that the first part of the music track is not attenuated. The instant un-mute behaviour is desirable in this case, when starting playback of a new track. See “Output Signal Path Soft Mute and Soft Un-Mute” (Figure 21) for an illustration of the soft mute function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1056 (0420h) DSP1 RX Filters (1)	9	DSP1RX_MUTE	1	DSP1 RX input path Soft Mute Control 0 = Un-mute 1 = Mute
	5	DSP1RX_MUTERATE	0	DSP1 RX input path Soft Mute Ramp Rate 0 = Fast ramp (maximum ramp time is 8ms) 1 = Slow ramp (maximum ramp time is 128ms)
	4	DSP1RX_UNMUTE_RAMP	0	DSP1 RX input path Unmute Ramp select 0 = Disabling soft-mute (DSP1RX_MUTE=0) will cause the volume to change immediately to DSP1RXL_VOL and DSP1RXR_VOL settings 1 = Disabling soft-mute (DSP1RX_MUTE=0) will cause the DAC volume to ramp up gradually to the DSP1RXL_VOL and DSP1RXR_VOL settings
R1312 (0520h) DSP2 Filters (1)	9	DSP2RX_MUTE	1	DSP2 RX input path Soft Mute Control 0 = Un-mute 1 = Mute
	5	DSP2RX_MUTERATE	0	DSP2 RX input path Soft Mute Ramp Rate 0 = Fast ramp (maximum ramp time is 8ms) 1 = Slow ramp (maximum ramp time is 128ms)
	4	DSP2RX_UNMUTE_RAMP	0	DSP2 RX input path Unmute Ramp select 0 = Disabling soft-mute (DSP2RX_MUTE=0) will cause the volume to change immediately to DSP2RXL_VOL and DSP2RXR_VOL settings 1 = Disabling soft-mute (DSP2RX_MUTE=0) will cause the DAC volume to ramp up gradually to the DSP2RXL_VOL and DSP2RXR_VOL settings

Table 31 DSP Input (RX) Soft Mute Control

DSP INPUT (RX) MONO MIX

A digital mono mix can be selected on the DSP1 RX and DSP2 RX input signal paths. The mono mix is generated as the sum of the Left and Right channel data. To prevent clipping, a 6dB attenuation is applied to the mono mix.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1056 (0420h) DSP1 RX Filters (1)	7	DSP1RX_MONO	0	DSP1 RX input path Mono Mix Control 0 = Disabled 1 = Enabled
R1312 (0520h) DSP2 RX Filters (1)	7	DSP2RX_MONO	0	DSP2 RX input path Mono Mix Control 0 = Disabled 1 = Enabled

Table 32 DSP Input (RX) Mono Mix and De-Emphasis Filter Control

DIGITAL TO ANALOGUE CONVERTER (DAC)

The WM8915 DACs receive digital input data from the DAC output mixers - see “Digital Mixing”. The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters four multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

The DAC oversampling rate is programmable; the high performance mode is selected by default. A low-power mode of DAC operation can be selected using the DAC_OSR128 bit - see “Clocking and Sample Rates” for details.

The analogue outputs from the DACs drive the Headphone outputs HPOUT1 and HPOUT2 via the output PGAs, as described in the “Output Signal Path” section.

The DACs are enabled using the register bits defined in Table 33.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (0005h) Power Management (5)	3	DAC2L_ENA	0	Left DAC2 Enable 0 = Disabled 1 = Enabled
	2	DAC2R_ENA	0	Right DAC2 Enable 0 = Disabled 1 = Enabled
	1	DAC1L_ENA	0	Left DAC1 Enable 0 = Disabled 1 = Enabled
	0	DAC1R_ENA	0	Right DAC1 Enable 0 = Disabled 1 = Enabled

Table 33 DAC Enable Control

OUTPUT SIGNAL PATH

The WM8915 output signal paths comprise two ground-referenced stereo headphone drivers and two stereo digital speaker drivers. These outputs are derived from the DAC output mixers - see “Digital Mixing” for details of the DAC output digital mixing function.

The WM8915 output signal paths can also be routed to the DSP1 TX and DSP2 TX output channels - see “Digital Mixing” for details of the DSP output signal mixing functions.

The WM8915 output signal paths and control registers are illustrated in Figure 20. See “Analogue Outputs” and “Digital Speaker Outputs” for further details of the Headphone outputs and Digital Speaker outputs respectively.

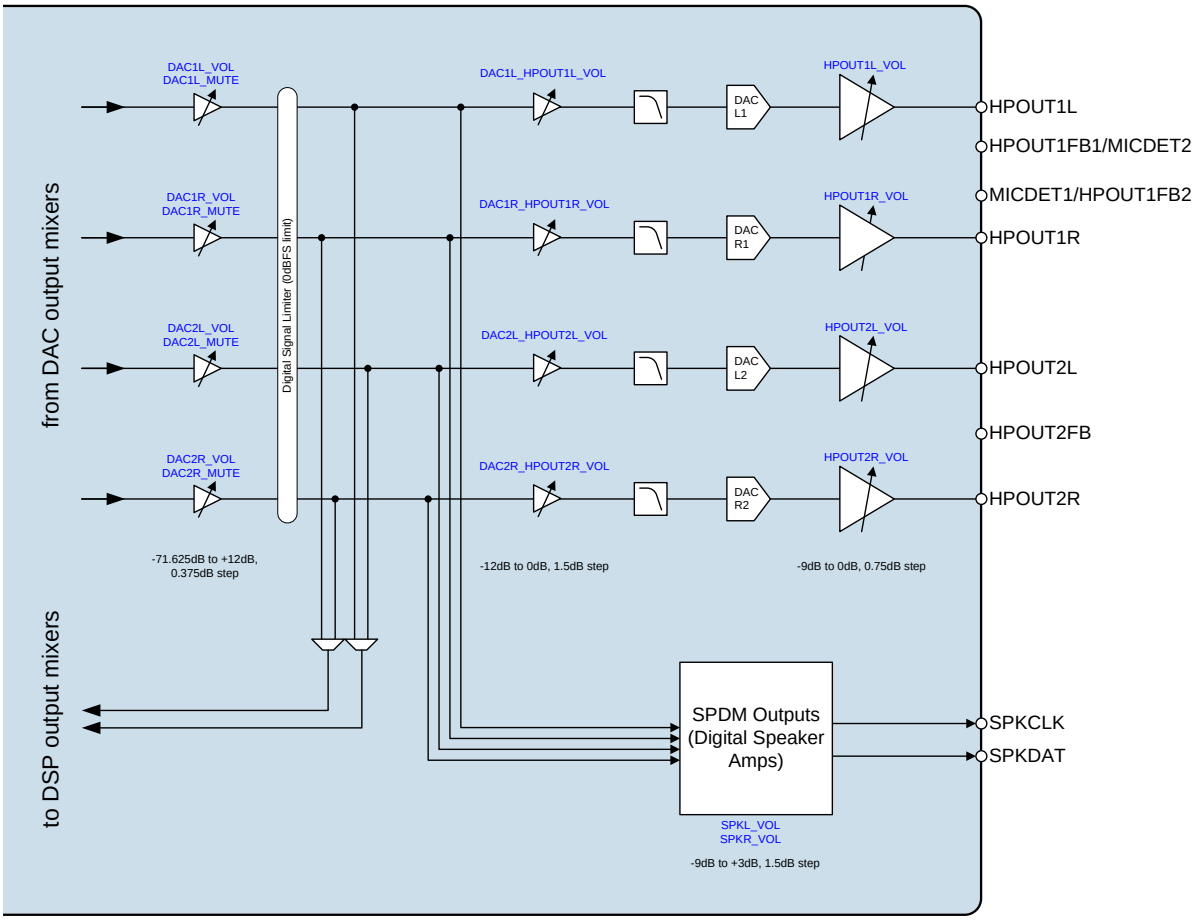


Figure 20 Control Registers for Output Signal Path

OUTPUT SIGNAL PATH DIGITAL VOLUME

The output signal level from each of the DAC output mixers can be controlled digitally over a range from -71.625dB to +12dB in 0.375dB steps, using the volume control registers described in Table 34. The level of attenuation for an eight-bit code X is given by:

0.375 × (X-192) dB for $1 \leq X \leq 224$; MUTE for $X = 0$; +12dB for $224 \leq X \leq 255$

The output signal level for each of the DAC output mixers is limited at 0dBFS. Note that volume settings greater than C0h (0dB) may cause signal clipping and distortion.

Each of these signal paths can be muted using the soft mute control bits described in Table 34. The WM8915 always applies a soft mute, where the volume is decreased gradually. The un-mute behaviour is configurable, as described in the "Output Signal Path Soft Mute and Soft Un-Mute" section.

The DAC1_VU and DAC2_VU bits control the loading of digital volume control data. When DAC1_VU is set to 0, the DAC1L_VOL or DAC1R_VOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to DAC1_VU. This makes it possible to update the gain of both channels simultaneously. A similar function for DAC2L and DAC2R is controlled by the DAC2_VU register bit.

The control registers described in Table 34 affect all of the output signal paths from the DAC output mixers. Note that additional digital and analogue volume controls are also provided for the HPOUT1 and HPOUT2 signal paths; these are described below in the "Headphone Signal Paths Volume Control" section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (0018h) DAC1 Left Volume	9	DAC1L_MUTE	1	DAC1L Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute
	8	DAC1_VU	N/A	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously
	7:0	DAC1L_VOL [7:0]	C0h (0dB)	DAC1L Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) E0h = 12.000dB FFh = 12.000dB (See Table 35 for volume range)
R25 (0019h) DAC1 Right Volume	9	DAC1R_MUTE	1	DAC1R Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute
	8	DAC1_VU	N/A	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously
	7:0	DAC1R_VOL [7:0]	C0h (0dB)	DAC1R Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) E0h = 12.000dB FFh = 12.000dB (See Table 35 for volume range)
R26 (001Ah) DAC2 Left Volume	9	DAC2L_MUTE	1	DAC2L Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8	DAC2_VU	N/A	DAC2L and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2L and DAC2R volume to be updated simultaneously
	7:0	DAC2L_VOL [7:0]	C0h (0dB)	DAC2L Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) E0h = 12.000dB FFh = 12.000dB (See Table 35 for volume range)
R27 (001Bh) DAC2 Right Volume	9	DAC2R_MUTE	1	DAC2R Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute
	8	DAC2_VU	N/A	DAC2R and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2R and DAC2R volume to be updated simultaneously
	7:0	DAC2R_VOL [7:0]	C0h (0dB)	DAC2R Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) E0h = 12.000dB FFh = 12.000dB (See Table 35 for volume range)

Table 34 Output Signal Path Digital Volume Control

DAC1L_VOL, DAC1R_VOL, DAC2L_VOL, DAC2R_VOL	Volume (dB)	DAC1L_VOL, DAC1R_VOL, DAC2L_VOL, DAC2R_VOL	Volume (dB)	DAC1L_VOL, DAC1R_VOL, DAC2L_VOL, DAC2R_VOL	Volume (dB)	DAC1L_VOL, DAC1R_VOL, DAC2L_VOL, DAC2R_VOL	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.375
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.750
3h	-70.875	43h	-46.875	83h	-22.875	C3h	1.125
4h	-70.500	44h	-46.500	84h	-22.500	C4h	1.500
5h	-70.125	45h	-46.125	85h	-22.125	C5h	1.875
6h	-69.750	46h	-45.750	86h	-21.750	C6h	2.250
7h	-69.375	47h	-45.375	87h	-21.375	C7h	2.625
8h	-69.000	48h	-45.000	88h	-21.000	C8h	3.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	3.375
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	3.750
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	4.125
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	4.500
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	4.875
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	5.250
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	5.625
10h	-66.000	50h	-42.000	90h	-18.000	D0h	6.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	6.375
12h	-65.250	52h	-41.250	92h	-17.250	D2h	6.750
13h	-64.875	53h	-40.875	93h	-16.875	D3h	7.125
14h	-64.500	54h	-40.500	94h	-16.500	D4h	7.500
15h	-64.125	55h	-40.125	95h	-16.125	D5h	7.875
16h	-63.750	56h	-39.750	96h	-15.750	D6h	8.250
17h	-63.375	57h	-39.375	97h	-15.375	D7h	8.625
18h	-63.000	58h	-39.000	98h	-15.000	D8h	9.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	9.375
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	9.750
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	10.125
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	10.500
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	10.875
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	11.250
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	11.625
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	12.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	12.000
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	12.000
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	12.000
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	12.000
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	12.000
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	12.000
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	12.000
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	12.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	12.000
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	12.000
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	12.000
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	12.000
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	12.000
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	12.000
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	12.000
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	12.000
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	12.000
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	12.000
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	12.000
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	12.000
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	12.000
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	12.000
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	12.000
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	12.000
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	12.000
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	12.000
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	12.000
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	12.000
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	12.000
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	12.000
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	12.000

Table 35 Output Signal Path Digital Volume Range

OUTPUT SIGNAL PATH SOFT MUTE AND SOFT UN-MUTE

The WM8915 has a soft mute function which ensures that a gradual attenuation is applied to the output signal paths when the mute is asserted. The soft mute rate can be selected using the DAC_MUTERATE bit.

When a mute bit is disabled, the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DAC_SOFTMUTEMODE register bit. If the gradual un-mute ramp is selected (DAC_SOFTMUTEMODE = 1), then the un-mute rate is determined by the DAC_MUTERATE bit.

Note that each output signal path is soft-muted by default. To play back an audio signal, the mute must first be disabled by setting the applicable mute control to 0 (see Table 34).

Soft Mute Mode would typically be enabled (DAC_SOFTMUTEMODE = 1) when using mute during playback of audio data so that when the mute is subsequently disabled, the volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing during a track).

Soft Mute Mode would typically be disabled (DAC_SOFTMUTEMODE = 0) when un-muting at the start of a music file, in order that the first part of the track is not attenuated (e.g. when starting playback of a new track, or resuming playback after pausing between tracks).

The output signal path soft-mute function is illustrated in Figure 21 for DAC1L and DAC1R. The same function is applicable to DAC2L and DAC2R also.

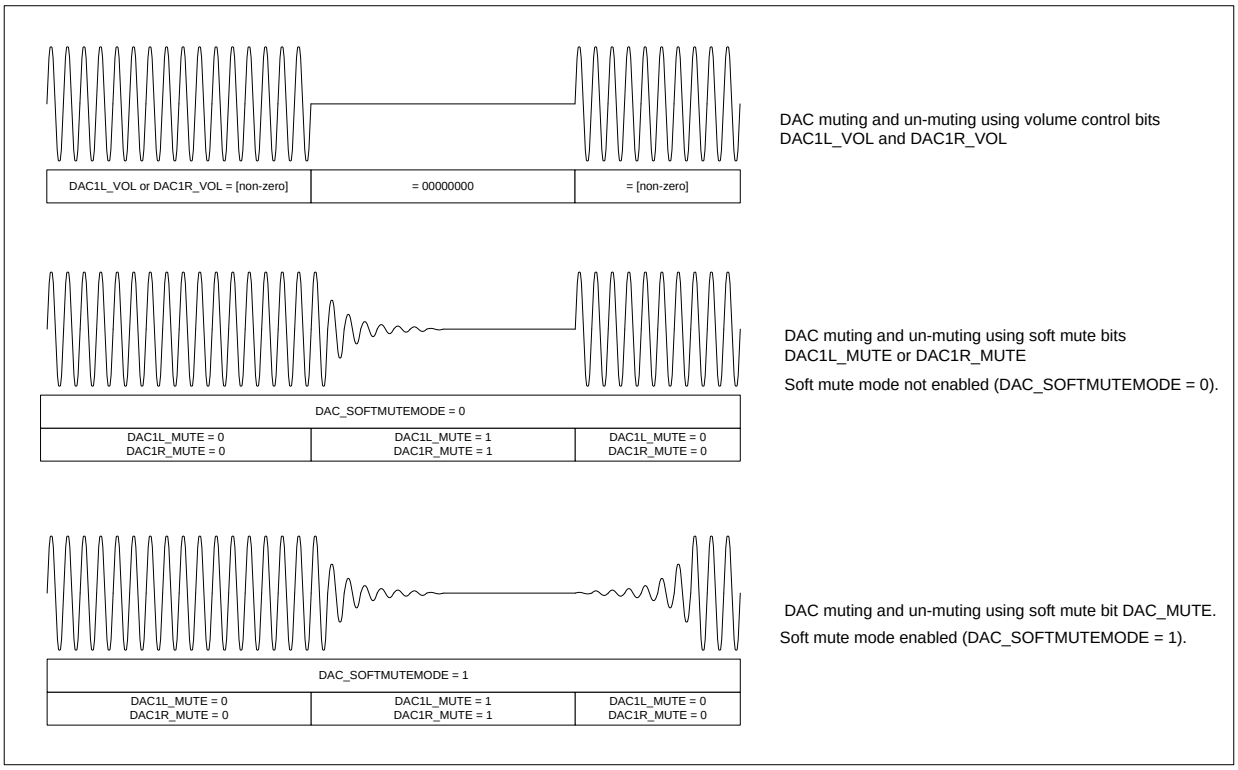


Figure 21 Output Signal Path Soft Mute Control

The Output Signal Path Soft Mute register controls are defined in Table 36.

The volume ramp rate during soft mute and un-mute is controlled by the DAC_MUTERATE bit. The ramp rate determines the rate at which the volume will be increased or decreased. Note that the actual ramp time depends on the extent of the difference between the muted and un-muted volume settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1552 (0610h) DAC Softmute	1	DAC_SOFT MUTEMODE	0	DAC Unmute Ramp select 0 = Disabling soft-mute (DAC [1/2][L/R]_MUTE=0) will cause the DAC volume to change immediately to DAC [1/2][L/R]_VOL settings 1 = Disabling soft-mute (DAC [1/2][L/R]_MUTE=0) will cause the DAC volume to ramp up gradually to the DAC [1/2][L/R]_VOL settings
	0	DAC_MUTE RATE	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (maximum ramp time is 10.7ms) 1 = Slow ramp (maximum ramp time is 171ms)

Table 36 Output Signal Path Soft-Mute Control

HEADPHONE SIGNAL PATHS ENABLE

The supply rails for headphone outputs are generated using an integrated dual-mode Charge Pump, which must be enabled whenever the headphone outputs are used. See the “Charge Pump” section for details on enabling and configuring this circuit.

The Headphone output paths can be actively discharged to AGND through internal resistors if desired. This is desirable at start-up in order to achieve a known output stage condition prior to enabling the VREF Midrail reference voltage. This is also desirable in shutdown to prevent the external connections from being affected by the internal circuits. The ground-referenced Headphone outputs are shorted to AGND by default; the short circuit is removed on each of these paths by setting the applicable fields HPOUT1L_RMV_SHORT, HPOUT1R_RMV_SHORT, HPOUT2L_RMV_SHORT or HPOUT2R_RMV_SHORT.

The ground-referenced Headphone output drivers are designed to suppress pops and clicks when enabled or disabled. However, it is necessary to control the drivers in accordance with a defined sequence in start-up and shut-down to achieve the pop suppression. It is also necessary to schedule the DC Servo offset correction at the appropriate point in the sequence (see “DC Servo”). Table 37 and Table 38 describe the recommended sequences for enabling and disabling these output drivers.

SEQUENCE	HPOUT1 ENABLE	HPOUT2 ENABLE
Step 1	HPOUT1L_ENA = 1 HPOUT1R_ENA = 1	HPOUT2L_ENA = 1 HPOUT2R_ENA = 1
Step 2	20µs delay	20µs delay
Step 3	HPOUT1L_ENA_DLY = 1 HPOUT1R_ENA_DLY = 1	HPOUT2L_ENA_DLY = 1 HPOUT2R_ENA_DLY = 1
Step 4	DC offset correction	DC offset correction
Step 5	HPOUT1L_RMV_SHORT = 1 HPOUT1L_ENA_OUTP = 1 HPOUT1R_RMV_SHORT = 1 HPOUT1R_ENA_OUTP = 1	HPOUT2L_RMV_SHORT = 1 HPOUT2L_ENA_OUTP = 1 HPOUT2R_RMV_SHORT = 1 HPOUT2R_ENA_OUTP = 1

Table 37 Headphone Output Enable Sequence

SEQUENCE	HPOUT1 DISABLE	HPOUT2 DISABLE
Step 1	HPOUT1L_RMV_SHORT = 0 HPOUT1L_ENA_OUTP = 0 HPOUT1L_ENA_DLY = 0 HPOUT1R_RMV_SHORT = 0 HPOUT1R_ENA_OUTP = 0 HPOUT1R_ENA_DLY = 0	HPOUT2L_RMV_SHORT = 0 HPOUT2L_ENA_OUTP = 0 HPOUT2L_ENA_DLY = 0 HPOUT2R_RMV_SHORT = 0 HPOUT2R_ENA_OUTP = 0 HPOUT2R_ENA_DLY = 0
Step 2	HPOUT1L_ENA = 0 HPOUT1R_ENA = 0	HPOUT2L_ENA = 0 HPOUT2R_ENA = 0

Table 38 Headphone Output Disable Sequence

The register bits relating to the Headphone Output control are defined in Table 39.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (0001h) Power Management (1)	7	HPOUT2L_ENA	0	Enables HPOUT2L input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT2L Enable sequence.
	6	HPOUT2R_ENA	0	Enables HPOUT2R input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT2R Enable sequence.
	5	HPOUT1L_ENA	0	Enables HPOUT1L input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT1L Enable sequence.
	4	HPOUT1R_ENA	0	Enables HPOUT1R input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT1R Enable sequence.
R96 (0060h) Analogue HP (1)	7	HPOUT1L_RMV_SHORT	0	Removes HPOUT1L short 0 = HPOUT1L short enabled 1 = HPOUT1L short removed For normal operation, this bit should be set as the final step of the HPOUT1L Enable sequence.
	6	HPOUT1L_OUTP	0	Enables HPOUT1L output stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the DC offset cancellation has been scheduled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5	HPOUT1L_DLY	0	Enables HPOUT1L intermediate stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the output signal path has been configured, and before DC offset cancellation is scheduled. This bit should be set with at least 20us delay after HPOUT1L_ENA.
	3	HPOUT1R_RMV_SHORT	0	Removes HPOUT1R short 0 = HPOUT1R short enabled 1 = HPOUT1R short removed For normal operation, this bit should be set as the final step of the HPOUT1R Enable sequence.
	2	HPOUT1R_OUTP	0	Enables HPOUT1R output stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the DC offset cancellation has been scheduled.
	1	HPOUT1R_DLY	0	Enables HPOUT1R intermediate stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the output signal path has been configured, and before DC offset cancellation is scheduled. This bit should be set with at least 20us delay after HPOUT1R_ENA.
R97 (0061h) Analogue HP (2)	7	HPOUT2L_RMV_SHORT	0	Removes HPOUT2L short 0 = HPOUT2L short enabled 1 = HPOUT2L short removed For normal operation, this bit should be set as the final step of the HPOUT2L Enable sequence.
	6	HPOUT2L_OUTP	0	Enables HPOUT2L output stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the DC offset cancellation has been scheduled.
	5	HPOUT2L_DLY	0	Enables HPOUT2L intermediate stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the output signal path has been configured, and before DC offset cancellation is scheduled. This bit should be set with at least 20us delay after HPOUT2L_ENA.
	3	HPOUT2R_RMV_SHORT	0	Removes HPOUT2R short 0 = HPOUT2R short enabled 1 = HPOUT2R short removed For normal operation, this bit should be set as the final step of the HPOUT2R Enable sequence.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2	HPOUT2R_OUTP	0	Enables HPOUT2R output stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the DC offset cancellation has been scheduled.
	1	HPOUT2R_DLY	0	Enables HPOUT2R intermediate stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the output signal path has been configured, and before DC offset cancellation is scheduled. This bit should be set with at least 20us delay after HPOUT2R_ENA.

Table 39 Headphone Output Signal Paths Control

HEADPHONE SIGNAL PATHS VOLUME CONTROL

Each of the Headphone output signal paths is provided with a set of volume control registers, allowing independent control of each of the HPOUT1L, HPOUT1R, HPOUT2L and HPOUT2R outputs.

The headphone signal paths incorporate a digital volume control (-12dB to 0dB in 1.5dB steps) and an analogue PGA volume control (-9dB to 0dB in 0.375dB steps). The associated control registers are described in Table 40.

Note that the headphone output signal paths are also controlled by the Output Signal Path Digital Volume controls, over a range of -71.625dB to +12dB, as described in Table 34. See Figure 20 for an illustration of the output signal path control registers.

The headphone output signal level is controlled by the HPOUT and DAC volume control registers, as illustrated in Figure 20. Note that the output signal level for each of the DAC output mixers is limited at 0dBFS.

To prevent "zipper noise", the analogue volume controls of the Headphone output PGAs are provided with a zero-cross function. When this feature is enabled, volume updates will not take place until a zero-crossing is detected. In the case of a long period without zero-crossings, a timeout function is provided. When the zero-cross function is enabled, the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout clock is enabled using TOCLK_ENA, the timeout period is set by TOCLK_DIV. See “Clocking and Sample Rates” for more information on these fields.

The DAC1_VU and DAC2_VU bits that control the DAC1L_VOL, DAC1R_VOL, DAC2L_VOL and DAC2R_VOL registers are duplicated in registers R28 through to R31, as described in Table 40; this provides additional flexibility to control the timing of any volume updates on the output signal paths.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (0015h) DAC1 HPOUT1 Volume	7:4	DAC1R_HPOUT1R_VOL [3:0]	1000	HPOUT1R Digital Volume Control -12dB to 0dB in 1.5dB steps 0000 = -12.0dB 0001 = -10.5dB … (1.5dB steps) 1000 = 0dB 1001 to 1111 = Reserved (See Table 41 for volume range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	DAC1L_HPOUT1L_VOL [3:0]	1000	HPOUT1L Digital Volume Control -12dB to 0dB in 1.5dB steps 0000 = -12.0dB 0001 = -10.5dB … (1.5dB steps) 1000 = 0dB 1001 to 1111 = Reserved (See Table 41 for volume range)
R22 (0016h) DAC2 HPOUT2 Volume	7:4	DAC2R_HPOUT2R_VOL [3:0]	1000	HPOUT2R Digital Volume Control -12dB to 0dB in 1.5dB steps 0000 = -12.0dB 0001 = -10.5dB … (1.5dB steps) 1000 = 0dB 1001 to 1111 = Reserved (See Table 41 for volume range)
	3:0	DAC2L_HPOUT2L_VOL [3:0]	1000	HPOUT2L Digital Volume Control -12dB to 0dB in 1.5dB steps 0000 = -12.0dB 0001 = -10.5dB … (1.5dB steps) 1000 = 0dB 1001 to 1111 = Reserved (See Table 41 for volume range)
R28 (001Ch) Output1 Left Volume	8	DAC1_VU	N/A	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously
	7	HPOUT1L_ZC	1	HPOUT1L PGA Zero Cross Enable 0 = Disabled 1 = Enabled
	3:0	HPOUT1L_VOL [3:0]	0000	HPOUT1L PGA Volume Control -9dB to 0dB in 0.75dB steps 0000 = -9.00dB 0001 = -8.25dB … (0.75dB steps) 1100 = 0dB 1101 to 1111 = Reserved (See Table 41 for volume range)
R29 (001Dh) Output1 Right Volume	8	DAC1_VU	N/A	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously
	7	HPOUT1R_ZC	1	HPOUT1R PGA Zero Cross Enable 0 = Disabled 1 = Enabled
	3:0	HPOUT1R_VOL [3:0]	0000	HPOUT1R PGA Volume Control -9dB to 0dB in 0.75dB steps 0000 = -9.00dB 0001 = -8.25dB … (0.75dB steps) 1100 = 0dB 1101 to 1111 = Reserved (See Table 41 for volume range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (001Eh) Output2 Left Volume	8	DAC2_VU	N/A	DAC2L and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2L and DAC2R volume to be updated simultaneously
	7	HPOUT2L_ZC	1	HPOUT2L PGA Zero Cross Enable 0 = Disabled 1 = Enabled
	3:0	HPOUT2L_VOL [3:0]	0000	HPOUT2L PGA Volume Control -9dB to 0dB in 0.75dB steps 0000 = -9.00dB 0001 = -8.25dB … (0.75dB steps) 1100 = 0dB 1101 to 1111 = Reserved (See Table 41 for volume range)
R31 (001Fh) Output2 Right Volume	8	DAC2_VU	N/A	DAC2L and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2L and DAC2R volume to be updated simultaneously
	7	HPOUT2R_ZC	1	HPOUT2R PGA Zero Cross Enable 0 = Disabled 1 = Enabled
	3:0	HPOUT2R_VOL [3:0]	0000	HPOUT2R PGA Volume Control -9dB to 0dB in 0.75dB steps 0000 = -9.00dB 0001 = -8.25dB … (0.75dB steps) 1100 = 0dB 1101 to 1111 = Reserved (See Table 41 for volume range)

Table 40 Headphone Signal Paths Volume Control

DAC1L_HPOUT1L_VOL, DAC1R_HPOUT1R_VOL, DAC2L_HPOUT2L_VOL, DAC2R_HPOUT2R_VOL,	VOLUME (dB)	HPOUT1L_VOL, HPOUT1R_VOL, HPOUT2L_VOL, HPOUT2R_VOL	VOLUME (dB)
0h	-12.00	0h	-9.00
1h	-10.50	1h	-8.25
2h	-9.00	2h	-7.50
3h	-7.50	3h	-6.75
4h	-6.00	4h	-6.00
5h	-4.50	5h	-5.25
6h	-3.00	6h	-4.50
7h	-1.50	7h	-3.75
8h	0.00	8h	-3.00
9h	0.00	9h	-2.25
Ah	0.00	Ah	-1.50
Bh	0.00	Bh	-0.75
Ch	0.00	Ch	0.00
Dh	0.00	Dh	Reserved
Eh	0.00	Eh	Reserved
Fh	0.00	Fh	Reserved

Table 41 Headphone Signal Paths Volume Range

DIGITAL SPEAKER (SPDM) SIGNAL PATHS VOLUME CONTROL

Each of the Digital Speaker (SPDM) output channels is provided with a digital volume control, allowing independent control of the each output, from -9dB to +3dB in 1.5dB steps.

Note that the SPDM signal paths are also controlled by the Output Signal Path Digital Volume controls, over a range of -71.625dB to +12dB, as described in Table 34. See Figure 20 for an illustration of the output signal path control registers.

The SPDM signal paths are controlled by the DAC and SPDM volume control registers, as illustrated in Figure 20. Note that the output signal level for each of the DAC output mixers is limited at 0dBFS.

Further details of the SPDM outputs, including selection of the Left and Right channel sources, are provided in the “Digital Speaker Outputs” section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2051 (0803h) PDM Speaker Volume	7:4	SPKR_VOL [3:0]	0110	PDM Speaker Output (Right) Digital Volume Control -9dB to +3dB in 1.5dB steps (See Table 43 for volume range)
	3:0	SPKL_VOL [3:0]	0110	PDM Speaker Output (Left) Digital Volume Control -9dB to +3dB in 1.5dB steps (See Table 43 for volume range)

Table 42 Digital Speaker Output (SPDM) Volume Control

SPKR_VOL, SPKL_VOL	VOLUME (dB)
0h	-9.00
1h	-7.50
2h	-6.00
3h	-4.50
4h	-3.00
5h	-1.50
6h	0.00
7h	1.50
8h	3.00
9h	0.00
Ah	0.00
Bh	0.00
Ch	0.00
Dh	0.00
Eh	0.00
Fh	0.00

Table 43 Digital Speaker Output (SPDM) Volume Range

CHARGE PUMP

The WM8915 incorporates a dual-mode Charge Pump which generates the supply rails for the headphone output drivers HPOUT1L, HPOUT1R, HPOUT2L and HPOUT2R. The Charge Pump has a single supply input, CPVDD, and generates split rails CPVOUTP and CPVOUTN according to the headphone output signal conditions. The Charge Pump connections are illustrated in Figure 22 (see "Applications Information" for external component values). An input decoupling capacitor may also be required at CPVDD, depending upon the system configuration.

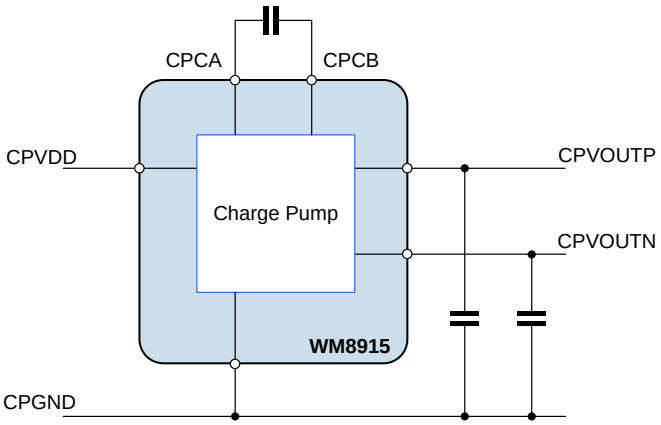


Figure 22 Charge Pump External Connections

The Charge Pump is enabled by setting the CP_ENA bit. When enabled, the charge pump adjusts the output voltages (CPVOUTP and CPVOUTN) as well as the switching frequency in order to optimise the power consumption according to the headphone output signal conditions.

The Charge Pump control mechanism enables the Wolfson 'Class W' mode, which allows the power consumption to be optimised in real time.

Under the recommended usage conditions of the WM8915, the Charge Pump will be enabled by running the default headphone Start-Up sequence as described in the "Control Write Sequencer" section. (Similarly, it will be disabled by running the Shut-Down sequence.) In these cases, the user does not need to write to the CP_ENA bit.

Note that the charge pump clock is derived from internal clock SYSCLK. Under normal circumstances, an external clock signal must be present for the charge pump to function. However, the FLL has a free-running mode that does not require an external clock but will generate an internal clock suitable for running the charge pump. The clock division from SYSCLK is handled transparently by the WM8915 without user intervention. Refer to the "Clocking and Sample Rates" section for more details on the FLL and the clocking configuration.

When the Charge Pump is disabled, the output can be left floating or can be actively discharged, depending on the CP_DISCH control bit.

The Charge Pump control fields are described in Table 44.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R64 (0040h) Charge Pump (1)	15	CP_ENA	0	Charge Pump Enable 0 = Disabled 1 = Enabled
R65 (0041h) Charge Pump (2)	15	CP_DISCH	1	Charge Pump Discharge Select 0 = Charge Pump outputs floating when disabled 1 = Charge Pump outputs discharged when disabled

Table 44 Charge Pump Control

DC SERVO

The WM8915 provides a DC servo circuit on the headphone outputs HPOUT1L, HPOUT1R, HPOUT2L and HPOUT2R in order to remove DC offset from these ground-referenced outputs. When enabled, the DC servo ensures that the DC level of these outputs remains within 1mV of ground. Removal of the DC offset is important because any deviation from GND at the output pin will cause current to flow through the load under quiescent conditions, resulting in increased power consumption. Additionally, the presence of DC offsets can result in audible pops and clicks at power up and power down.

The recommended usage of the DC Servo is initialised by running the default Start-Up sequence as described in the “Control Write Sequencer” section. The default Start-Up sequence executes a series of DC offset corrections, after which the measured offset correction is maintained on the headphone output channels.

If a different usage is required, eg. if a periodic DC offset correction is required, then the default Start-Up sequence may be modified according to specific requirements. Updates to the DC Servo correction can also be scheduled using register writes, including during audio playback. The relevant control fields are described in the following paragraphs and are defined in Table 45.

DC SERVO ENABLE AND START-UP

The DC Servo circuit is enabled on HPOUT1L and HPOUT1R by setting DCS_ENA_CHAN_0 and DCS_ENA_CHAN_1 respectively. Equivalent registers are provided for HPOUT2L and HPOUT2R. When the DC Servo is enabled, the DC offset correction can be commanded in a number of different ways, including single-shot and periodically recurring events.

Writing a logic 1 to DCS_TRIG_STARTUP_*n* initiates a series of DC offset measurements and applies the necessary correction to the associated output; (‘n’ = 0 for HPOUT1L, 1 for HPOUT1R, 2 for HPOUT2L, 3 for HPOUT2R). On completion, the headphone output will be within 1mV of AGND. This is the DC Servo mode selected by the default Start-Up sequence. Completion of the DC offset correction triggered in this way is indicated by the DCS_STARTUP_COMPLETE field, as described in Table 45. Typically, this operation takes 86ms per channel.

For correct operation of the DC Servo Start-Up mode, it is important that there is no active audio signal present on the signal path while the mode is running. The DC Servo Start-Up mode should be scheduled at the correct position within the Headphone Output Enable sequence, as described in the Output Signal Path” section. All other stages of the analogue signal path should be fully enabled prior to commanding the Start-Up mode; the DAC Digital Mute function should be used, where appropriate, to ensure there is no active audio signal present during the DC Servo measurements.

Writing a logic 1 to DCS_TRIG_DAC_WR_*n* causes the DC offset correction to be set to the value contained in the DCS_DAC_WR_VAL_*n* fields in Register R85 and R86. This mode is useful if the required offset correction has already been determined and stored; it is faster than the DCS_TRIG_STARTUP_*n* mode, but relies on the accuracy of the stored settings. Completion of the DC offset correction triggered in this way is indicated by the DCS_DAC_WR_COMPLETE field, as described in Table 45. Typically, this operation takes 2ms per channel.

The current DC offset value for each Headphone output channel can be read from the DCS_DAC_WR_VAL_*n* fields. These values may form the basis of settings that are subsequently used by the DC Servo in DAC Write mode. Note that these fields have a different definition for Read and Write, as described in Table 45.

When using either of the DC Servo options above, the status of the DC offset correction process is indicated by the DCS_CAL_COMPLETE field; this is the logical OR of the DCS_STARTUP_COMPLETE and DCS_DAC_WR_COMPLETE fields.

The DCS_DAC_WR_COMPLETE bits can be used as inputs to the Interrupt control circuit or used to generate an external logic signal on a GPIO pin. See “Interrupts” and “General Purpose Input/Output” for further details.

The DC Servo control fields associated with start-up operation are described in Table 45. It is important to note that, to minimise audible pops/clicks, the Start-Up and DAC Write modes of DC Servo operation should be commanded as part of a control sequence which includes muting and shorting of the headphone outputs; a suitable sequence is defined in the default Start-Up sequence.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R80 (0050h) DC Servo (1)	3	DCS_ENA_CHAN_3	0	DC Servo enable for HPOUT2R 0 = Disabled 1 = Enabled
	2	DCS_ENA_CHAN_2	0	DC Servo enable for HPOUT2L 0 = Disabled 1 = Enabled
	1	DCS_ENA_CHAN_1	0	DC Servo enable for HPOUT1R 0 = Disabled 1 = Enabled
	0	DCS_ENA_CHAN_0	0	DC Servo enable for HPOUT1L 0 = Disabled 1 = Enabled
R81 (0051h) DC Servo (2)	7	DCS_TRIG_START UP_3	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT2R. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.
	6	DCS_TRIG_START UP_2	0	*as above, for HPOUT2L*
	5	DCS_TRIG_START UP_1	0	*as above, for HPOUT1R*
	4	DCS_TRIG_START UP_0	0	*as above, for HPOUT1L*
	3	DCS_TRIG_DAC_W R_3	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT2R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.
	2	DCS_TRIG_DAC_W R_2	0	*as above, for HPOUT2L*
	1	DCS_TRIG_DAC_W R_1	0	*as above, for HPOUT1R*
	0	DCS_TRIG_DAC_W R_0	0	*as above, for HPOUT1L*
R85 (0055h) DC Servo (6)	15:8	DCS_DAC_WR_VA L_3 [7:0]	00h	Writing to this field sets the DC Offset value for HPOUT2R in DAC Write DC Servo mode. Reading this field gives the current DC Offset value for HPOUT2R. Two's complement format. LSB is 0.25mV. Range is -32mV to +31.75mV
	7:0	DCS_DAC_WR_VA L_2 [7:0]	00h	*as above, for HPOUT2L*
R86 (0056h) DC Servo (7)	15:8	DCS_DAC_WR_VA L_1 [7:0]	00h	*as above, for HPOUT1R*
	7:0	DCS_DAC_WR_VA L_0 [7:0]	00h	*as above, for HPOUT1L*

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R87 (0057h) DC Servo Readback	11:8	DCS_CAL_COMPLETE [3:0]	00	DC Servo Complete status 0 = DAC Write or Start-Up DC Servo mode not completed. 1 = DAC Write or Start-Up DC Servo mode complete. Bit [3] = HPOUT2R Bit [2] = HPOUT2L Bit [1] = HPOUT1R Bit [0] = HPOUT1L
	7:4	DCS_DAC_WR_COMPLETE [3:0]	00	DC Servo DAC Write status 0 = DAC Write DC Servo mode not completed. 1 = DAC Write DC Servo mode complete. Bit [3] = HPOUT2R Bit [2] = HPOUT2L Bit [1] = HPOUT1R Bit [0] = HPOUT1L
	3:0	DCS_STARTUP_COMPLETE [3:0]	00	DC Servo Start-Up status 0 = Start-Up DC Servo mode not completed. 1 = Start-Up DC Servo mode complete. Bit [3] = HPOUT2R Bit [2] = HPOUT2L Bit [1] = HPOUT1R Bit [0] = HPOUT1L

Table 45 DC Servo Enable and Start-Up Modes

DC SERVO ACTIVE MODES

The DC Servo modes described above are suitable for initialising the DC offset correction circuit on the Headphone outputs as part of a controlled start-up sequence which is executed before the signal path is fully enabled. Additional modes are available for use whilst the signal path is active; these modes may be of benefit following a large change in signal gain, which can lead to a change in DC offset level. Periodic updates may also be desirable to remove slow drifts in DC offset caused by changes in parameters such as device temperature.

The DC Servo circuit is enabled on HPOUT1L and HPOUT1R by setting DCS_ENA_CHAN_0 and DCS_ENA_CHAN_1 respectively, as described earlier in Table 45. The DC Servo circuit is enabled on HPOUT2L and HPOUT2R by setting DCS_ENA_CHAN_2 and DCS_ENA_CHAN_3 respectively.

Writing a logic 1 to DCS_TRIG_SINGLE_*n* initiates a single DC offset measurement and adjustment to the associated output; ('n' = 0 for HPOUT1L, 1 for HPOUT1R, 2 for HPOUT2L, 3 for HPOUT2R). This will adjust the DC offset correction on the selected channel by no more than 1LSB (0.25mV).

Writing a logic 1 to DCS_TRIG_SERIES_*n* initiates a series of DC offset measurements and applies the necessary correction to the associated output. The number of DC Servo operations performed is determined by DCS_SERIES_NO_01 (for HPOUT1L and HPOUT1R) or DCS_SERIES_NO_23 (for HPOUT1L and HPOUT1R). In each case, a maximum of 128 operations may be selected, though a much lower value will be sufficient in most applications.

Setting DCS_TIMER_PERIOD_01 to a non-zero value will cause a single DC offset measurement and adjustment to be scheduled on a periodic basis for HPOUT1L and HPOUT1R. Setting DCS_TIMER_PERIOD_23 to a non-zero value will cause a single DC offset measurement and adjustment to be scheduled on a periodic basis for HPOUT2L and HPOUT2R. In each case, periodic rates ranging from every 0.52s to in excess of 2hours can be selected.

The DC Servo control fields associated with active modes (suitable for use on a signal path that is in active use) are described in Table 46.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R81 (0051h) DC Servo (2)	15	DCS_TRIG_SINGLE_3	0	Writing 1 to this bit selects a single DC offset correction for HPOUT2R. In readback, a value of 1 indicates that the DC Servo single correction is in progress.
	14	DCS_TRIG_SINGLE_2	0	*as above, for HPOUT2L*
	13	DCS_TRIG_SINGLE_1	0	*as above, for HPOUT1R*
	12	DCS_TRIG_SINGLE_0	0	*as above, for HPOUT1L*
	11	DCS_TRIG_SERIES_3	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT2R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.
	10	DCS_TRIG_SERIES_2	0	*as above, for HPOUT2L*
	9	DCS_TRIG_SERIES_1	0	*as above, for HPOUT1R*
	8	DCS_TRIG_SERIES_0	0	*as above, for HPOUT1L*
R82 (0052h) DC Servo (3)	11:8	DCS_TIMER_PERIOD_23 [3:0]	0000	Time between periodic updates (HPOUT2L and HPOUT2R). Time is calculated as 0.251s x (2^PERIOD) 0000 = Off 0001 = 0.502s …. 1010 = 257s (4min 17s) 1111 = 8224s (2hr 17ms)
	3:0	DCS_TIMER_PERIOD_01 [3:0]	0000	Time between periodic updates (HPOUT1L and HPOUT1R). Time is calculated as 0.251s x (2^PERIOD) 0000 = Off 0001 = 0.502s …. 1010 = 257s (4min 17s) 1111 = 8224s (2hr 17ms)
R84 (0054h) DC Servo (5)	14:8	DCS_SERIES_NO_23 [6:0]	010_1010	Number of DC Servo updates to perform in a series event (HPOUT2L and HPOUT2R). 0 = 1 update 1 = 2 updates ... 127 = 128 updates
	6:0	DCS_SERIES_NO_01 [6:0]	010_1010	Number of DC Servo updates to perform in a series event (HPOUT1L and HPOUT1R). 0 = 1 update 1 = 2 updates ... 127 = 128 updates

Table 46 DC Servo Active Modes

GPIO / INTERRUPT OUTPUTS FROM DC SERVO

When using the DC Servo Start-Up or DAC Write modes, the DCS_CAL_COMPLETE register provides readback of the status of the DC offset correction. This can be read from register R87 as described in Table 45.

The DCS_CAL_COMPLETE bits can also be used as inputs to the Interrupt control circuit and used to trigger an Interrupt event - see “Interrupts”.

The DCS_CAL_COMPLETE bits can also be used as inputs to the GPIO function and used to generate external logic signals indicating the DC Servo status. See “General Purpose Input/Output” for details of how to configure a GPIO pin to output the DC Servo status.

ANALOGUE OUTPUTS

The WM8915 provides two ground-referenced stereo headphone outputs. These outputs are derived from the four DAC channels (DAC1L, DAC1R, DAC2L and DAC2R). Volume control is provided on each of these outputs as described in the “Output Signal Path” section.

Each headphone output driver is capable of driving up to 30mW into a 16Ω load or 25mW into a 32Ω load such as a stereo headset or headphones. The outputs are ground-referenced, eliminating any requirement for AC coupling capacitors. This is achieved by having separate positive and negative supply rails powered by an on-chip charge pump. A DC Servo circuit removes any DC offset from the headphone outputs, suppressing ‘pop’ noise and minimising power consumption. The Charge Pump and DC Servo are described separately (see “Charge Pump” and “DC Servo” respectively).

It is recommended to connect a zobel network to the headphone output pins HPOUT1L, HPOUT1R, HPOUT2L and HPOUT2R for best audio performance in all applications. The components of the zobel network have the effect of dampening high frequency oscillations or instabilities that can arise outside the audio band under certain conditions. Possible sources of these instabilities include the inductive load of a headphone coil or an active load in the form of an external line amplifier. The capacitance of lengthy cables or PCB tracks can also lead to amplifier instability. The zobel network should comprise of a 20Ω resistor and 100nF capacitor in series with each other, as illustrated in Figure 23.

If any ground-referenced headphone output is not used, then the zobel network components can be omitted from the corresponding output pin, and the pin can be left floating. The respective headphone driver(s) should not be enabled in this case.

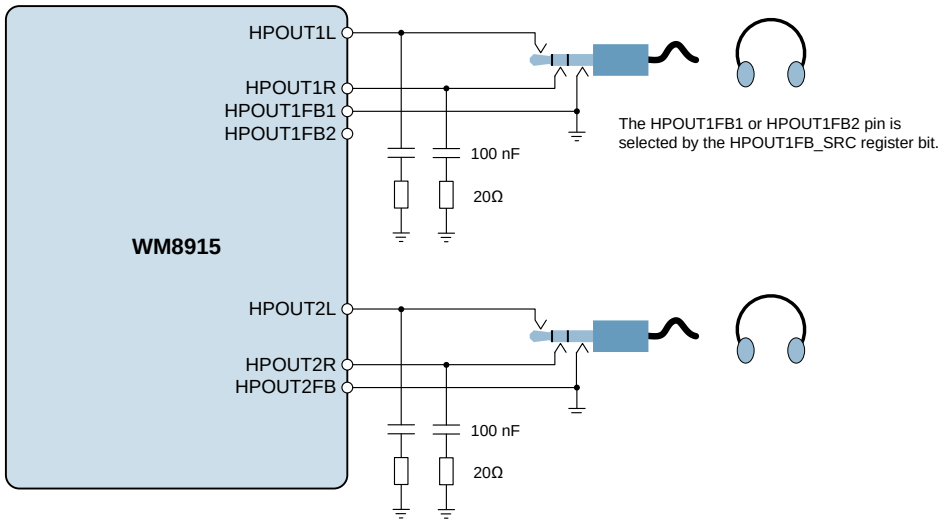


Figure 23 Zobel Network Components for Headphone Output

The headphone outputs incorporate a common mode, or ground loop, feedback path which provides rejection of system-related ground noise. The feedback pins must be connected to ground for normal operation of the headphone output.

Note that the feedback pins should be connected to GND close to the headphone jack, as illustrated in Figure 23.

The ground feedback path for HPOUT1L and HPOUT1R is provided via the HPOUT1FB1 or HPOUT1FB2 pins; the applicable connection must be selected using the HPOUT1FB_SRC register, as described in Table 47.

Note that the HPOUT1FB1 and HPOUT1FB2 pins also support the Accessory Detect (MICDET) functions, as described in "External Accessory Detection". To avoid unwanted interaction, it is recommended to set the MICD_SRC register to the same value as the HPOUT1FB_SRC register.

The ground feedback path for HPOUT2L and HPOUT2R is provided via the HPOUT2FB pin. No register configuration is required for the HPOUT2FB connection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49 (0031h) Accessory Detect Mode 2	2	HPOUT1FB_SRC	0	HPOUT1 Ground feedback pin select 0 = HPOUT1FB1/MICDET2 1 = HPOUT1FB2/MICDET1
	1	MICD_SRC	0	Accessory Detect (MICDET) pin select 0 = HPOUT1FB2/MICDET1 1 = HPOUT1FB1/MICDET2

Table 47 Headphone Output Ground Feedback Control

DIGITAL SPEAKER OUTPUTS

The WM8915 supports a two-channel digital speaker (SPDM) output interface. Two channels of audio data are multiplexed on the SPKDAT pin; the data is clocked using the output pin SPKCLK.

The digital speaker output channels are enabled using the control bits described in Table 49.

When the digital speaker (SPDM) interface is enabled, the WM8915 outputs a clock signal on the SPKCLK pin. Under default conditions, the clock frequency is 6.144MHz. The clock frequency can be adjusted using the SPK_OSR128 register; setting this register to 0 gives a clock frequency of 3.072MHz. The clock frequency is also controlled by the SYSCLK_RATE register, as described in Table 48. See "Clocking and Sample Rates" for details of the SPK_OSR128 and SYSCLK_RATE registers.

SYSCLK_RATE	SPK_OSR128	SPKCLK FREQUENCY
0	0	3.072MHz
0	1	3.072MHz
1	0	3.072MHz
1	1	6.144MHz (default)
Note: The quoted SPKCLK frequency assumes SYSCLK frequency of 12.288MHz. The SPKCLK frequency scales proportionately for other SYSCLK frequencies (eg. 11.2896MHz).		

Table 48 SPDM Clock Frequency

Two audio channels are interleaved on SPKDAT as illustrated in Figure 24. Note that the SPDM interface supports two different operating modes; these are selected using the SPK_FMT register bit. See "Signal Timing Requirements" for detailed timing information in both modes.

When SPK_FMT = 0 (Mode A), then the Left PDM channel is valid at the rising edge of SPKCLK; the Right PDM channel is valid at the falling edge of SPKCLK.

When SPK_FMT = 1 (Mode B), then the Left PDM channel is valid during the low phase of SPKCLK; the Right PDM channel is valid during the high phase of SPKCLK.

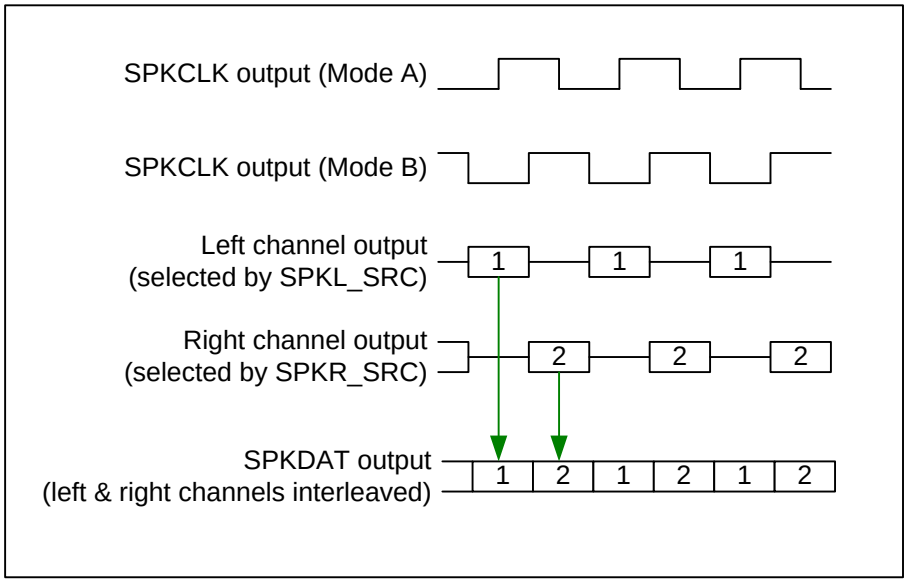


Figure 24 Digital Speaker Outputs (PDM) Interface Timing

The source for each SPDM channel is selectable from the four DAC channels (DAC1L, DAC1R, DAC2L and DAC2R). The audio source for the left/right channels on SPKDAT are selected using the SPKL_SRC and SPKR_SRC registers respectively.

Volume control is provided on each of the SPDM channels as described in the “Output Signal Path” section; the SPKR_VOL and SPKL_VOL registers provide independent control of the two SPDM channels.

Each of the PDM channels can be independently muted. When muted, the default output on each channel is a DSD-compliant silent stream (0110_1001b). The mute output code can be programmed to other values if required, using the SPK_MUTE_SEQ1 register field. The mute output code can be transmitted MSB-first or LSB-first; this is selectable using the SPK_MUTE_ENDIAN register.

Note that the PDM Mute function is not a soft-mute; the audio output is interrupted immediately when the PDM mute is asserted. It is recommended to use the DAC soft-mute function to reduce audio to zero before applying the PDM mute. See “Output Signal Path” for details of the DAC soft-mute function.

If a PDM channel is muted without first using the DAC soft-mute, then the pop noise can be minimised using the zero-cross function on that channel. In this case, mute and un-mute commands will not take place until a zero-cross is detected. Note that a timeout period is associated with this function, which must be enabled using TOCLK_ENA (see “Clocking and Sample Rates”).

If the DAC soft-mute is used to control the audio signal before selecting the PDM mute, then the zero-cross function should be disabled.

The Digital Speaker PDM signal paths and control registers are illustrated in Figure 25.

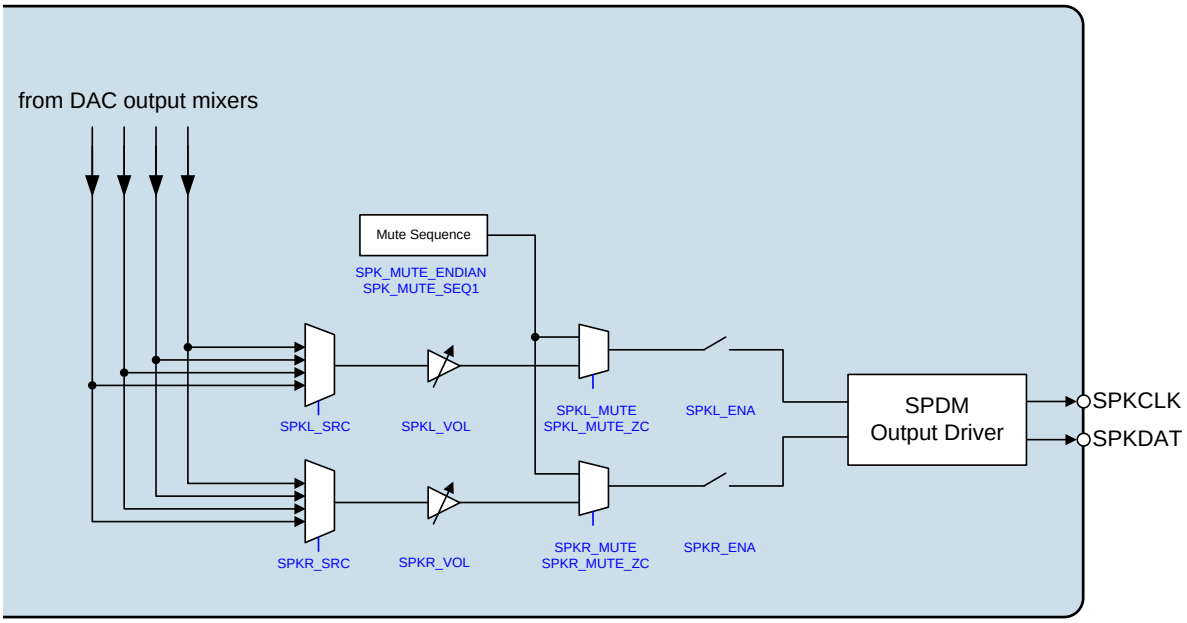


Figure 25 Digital Speaker Output (SPDM) Signal Paths

The Digital Speaker Output (PDM) interface control fields are described in Table 49.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2048 (0800h) Left PDM Speaker	4	SPKL_ENA	0	PDM Speaker Output (Left) Enable 0 = Disabled 1 = Enabled
	3	SPKL_MUTE	0	PDM Speaker Output (Left) Mute 0 = Audio output 1 = Mute Sequence output
	2	SPKL_MUTE_ZC	0	PDM Speaker Output (Left) Zero Cross 0 = Disabled 1 = Enabled
	1:0	SPKL_SRC [1:0]	00	PDM Speaker Output (Left) Source 00 = DAC1L 01 = DAC1R 10 = DAC2L 11 = DAC2R
R2049 (0801h) Right PDM Speaker	4	SPKR_ENA	0	PDM Speaker Output (Right) Enable 0 = Disabled 1 = Enabled
	3	SPKR_MUTE	0	PDM Speaker Output (Right) Mute 0 = Audio output 1 = Mute Sequence output
	2	SPKR_MUTE_ZC	0	PDM Speaker Output (Right) Zero Cross 0 = Disabled 1 = Enabled
	1:0	SPKR_SRC [1:0]	01	PDM Speaker Output (Right) Source 00 = DAC1L 01 = DAC1R 10 = DAC2L 11 = DAC2R
R2050 (0802h) PDM Speaker Mute Sequence	8	SPK_MUTE_ENDIAN	0	PDM Speaker Output Mute Sequence Control 0 = Mute sequence is LSB first 1 = Mute sequence output is MSB first
	7:0	SPK_MUTE_SEQ1 [7:0]	69h	PDM Speaker Output Mute Sequence Defines the 8 bit code that is output on SPKDAT (left) or SPKDAT (right) when muted.
R2051 (0803h) PDM Speaker Volume	15	SPK_FMT	0	PDM Speakout Output timing format 0 = Mode A (PDM data is valid at the rising/falling edges of SPKCLK) 1 = Mode B (PDM data is valid during the high/low phase of SPKCLK)

Table 49 Digital Speaker Output (SPDM) Control

EXTERNAL ACCESSORY DETECTION

The WM8915 provides an accessory detection function which can sense the impedance of external components via dedicated monitor pins.

Headphone impedance can be detected via the HPDETL and HPDETR pins; this can be used to set different gain levels or other configuration settings according to the type of load connected. For example, different settings may be applicable to Headphone or Line output loads.

Microphones and other accessories can be detected via the MICDET1 or MICDET2 pins. The insertion or removal of a microphone, and the status of a hookswitch can be detected. This feature can also be used to detect push-button operation.

When headphone detection is selected on HPDETL or HPDETR, the WM8915 produces a single result of the measured impedance. When microphone detection is selected, a cyclic schedule is enabled, and the MICDET impedance is measured repeatedly. The Interrupt function can be used to indicate the accessory detection status.

Note that SYSCLK must be present and enabled when using the accessory detection function; see "Clocking and Sample Rates" for details of SYSCLK and the associated register control fields.

Note that, where specific timing or frequency figures for External Accessory detection are quoted, these figures assume a SYSCLK frequency of 12.288MHz. The timing scales proportionately for other SYSCLK frequencies (eg. 11.2896MHz).

The Frequency Locked Loop (FLL) free-running mode provides flexibility to clock the microphone detection function without any external reference clock, eg. in low-power standby operating conditions. See "Clocking and Sample Rates" for details of the WM8915 clocking options and FLL.

HEADPHONE DETECT

The WM8915 headphone detection circuit measures the impedance of an external load connected to the headphone outputs. This feature can be used to set different gain levels or to apply other configuration settings according to the type of load connected. Two separate monitor pins are provided for headphone detection; each of these may be associated with any of the four headphone outputs of the WM8915.

Headphone detection may only be selected on one channel at a time. The available channels are the HPDETL pin or the HPDETR pin. The selected channel is determined by the JD_MODE register as described in Table 50.

Headphone detection on the selected channel is commanded by writing a '1' to the HP_POLL register bit.

When headphone detection is commanded, the WM8915 uses an adjustable current source to determine the connected impedance. A sweep of measurement currents is applied. The rate of this sweep can be adjusted using the HP_CLK_DIV and HP_STEP_SIZE registers. To avoid audible clicks, the default step size should always be used (HP_STEP_SIZE = 0).

The timing of the current source ramp is also controlled by the HP_HOLDTIME register. It is recommended that the default setting (001b) be used for this parameter.

Completion of the headphone detection is indicated by the HP_DONE register bit. When this bit is set, the measured load impedance can be read from the HP_LVL register. Note that, after the HP_DONE bit has been asserted, it will remain asserted until a subsequent headphone detection measurement is commanded.

The headphone detection function is an input to the Interrupt control circuit and can be used to trigger an Interrupt event on completion of the headphone detection - see "Interrupts".

The headphone detection function can also generate a GPIO output, providing an external indication of the headphone detection. See "General Purpose Input/Output" for details of how to configure a GPIO pin to output the Headphone Detection signal.

The register fields associated with Headphone Detection are described in Table 50. The external circuit configuration is illustrated in Figure 26.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (0030h) Accessory Detect Mode 1	1:0	JD_MODE [1:0]	00	Accessory Detect Mode Select 00 = MICDET measurement 01 = HPDETL measurement 10 = HPDETR measurement 11 = Reserved Note that the MICDET function is provided on the MICDET1 or MICDET2 pins, depending on the MICD_SRC register bit.
R52 (0034h) Headphone Detect 1	7:5	HP_HOLDTIME [2:0]	001	Headphone Detect Hold Time (Selects the hold time between ramp up and ramp down of the headphone detect current source. The clock cycle rate is set by HP_CLK_DIV) 000 = 1 clock cycle 001 = 4 clock cycles 010 = 16 clock cycles 011 = 64 clock cycles 100 = 256 clock cycles 101 = 512 clock cycles 110 = 768 clock cycles 111 =1024 clock cycles
	4:3	HP_CLK_DIV [1:0]	00	Headphone Detect Clock Rate (Selects the clocking rate of the headphone detect adjustable current source.) 00 = 32kHz 01 = 16kHz 10 = 8kHz 11 = 4kHz
	1	HP_STEP_SIZE	0	Headphone Detect Ramp Rate 0 = Normal rate 1 = Fast rate
	0	HP_POLL	0	Headphone Detect Enable Write 1 to start HP Detect function
R53 (0035h) Headphone Detect 2	7	HP_DONE	0	Headphone Detect Status 0 = HP Detect not complete 1 = HP Detect done
	6:0	HP_LVL [6:0]	00h	Headphone Detect Level LSB = 1 ohm Valid from 8..126 ohm 08h = 8 ohm or less 09h = 9 ohm 0Ah = 10 ohm …. 7Dh = 125 ohm 7Eh = 126 ohm or more

Table 50 Headphone Detect Control

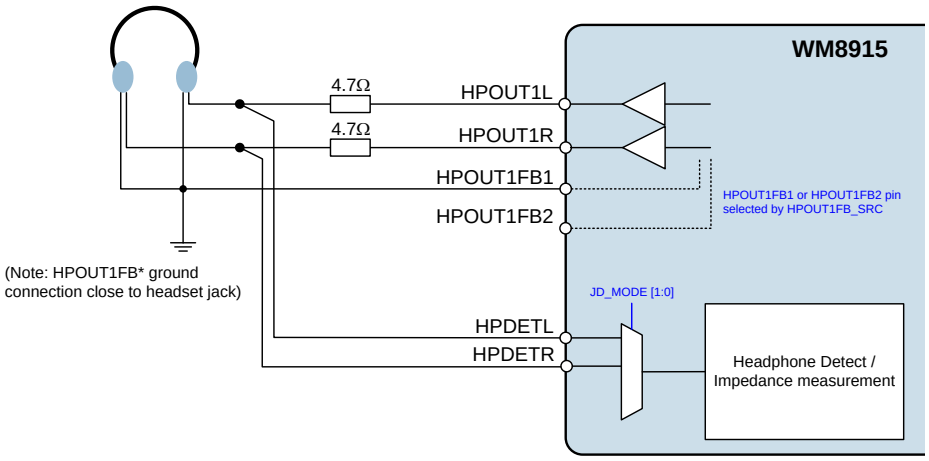


Figure 26 Headphone Detect Interface

The external connections for the Headphone Detect circuit are illustrated in Figure 26. Note that any combination of headphone outputs (HPOUT1L, HPOUT1R, HPOUT2L and HPOUT2R) may be connected to HPDETL or HPDETR pins, according to the application requirements.

Note that, where external resistors are connected in series with the headphone load, as illustrated, it is recommended that the HPDET connection is to the headphone side of the resistors. If the HPDET connection is made to the WM8915 side of the resistors, this will lead to a corresponding offset in the measured impedance.

Note that the measurement accuracy of the headphone detect function may be up to +/-30%.

Under default conditions, the measurement time varies between 17ms and 61ms according to the impedance of the external load. A high impedance will be measured faster than a low impedance.

MICROPHONE DETECT

The WM8915 microphone detection circuit measures the impedance of an external load connected to one of the MICDET pins. This feature can be used to detect the presence of a microphone, and the status of the associated hookswitch. It can also be used to detect push-button status or the connection of other external accessories.

The microphone detection circuit measures the impedance connected to MICDET1 or MICDET2, and reports whether the measured impedance lies within one of 9 pre-defined levels (including the 'no accessory detected' level). This means it can detect the presence of a typical microphone and up to 7 push-buttons. One of the impedance levels is specifically designed to detect a video accessory (typical 75Ω) load if required.

The microphone detection circuit uses one of the MICBIAS outputs as a reference. The WM8915 will automatically enable the appropriate MICBIAS when required in order to perform the detection function; this allows the detection function to be supported in low-power standby operating conditions.

To select microphone detection on one of the MICDET pins, the JD_MODE register must be set to 00. The JD_MODE register is defined in Table 50. Note that the WM8915 cannot perform headphone and microphone detection simultaneously.

The microphone detection circuit can be enabled on the MICDET1 pin or the MICDET2 pin, selected by the MICD_SRC register.

Note that the MICDET1 and MICDET2 pins also support the Headphone ground feedback function for HPOUT1, as described in the "Analogue Outputs" section. To avoid unwanted interaction, it is recommended to set the HPOUT1FB_SRC register to the same value as the MICD_SRC register.

When JD_MODE is set to 00, then Microphone detection is enabled by setting MICD_ENA.

When microphone detection is enabled, the WM8915 performs a number of measurements in order to determine the MICDET impedance. The measurement process is repeated at a cyclic rate controlled by MICD_RATE. (The MICD_RATE register selects the delay between completion of one measurement and the start of the next.)

For best accuracy, the measured impedance is only deemed valid after more than one successive measurement has produced the same result. The MICD_DBTIME register provides control of the de-bounce period; this can be either 2 measurements or 4 measurements.

When the microphone detection result has settled (ie. after the applicable de-bounce period), the WM8915 indicates valid data by setting the MICD_VALID bit. The measured impedance is indicated using the MICD_LVL and MICD_STS register bits, as described in Table 51.

The MICD_VALID bit, when set, remains asserted for as long as the microphone detection function is enabled (ie. while MICD_ENA = 1). If the detected impedance changes, then the MICD_LVL and MICD_STS fields will change, but the MICD_VALID bit will remain set, indicating valid data at all times.

The microphone detection reports a measurement result in one of the pre-defined impedance levels. Each measurement level can be enabled or disabled independently; this provides flexibility according to the required thresholds, and offers a faster measurement time in some applications. The MICD_LVL_SEL register is described in detail later in this section.

Note that the impedance levels quoted in the MICD_LVL description assume that a microphone (475Ω to 30kΩ impedance) is also present on the MICDET pin. The limits quoted in the "Electrical Characteristics" refer to the combined effective impedance on the MICDET pin. Typical external components are described in the "Applications Information" section.

The microphone detection function is an input to the Interrupt control circuit and can be used to trigger an Interrupt event every time an accessory insertion, removal or impedance change is detected. See "Interrupts" for further details.

The microphone detection function can also generate a GPIO output, providing an external indication of the microphone detection. This GPIO output is pulsed every time an accessory insertion, removal or impedance change is detected. See "General Purpose Input/Output" for details of how to configure a GPIO pin to output the microphone detection signal.

The register fields associated with Microphone Detection (or other accessories) are described in Table 51. The external circuit configuration is illustrated in Figure 27.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (0030h) Accessory Detect Mode 1	1:0	JD_MODE [1:0]	00	Accessory Detect Mode Select 00 = MICDET measurement 01 = HPDETL measurement 10 = HPDETR measurement 11 = Reserved Note that the MICDET function is provided on the MICDET1 or MICDET2 pins, depending on the MICD_SRC register bit.
R49 (0031h) Accessory Detect Mode 2	2	HPOUT1FB_SRC	0	HPOUT1 Ground feedback pin select 0 = HPOUT1FB1/MICDET2 1 = HPOUT1FB2/MICDET1
	1	MICD_SRC	0	Accessory Detect (MICDET) pin select 0 = HPOUT1FB2/MICDET1 1 = HPOUT1FB1/MICDET2
	0	MICD_BIAS_SRC	0	Accessory Detect (MICDET) reference select 0 = MICBIAS1 1 = MICBIAS2
R56 (0038h) Mic Detect 1	15:12	MICD_BIAS_STARTTIME [3:0]	0111	Mic Detect Bias Startup Delay (If MICBIAS is not enabled already, this field selects the delay time allowed for MICBIAS to startup prior to performing the MICDET function.) 0000 = 0ms (continuous) 0001 = 0.25ms 0010 = 0.5ms 0011 = 1ms 0100 = 2ms 0101 = 4ms 0110 = 8ms 0111 = 16ms 1000 = 32ms 1001 = 64ms 1010 = 128ms 1011 = 256ms 1100 to 1111 = 512ms
	11:8	MICD_RATE [3:0]	0110	Mic Detect Rate (Selects the delay between successive Mic Detect measurements.) 0000 = 0ms (continuous) 0001 = 0.25ms 0010 = 0.5ms 0011 = 1ms 0100 = 2ms 0101 = 4ms 0110 = 8ms 0111 = 16ms 1000 = 32ms 1001 = 64ms 1010 = 128ms 1011 = 256ms 1100 to 1111 = 512ms

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	MICD_DBTIME	0	Mic Detect De-bounce 0 = 2 measurements 1 = 4 measurements
	0	MICD_ENA	0	Mic Detect Enable 0 = Disabled 1 = Enabled
R57 (0039h) Mic Detect 2	7:0	MICD_LVL_SEL [7:0]	1011_1111	Mic Detect Level Select (enables Mic Detection in specific impedance ranges) [7] = Enable >475 ohm detection [6] = Not used - must be set to 0 [5] = Enable 326 ohm detection [4] = Enable 152 ohm detection [3] = Enable 77 ohm detection [2] = Enable 47.6 ohm detection [1] = Enable 29.4 ohm detection [0] = Enable 14 ohm detection Note that the impedance values quoted assume that a microphone (475ohm-30kohm) is also present on the MICDET pin.
R58 (003Ah) Mic Detect 3	10:2	MICD_LVL [8:0]	0_0000_0000	Mic Detect Level (indicates the measured impedance) [8] = >475 ohm, <30k ohm [7] = Not used [6] = 326 ohm [5] = 152 ohm [4] = 77 ohm [3] = 47.6 ohm [2] = 29.4 ohm [1] = 14 ohm [0] = <2 ohm Note that the impedance values quoted assume that a microphone (475ohm-30kohm) is also present on the MICDET pin.
	1	MICD_VALID	0	Mic Detect Data Valid 0 = Not Valid 1 = Valid
	0	MICD_STS	0	Mic Detect Status 0 = No Mic Accessory present (impedance is >30k ohm) 1 = Mic Accessory is present (impedance is <30k ohm)

Table 51 Microphone Detect Control

The external connections for the Microphone Detect circuit are illustrated in Figure 27. In typical applications, it can be used to detect a microphone or button press.

By default, the microphone detection function uses MICBIAS2 as a reference. The microphone detection function will automatically enable MICBIAS2 when required for MICDET impedance measurement. It is also possible to select MICBIAS1 as the reference for the microphone detection circuit. This is selected using the MICD_BIAS_SRC register, as described in Table 51.

If the selected reference (MICBIAS1 or MICBIAS2) is not already enabled (ie. if MICB*n*_ENA = 0, where *n* is '1' or '2' as appropriate), then the applicable MICBIAS source will be enabled for short periods of time only, every time the impedance measurement is scheduled. To allow time for the

MICBIAS source to start-up, a time delay is applied before the measurement is performed; this is configured using the MICD_BIAS_STARTTIME register, as described in Table 51.

The MICD_BIAS_STARTTIME register should be set to 16ms or more if MICB*n*_RATE = 1 (pop-free start-up / shut-down). The MICD_BIAS_STARTTIME register should be set to 0.25ms or more if MICB*n*_RATE = 0 (fast start-up / shut-down).

If the selected reference is not enabled continuously (ie. if MICB*n*_ENA = 0), then the applicable MICBIAS discharge bit (MICB*n*_DISCH) should be set to 0.

The MICBIAS sources are configured using the registers described in Table 1, in the "Analogue Input Signal Path" section.

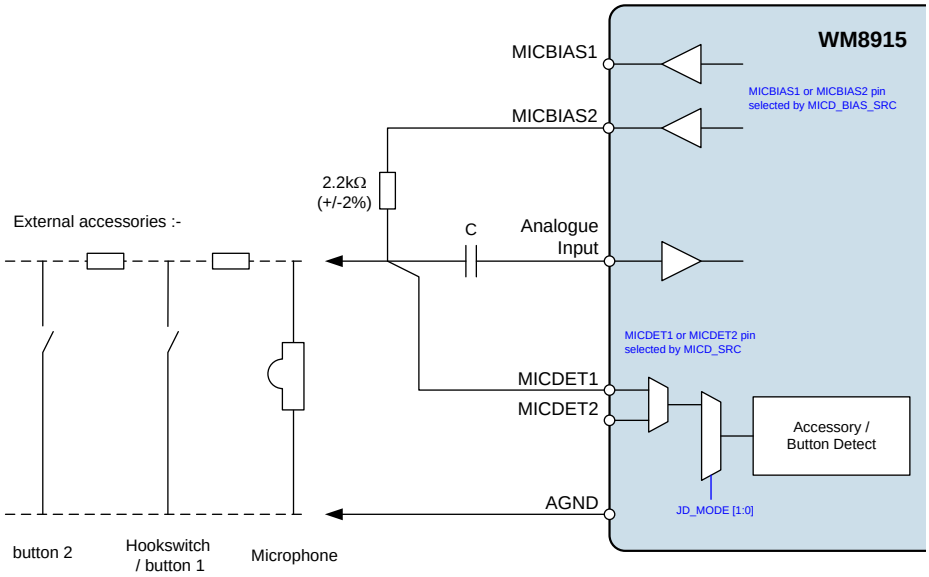


Figure 27 Microphone Detect Interface

The MICD_LVL_SEL [7:0] register bits allow each of the impedance measurement levels to be enabled or disabled independently. This allows the function to be tailored to the particular application requirements.

If one or more bits within the MICD_LVL_SEL register is set to 0, then the corresponding impedance level will be disabled. Any measured impedance which lies in a disabled level will be reported as the next lowest, enabled level.

For example, the MICD_LVL_SEL [3] bit enables the detection of impedances around 77Ω. If MICD_LVL_SEL [3] = 0, then an external impedance of 77Ω will not be indicated as 77Ω but will be indicated as 47Ω; this would be reported in the MICD_LVL register as MICD_LVL [3] = 1.

With all measurement levels enabled, the WM8915 can detect the presence of a typical microphone and up to 7 push-buttons. The microphone detect function is specifically designed to detect a video accessory (typical 75Ω) load if required.

See "Applications Information" for typical recommended external components for microphone, video or push-button accessory detection.

The microphone detection circuit assumes that a 2.2kΩ (2%) resistor is connected to the selected MICBIAS reference, as illustrated. Different resistor values will lead to inaccuracy in the impedance measurement.

The measurement accuracy of the microphone detect function is assured whenever the connected load is within the applicable limits specified in the "Electrical Characteristics". Note that a 2.2kΩ (2%) resistor must also be connected between MICDET and the selected MICBIAS reference.

Note that the connection of a microphone will change the measured impedance on the MICDET pin; see "Applications Information" for recommended components for typical applications.

The measurement time varies between 100µs and 500µs according to the impedance of the external load. A high impedance will be measured faster than a low impedance.

The timing of the microphone detect function is illustrated in Figure 28. Two different cases are shown, according to whether MICBIAS*n* is enabled periodically by the impedance measurement function (MICB*n*_ENA=0), or is enabled at all times (MICB*n*_ENA=1).

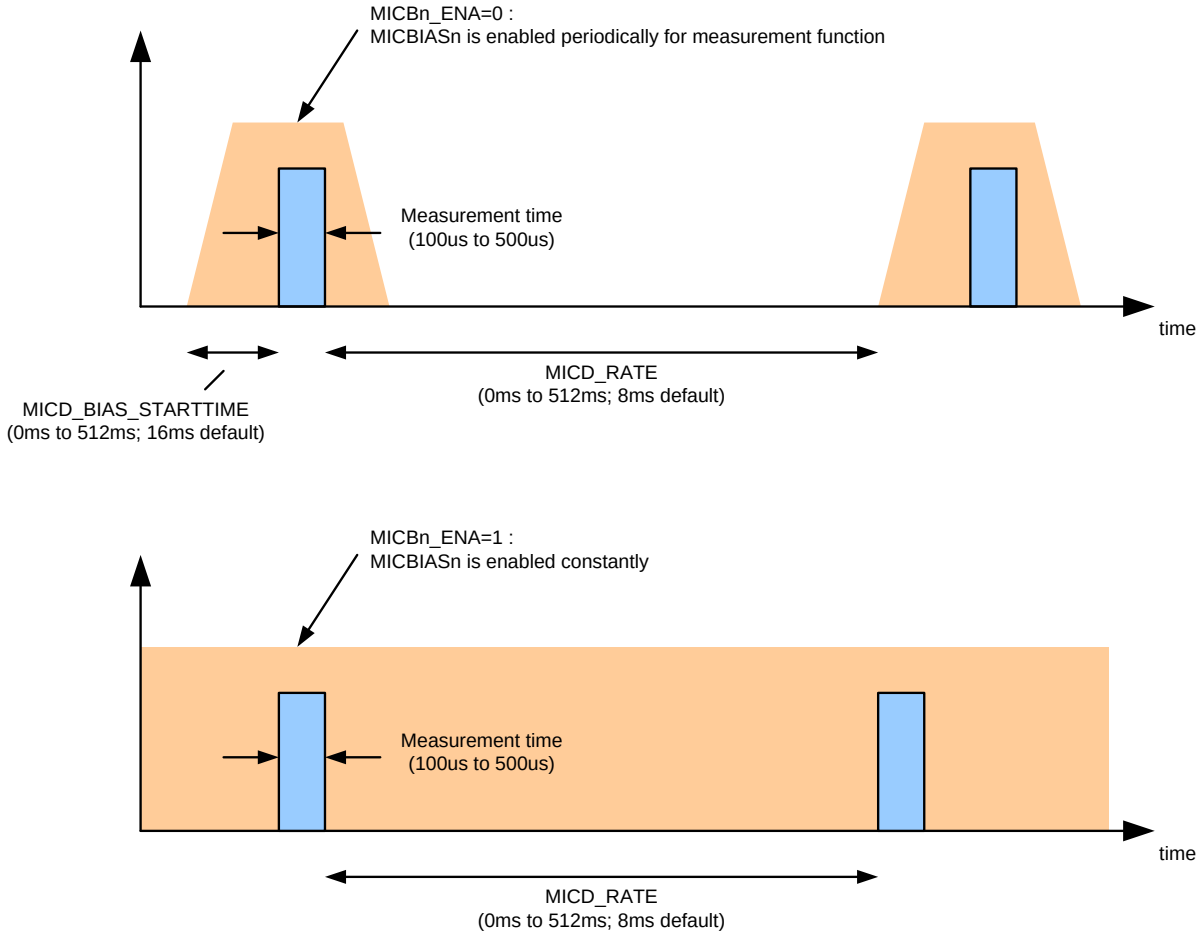


Figure 28 Microphone Detect Timing

GENERAL PURPOSE INPUT/OUTPUT

The WM8915 provides a number of GPIO functions to enable interfacing and detection of external hardware and to provide logic outputs to other devices. The input functions can be polled directly or can be used to generate an Interrupt (IRQ) event. The GPIO and Interrupt circuits support the following functions:

- Audio interface functions (ADCLRCLK1, ADCLRCLK2)
- Button detect (GPIO input)
- Logic '1' and logic '0' output (GPIO output)
- Interrupt (IRQ) status output
- Microphone accessory status detection
- Headphone accessory status detection
- Dynamic Range Control (DRC) signal activity detection
- Digital Core FIFO error status output
- Control Write Sequencer status output
- DC Servo Complete status output
- FLL Clock Switch status output
- Frequency Locked Loop (FLL) Lock status output
- Clock output (SYSCLK divided by OPCLK_DIV)
- Frequency Locked Loop (FLL) Clock output

GPIO CONTROL

For each GPIO, the selected function is determined by the GPn_FN field, where n identifies the GPIO pin (1 to 5). The pin direction, set by GPn_DIR, must be set according to function selected by GPn_SEL.

The audio interface functions ADCLRCLK1 and ADCLRCLK2 are supported using the GPIO1 pin and GPIO2 pins respectively. These functions are selected by setting the corresponding GPn_FN register to 00h.See "Digital Audio Interface Control" for further details.

When a pin is configured as a GPIO input (GPn_DIR = 1), the logic level at the pin can be read from the respective GPn_LVL bit. Note that GPn_LVL is not affected by the GPn_POL bit.

A de-bounce circuit can be enabled on any GPIO input, to avoid false event triggers. This is enabled on each pin by setting the respective GPn_DB bit. Note that TOCLK must be enabled when this input de-bouncing is required.

When a pin is configured as a Logic Level output (GPn_DIR = 0, GPn_FN = 01h), its level can be set to logic 0 or logic 1 using the GPn_LVL field.

When a pin is configured as an output (GPn_DIR = 0), the polarity can be inverted using the GPn_POL bit. When GPn_POL = 1, then the selected output function is inverted. In the case of Logic Level output (GPn_FN = 01h), the external output will be the opposite logic level to GPn_LVL when GPn_POL = 1.

A GPIO output can be either CMOS driven or Open Drain. This is selected on each pin using the respective GPn_OP_CFG bit.

Internal pull-up and pull-down resistors may be enabled using the GPn_PU and GPn_PD fields; this allows greater flexibility to interface with different signals from other devices.

Each of the GPIO pins is an input to the Interrupt control circuit and can be used to trigger an Interrupt event. An interrupt event is triggered on the rising and falling edge of the GPIO input. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

The register fields that control the GPIO pins are described in Table 52.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1792 (0700h) GPIO1 to R1796 (0704h) GPIO5	15	GPn_DIR	1	GPIOn Pin Direction 0 = Output 1 = Input
	14	GPn_PU	0	GPIOn Pull-Up Enable 0 = Disabled 1 = Enabled
	13	GPn_PD	1	GPIOn Pull-Down Enable 0 = Disabled 1 = Enabled
	10	GPn_POL	0	GPIOn Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)
	9	GPn_OP_CFG	0	GPIOn Output Configuration 0 = CMOS 1 = Open Drain
	8	GPn_DB	1	GPIOn Input De-bounce 0 = Disabled 1 = Enabled
	6	GPn_LVL	0	GPIOn level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. For output functions only, when GPn_POL is set, the register contains the opposite logic level to the external pin.
	4:0	GPn_FN [4:0]	0001	GPIOn Pin Function (see Table 53 for details)
Note: *n* is a number 1 to 5 that identifies the individual GPIO.				

Table 52 GPIO Function Control

GPIO FUNCTION SELECT

The available GPIO functions are described in Table 53. The function of each GPIO is set using the GPn_FN register, where n identifies the GPIO pin (1 to 5). Note that the respective GPn_DIR must also be set according to whether the function is an input or output.

GPn_FN	DESCRIPTION	COMMENTS
00h	GPIO1 - ADCLRCLK1 GPIO2 - ADCLRCLK2 GPIO3 - n/a GPIO4 - n/a GPIO5 - n/a	Alternate functions for AIF1 and AIF2.
01h	Button detect input / Logic level output	GPn_DIR = 0: GPIO pin logic level is set by GPn_LVL. GPn_DIR = 1: Button detect or logic level input.
02h	IRQ	Interrupt (IRQ) output 0 = IRQ not asserted 1 = IRQ asserted
03h	Microphone Detect	Microphone Detect (MICDET accessory) IRQ output A single 31µs pulse is output whenever an accessory insertion, removal or impedance change is detected.
04h	Headphone Detect Complete	Indicates Headphone Detection status 0 = Headphone Detect not complete 1 = Headphone Detect complete

GPn_FN	DESCRIPTION	COMMENTS
05h	DSP1 DRC Signal Detect	Indicates DSP1 DRC Signal Detect status 0 = Normal 1 = Activity Detected
06h	DSP2 DRC Signal Detect	Indicates DSP2 DRC Signal Detect status 0 = Normal 1 = Activity Detected
07h	FIFO Error	Indicates a Digital Core FIFO Error condition 0 = Normal 1 = FIFO Error
08h	Write Sequencer Status	Indicates Write Sequencer status 0 = Sequencer Busy (sequence in progress) 1 = Sequencer Idle
09h	DCS_01 Done	Indicates DC Servo status on HPOUT1L and HPOUT1R 0 = DC Servo not complete 1 = DC Servo complete
0Ah	DCS_23 Done	Indicates DC Servo status on HPOUT2L and HPOUT2R 0 = DC Servo not complete 1 = DC Servo complete
0Bh	FLL Clock Switch	Indicates FLL Clock Switch status 0 = FLL Clock Switch not complete (transition in progress) 1 = FLL Clock Switch complete
0Ch	FLL Lock	Indicates FLL Lock status 0 = Not locked 1 = Locked
0Dh	OPCLK Clock Output	GPIO Clock derived from SYSCLK
0Eh	FLL Clock Output	Clock output from FLL
0Fh to 1Fh	Reserved	

Table 53 GPIO Function Select

BUTTON DETECT (GPIO INPUT)

Button detect functionality can be selected on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. The same functionality can be used to support a Jack Detect input function.

It is recommended to enable the GPIO input de-bounce feature when using GPIOs as button input or Jack Detect input.

The GPn_LVL fields may be read to determine the logic levels on a GPIO input, after the selectable de-bounce controls. Note that GPn_LVL is not affected by the GPn_POL bit.

The de-bounced GPIO signals are also inputs to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edge of the GPIO input. The associated interrupt bits are latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

LOGIC ‘1’ AND LOGIC ‘0’ OUTPUT (GPIO OUTPUT)

The WM8915 can be programmed to drive a logic high or logic low level on any GPIO pin by selecting the “GPIO Output” function as described in “GPIO Control”. The output logic level is selected using the respective GPn_LVL bit.

Note that the polarity of the GPIO output can be inverted using the GPn_POL registers. If GPn_POL = 1, then the external output will be the opposite logic level to GPn_LVL.

INTERRUPT (IRQ) STATUS OUTPUT

The WM8915 has an Interrupt Controller which can be used to indicate when any selected Interrupt events occur. An interrupt can be generated by any of the events described throughout the GPIO function definition above. Individual interrupts may be masked in order to configure the Interrupt as required. See “Interrupts” for further details.

The Interrupt (IRQ) status may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

MICROPHONE ACCESSORY STATUS DETECTION

The WM8915 provides an impedance measurement circuit on the MICDET pin to detect the connection of a microphone or other external accessory. See “External Accessory Detection” for further details.

A logic signal from the microphone detect circuit may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This logic signal is set high for a single pulse duration of 31µs whenever an accessory insertion, removal or impedance change is detected.

The microphone detection circuit is also an input to the Interrupt control circuit. An interrupt event is triggered whenever an accessory insertion, removal or impedance change is detected. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

HEADPHONE ACCESSORY STATUS DETECTION

The WM8915 provides a headphone detection circuit on the HPDETL and HPDETR pins to measure the impedance of an external load connected to the headphone outputs. See “External Accessory Detection” for further details.

A logic signal from the headphone detection circuit may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This logic signal is set low when a Headphone Detect measurement is triggered, and is set high when the Headphone Detect function has completed. A rising edge indicates completion of a Headphone Detect measurement.

The headphone detection circuit is also an input to the Interrupt control circuit. An interrupt event is triggered whenever a headphone detection measurement has completed. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

DYNAMIC RANGE CONTROL (DRC) SIGNAL ACTIVITY DETECTION

Signal activity detection is provided on the Dynamic Range Controllers (DRCs). These may be configured to indicate when a signal is present on the respective signal path (DSP1 or DSP2). The signal activity status signals may be used to control other events if required. See “Digital Core Architecture” for more details of the DRCs and the available digital signal paths.

When a DRC is enabled, as described in “Dynamic Range Control (DRC)”, then signal activity detection can be enabled by setting the respective DSP*n*DRC_SIG_DET register bit. The applicable threshold can be defined either as a Peak level (Crest Factor) or an RMS level, depending on the DSP*n*DRC_SIG_DET_MODE register bit. When Peak level is selected, the threshold is determined by DSP*n*DRC_SIG_DET_PK, which defines the applicable Crest Factor (Peak to RMS ratio) threshold. If RMS level is selected, then the threshold is set using DSP*n*DRC_SIG_DET_RMS. These register fields are set independently for each of the Dynamic Range Controllers, as described in Table 54.

The DRC Signal Detect signals may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The DRC Signal Detect signals are inputs to the Interrupt control circuit. An interrupt event is triggered on the rising edge of the DRC Signal Detect signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1088 (0440h) DSP1 DRC (1)	15:11	DSP1DRC_SIG_DET_RMS [4:0]	00000	DSP1 DRC Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when DSP1DRC_SIG_DET_MODE=1. 00000 = -30dB 00001 = -31.5dB …. (1.5dB steps) 11110 = -75dB 11111 = -76.5dB
	10:9	DSP1DRC_SIG_DET_PK [1:0]	00	DSP1 DRC Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when DSP1DRC_SIG_DET_MODE=0. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7	DSP1DRC_SIG_DET_MODE	0	DSP1 DRC Signal Detect Mode 0 = Peak threshold mode 1 = RMS threshold mode
	6	DSP1DRC_SIG_DET	0	DSP1 DRC Signal Detect Enable 0 = Disabled 1 = Enabled
R1344 (0550h) DSP2 DRC (1)	15:11	DSP2DRC_SIG_DET_RMS [4:0]	00000	DSP2 DRC Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when DSP2DRC_SIG_DET_MODE=1. 00000 = -30dB 00001 = -31.5dB …. (1.5dB steps) 11110 = -75dB 11111 = -76.5dB
	10:9	DSP2DRC_SIG_DET_PK [1:0]	00	DSP2 DRC Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when DSP2DRC_SIG_DET_MODE=0. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7	DSP2DRC_SIG_DET_MODE	0	DSP2 DRC Signal Detect Mode 0 = Peak threshold mode 1 = RMS threshold mode
	6	DSP2DRC_SIG_DET	0	DSP2 DRC Signal Detect Enable 0 = Disabled 1 = Enabled

Table 54 DRC Signal Activity Detect GPIO/Interrupt Control

DIGITAL CORE FIFO ERROR STATUS OUTPUT

The WM8915 monitors the Digital Core for error conditions which may occur if a clock rate mismatch is detected. Under these conditions, the digital audio may become corrupted.

The most likely cause of a Digital Core FIFO Error condition is an incorrect system clocking configuration. See “Clocking and Sample Rates” for the WM8915 system clocking requirements.

The Digital Core FIFO Error function is provided in order that the system configuration can be verified during product development.

The FIFO Error signal may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The FIFO Error signal is an input to the Interrupt control circuit. An interrupt event is triggered on the rising edge of the FIFO Error signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

CONTROL WRITE SEQUENCER STATUS OUTPUT

The WM8915 Control Write Sequencer (WSEQ) can be used to execute a sequence of register write operations in response to a simple trigger event. When the Control Write Sequencer is executing a sequence, normal access to the register map via the Control Interface is restricted. See “Control Write Sequencer” for details of the Control Write Sequencer.

The WM8915 generates a signal indicating the status of the Control Write Sequencer, in order to signal to the host processor whether the Control Interface functionality is restricted due to an ongoing Control Sequence. The WSEQ_DONE flag register indicates whether the sequencer is idle, or if it is currently executing a Control Write sequence.

The Write Sequencer status may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The Write Sequencer status is an input to the Interrupt control circuit. An interrupt event is triggered on completion of a Control Sequence. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

DC SERVO COMPLETE STATUS OUTPUT

The WM8915 DC Servo can be used to remove DC offsets from the ground-referenced headphone outputs. The offset correction process can be commanded in a number of different ways, as described in “DC Servo”.

The DC Servo Start-Up mode is commanded by writing a logic 1 to DCS_TRIG_STARTUP_*n*. The DC Servo DAC Write mode is commanded by writing a logic 1 to DCS_TRIG_DAC_WR_*n*. Completion of either of these DC Servo modes is indicated in the DCS_CAL_COMPLETE register as described in Table 45.

The DC Servo status may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The “DCS_01 DONE” output is asserted when the DC Servo is enabled on HPOUT1L and HPOUT1R and the DC Servo Start-Up or DAC Write mode has completed on both channels.

The “DCS_23 DONE” output is asserted when the DC Servo is enabled on HPOUT2L and HPOUT2R and the DC Servo Start-Up or DAC Write mode has completed on both channels.

The associated logic is illustrated in Figure 29. Note that, if the DC Servo is not enabled on any channel, then the “DCS Done” indication for that channel is set as if it had completed.

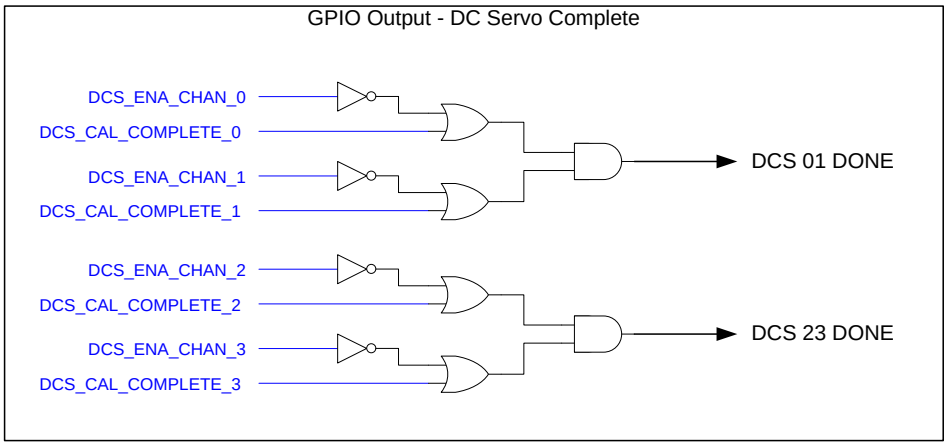


Figure 29 DC Servo Complete Status Output

The DC Servo status is an input to the Interrupt control circuit. An interrupt event is triggered on the rising edge of the DC Servo Complete signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

FREQUENCY LOCKED LOOP (FLL) CLOCK SWITCH STATUS OUTPUT

The WM8915 supports glitch-free transition between input reference clocks (provided that the selected output frequency is not changed). The internal signal indicating the FLL Clock Switch transition status may be used externally to monitor the FLL status. See “Clocking and Sample Rates” for more details of the FLL.

The FLL Clock Switch signal may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The FLL Clock Switch is an input to the Interrupt control circuit. An interrupt event is triggered on the rising edge of the FLL Clock Switch signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

FREQUENCY LOCKED LOOP (FLL) LOCK STATUS OUTPUT

The WM8915 maintains a flag indicating the lock status of the FLL; this flag may be used to control other events if required. See “Clocking and Sample Rates” for more details of the FLL.

The FLL Lock signal may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The FLL Lock signal is an input to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edges of the FLL Lock signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

OPCLK CLOCK OUTPUT

A clock output (OPCLK) derived from SYSCLK may be output on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This clock is enabled by register bit OPCLK_ENA, and its frequency is controlled by OPCLK_DIV.

See “Clocking and Sample Rates” for more details of the System Clock (SYSCLK).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (0002h) Power Management (2)	11	OPCLK_ENA	0b	GPIO Clock Output (OPCLK) Enable 0 = Disabled 1 = Enabled
R521 (0209h) Clocking 1	2:0	OPCLK_DIV	000	GPIO Output Clock (OPCLK) Divider 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16

Table 55 OPCLK Control

FLL CLOCK OUTPUT

The FLL Clock output may be output directly on any GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

See “Clocking and Sample Rates” for more details of the WM8915 system clocking and for details of how to enable and configure the Frequency Locked Loop.

INTERRUPTS

The Interrupt Controller has multiple inputs. These include the GPIO input pins, the accessory detection circuits, FLL Lock circuits, Microphone activity detection, Digital FIFO error detection and the Write Sequencer status flag. Any combination of these inputs can be used to trigger an Interrupt (IRQ) event.

There is an Interrupt Status field associated with each of the IRQ inputs. These fields are asserted whenever a logic edge is detected on the respective input. Some inputs are triggered on rising edges only; some are triggered on both edges, as noted in Table 56. The Interrupt Status fields are held in Registers R1840 and R1841. The status of these Interrupt flags can be read at any time from these registers, or else in response to the Interrupt (IRQ) output being signalled via a GPIO pin.

All of the Interrupt Status fields are edge-triggered, as noted above. Many of these are triggered on both the rising and falling edges and, therefore, the Interrupt Status fields cannot indicate which edge has been detected. The “Raw Status” fields in Register R1842 provide readback of the current value of selected Interrupt input signals. Note that the logic levels of any GPIO inputs can be read using the GPn_LVL registers, as described in Table 52.

Individual mask bits can select or deselect different functions from the Interrupt controller. These are listed within the Interrupt Status Mask registers, as described in Table 56. Note that the Interrupt Status fields remain valid, even when masked, but the masked bits will not cause the Interrupt (IRQ) output to be asserted.

The Interrupt (IRQ) output represents the logical ‘OR’ of all the unmasked IRQ inputs. The bits within the Interrupt Status registers are latching fields and, once they are set, they are not reset until a ‘1’ is written to the respective register bit in the Interrupt Status register(s). The Interrupt (IRQ) output is not reset until each of the unmasked IRQ inputs has been reset.

De-bouncing of the GPIO inputs can be enabled using the register bits described in Table 52. This is enabled by default on all GPIO inputs, in order to avoid false detections.

The Interrupt (IRQ) output can be globally masked by setting the IM_IRQ register. Under default conditions, the Interrupt (IRQ) is not masked.

The Interrupt (IRQ) flag may be output on a GPIO pin - see “General Purpose Input/Output”.

The Interrupt Controller register fields are described in Table 56.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1840 (0730h) Interrupt Status 1	4	GP5_EINT	0	GPIO5 Interrupt status (Rising and falling edge triggered) Note: Cleared when a ‘1’ is written.
	3	GP4_EINT	0	GPIO4 Interrupt status (Rising and falling edge triggered) Note: Cleared when a ‘1’ is written.
	2	GP3_EINT	0	GPIO3 Interrupt status (Rising and falling edge triggered) Note: Cleared when a ‘1’ is written.
	1	GP2_EINT	0	GPIO2 Interrupt status (Rising and falling edge triggered) Note: Cleared when a ‘1’ is written.
	0	GP1_EINT	0	GPIO1 Interrupt status (Rising and falling edge triggered) Note: Cleared when a ‘1’ is written.
R1841 (0731h) Interrupt Status 2	12	DCS_DONE_23_EINT	0	DC Servo Channels 2,3 IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.
	11	DCS_DONE_01_EINT	0	DC Servo Channels 0,1 IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.
	10	WSEQ_DONE_EINT	0	Write Sequencer IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.
	9	FIFOS_ERR_EINT	0	Digital Core FIFO Error IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.
	7	DSP2DRC_SIG_DET_EINT	0	DSP2 DRC Signal Detect IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.
	6	DSP1DRC_SIG_DET_EINT	0	DSP1 DRC Signal Detect IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.
	3	FLL_SW_CLK_DONE_EINT	0	FLL Clock Switch IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.
	2	FLL_LOCK_EINT	0	FLL Lock IRQ status (Rising and falling edge triggered) Note: Cleared when a ‘1’ is written.
	1	HP_DONE_EINT	0	Headphone Detection IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.
	0	MICD_EINT	0	Microphone Detection IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.
R1842 (0732h) Interrupt Raw Status 2	12	DCS_DONE_23_STS	0	DC Servo Channels 2,3 (HPOUT2L and HPOUT2R) status 0 = DC Servo not complete 1 = DC Servo complete

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	11	DCS_DONE_01_STS	0	DC Servo Channels 0,1 (HPOUT1L and HPOUT1R) status 0 = DC Servo not complete 1 = DC Servo complete
	10	WSEQ_DONE_STS	0	Write Sequencer status 0 = Sequencer Busy (sequence in progress) 1 = Sequencer Idle
	9	FIFOS_ERR_STS	0	Digital Core FIFO Error status 0 = Normal 1 = FIFO Error
	7	DSP2DRC_SIG_DET_STS	0	DSP2 DRC Signal Detect status 0 = Normal 1 = Activity Detected
	6	DSP1DRC_SIG_DET_STS	0	DSP1 DRC Signal Detect status 0 = Normal 1 = Activity Detected
	2	FLL_LOCK_STS	0	FLL Lock status 0 = Not locked 1 = Locked
R1848 (0738h) Interrupt Status 1 Mask	4	IM_GP5_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	3	IM_GP4_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	2	IM_GP3_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	1	IM_GP2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	0	IM_GP1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
R1849 (0739h) Interrupt Status 2 Mask	12	IM_DCS_DONE_23_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	11	IM_DCS_DONE_01_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	10	IM_WSEQ_DONE_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	9	IM_FIFOS_ERR_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	7	IM_DSP2DRC_SIG_DET_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	6	IM_DSP1DRC_SIG_DET_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	3	IM_FLL_SW_CLK_DONE_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	2	IM_FLL_LOCK_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	1	IM_HP_DONE_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	0	IM_MICD_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
R1856 (0740h) Interrupt Control	0	IM_IRQ	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 56 Interrupt Configuration

DIGITAL AUDIO INTERFACE

The WM8915 provides digital audio interfaces for inputting DAC playback data and for outputting ADC or Digital Microphone data. Flexible routing options also allow digital audio to be switched or mixed between interfaces without involving any of the DAC or ADC signal paths.

The WM8915 provides two audio interfaces, AIF1 and AIF2. Each of these is independently configurable on the respective transmit (TX) and receive (RX) paths. AIF1 supports up to 3 stereo pairs of input and output signal paths; AIF2 supports 1 stereo pair of input and output signal paths.

The digital audio interfaces provide a flexible capability to support different data formats and different audio sample rates. In the case of AIF1, it is possible to support different sample rates simultaneously on any of the input or output paths.

The DSP1 and DSP2 output signal paths can each be routed to one of the AIF1 TX signal paths and/or the AIF2 TX signal paths. The DSP1 and DSP2 input signal paths take their input from one of the AIF1 RX or AIF2 RX signal paths.

Each of the digital audio interfaces uses five pins:

- ADCDAT: Data output for ADC / Digital Microphone
- ADCLRCLK: Left/Right data alignment clock for ADC / Digital Microphone
- DACDAT: Data input for DAC signal paths
- DACLRCLK: Left/Right data alignment clock for DAC signal paths
- BCLK: Bit clock, for synchronisation

In master interface mode, the clock signals BCLK, DACLRCLK and ADCLRCLK are outputs from the WM8915. In slave mode, these signals are inputs, as illustrated below.

As an option, the DACLRCLK pin can be used to provide clocking for both the ADCDAT output and the DACDAT input signal paths.

Four different audio data formats are supported each digital audio interface:

- I^2S
- Left Justified
- DSP mode A
- DSP mode B

The Left Justified and DSP-B modes are valid in Master mode only (ie. BCLK and LRCLK are outputs from the WM8915). These modes cannot be supported in Slave mode.

All four of these modes are MSB first. Data words are encoded in 2's complement format. Each of the audio interface modes is described in the following sections. Refer to the "Electrical Characteristics" section for timing information.

Two variants of DSP mode are supported - 'Mode A' and 'Mode B'. Mono PCM operation can be supported using the DSP modes.

MASTER AND SLAVE MODE OPERATION

The WM8915 digital audio interfaces can operate as a master or slave as shown in Figure 30 and Figure 31.

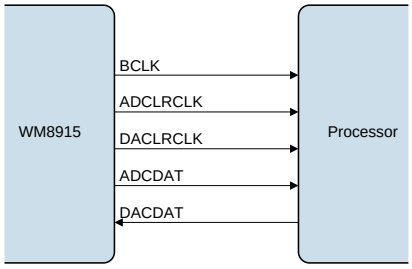


Figure 30 Master Mode

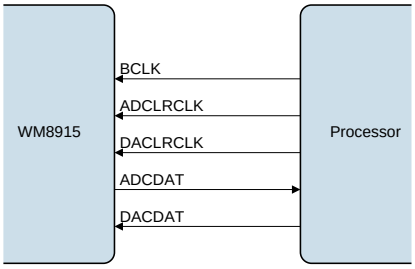


Figure 31 Slave Mode

AUDIO DATA FORMATS

The WM8915 digital audio interfaces AIF1 and AIF2 can be configured to operate in I^2S, Left-Justified, DSP-A or DSP-B interface modes. Note that Left-Justified and DSP-B modes are valid in Master mode only (ie. BCLK and LRCLK are outputs from the WM8915).

The digital audio interfaces AIF1 and AIF2 also provide flexibility to support multiple 'slots' of audio data within each LRCLK frame. This flexibility allows multiple pairs of audio channels to be supported (on AIF1 only) and also allows each interface to carry multiple samples of any audio channel(s) within a single LRCLK frame.

The data formats described in this section are generic descriptions, assuming only one stereo pair of audio samples per LRCLK frame. In these cases, the AIF is configured to transmit (or receive) in the first available position in each frame (ie. the Slot 0 position).

The options for multi-channel operation and mixed sample rates are described in the following section ("AIF Timeslot Configuration").

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In master mode, the LRCLK output will resemble the frame pulse shown in Figure 32 and Figure 33. In slave mode, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse.

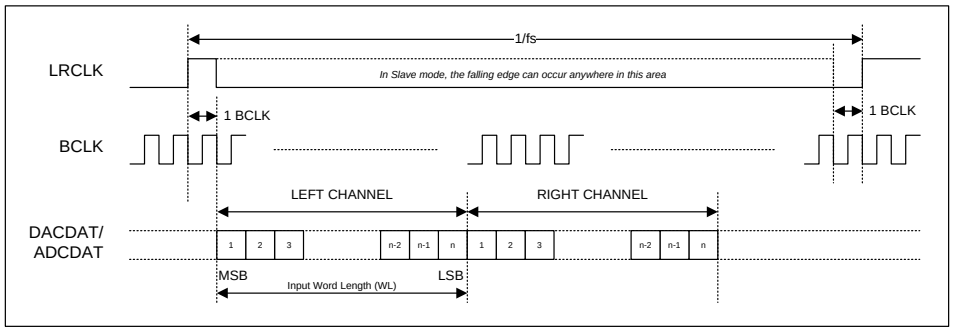


Figure 32 DSP Mode A Data Format

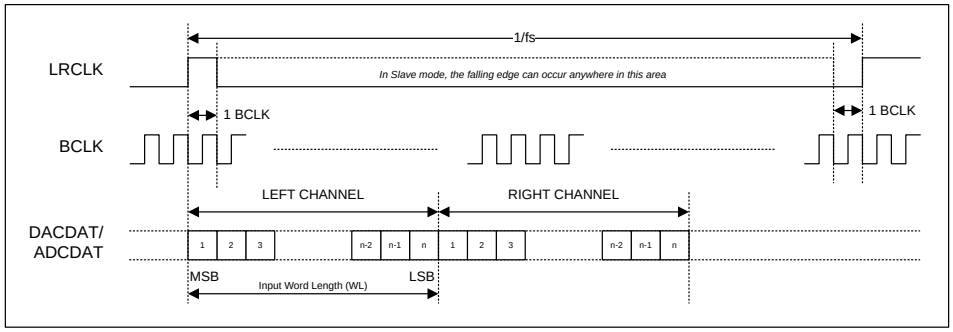


Figure 33 DSP Mode B Data Format

PCM operation is supported in DSP interface mode. WM8915 ADC or Digital Microphone data that is output on the Left Channel will be read as mono PCM data by the receiving equipment. Mono PCM data received by the WM8915 will be treated as Left Channel data. This data may be routed to the Left/Right DACs using the control fields described in the "Digital Mixing" and "Digital Audio Interface Control" sections.

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

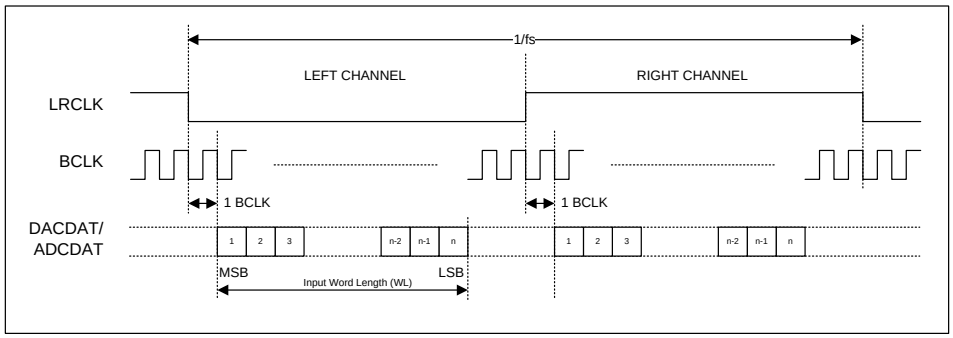


Figure 34 I2S Data Format (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

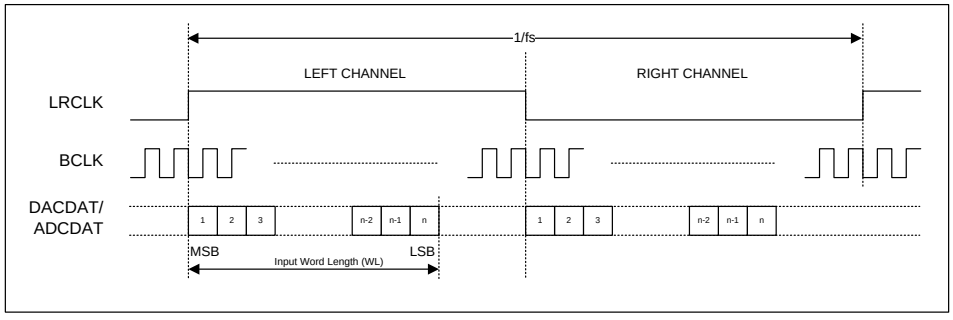


Figure 35 Left Justified Data Format (assuming n-bit word length)

AIF TIMESLOT CONFIGURATION

Digital audio interface AIF1 supports multi-channel operation; up to 3 stereo input channels and 3 stereo output channels can be supported simultaneously. Mixed sample rates are also possible, by allowing a configurable number of audio samples per frame. For example, an 8kHz channel (A) can be supported alongside a 48kHz channel (B) by accommodating 6 samples of channel B for each 1 sample of channel A data.

AIF2 also provides flexible configuration options, but supports only 1 stereo input pair and 1 stereo output pair.

Note that, in each of the interfaces, both sides of each stereo pair must operate at the same sample rate. Note that all the sample rates on AIF1 and AIF2 must be integer-related: the SYSCLK frequency will support 48kHz (and related) sample rates or 44.1kHz (and related) sample rates, but not both together. It is not possible to enable 44.1kHz and 48kHz audio data at the same time.

A high degree of flexibility is provided to define the position of the audio samples within each LRCLK frame; the audio channels may be interleaved, or back-to-back, or arranged in any order within the frame.

Each of the audio channels can be enabled or disabled independently on the transmit (TX) and receive (RX) signal paths.

For each enabled channel, the audio samples are assigned to one or more slots within the LRCLK frame. The applicable slots are defined by setting the Start Slot, the Slot Spacing, and the Number of Slots; these parameters are independently configured for each enabled channel.

There is no requirement to assign every available timeslot to an audio sample; some slots may be left unused if desired. Care is required, however, to ensure that no timeslot is allocated to more than one audio channel. The WM8915 provides error status flags which indicate if a configuration error has been detected (ie. if there is contention amongst the timeslot allocations).

The number of BCLK cycles within a slot is configurable; this is the Slot Length. The number of valid data bits within a slot is also configurable; this is the Word Length. It is required that there are enough BCLK cycles within each LRCLK frame to transmit or receive all of the enabled audio channels. Note that the transmit (TX) and receive (RX) sides of the AIF1 and AIF2 are all independently configurable.

Examples of the AIF Timeslot Configurations are illustrated in Figure 36 to Figure 39. One example is shown for each of the four possible data formats.

Figure 36 shows an example of DSP Mode A format. Channels 0 and 1 are allocated 3 timeslots each, whilst channels 2 and 3 are allocated 1 timeslot per LRCLK frame. This configuration would be suitable for 48kHz data (channel 0 and 1) and 16kHz data (channel 2 and 3).

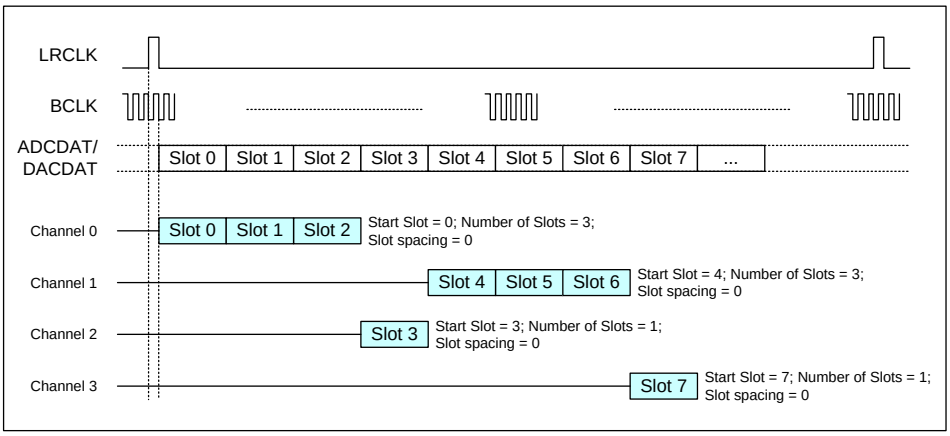


Figure 36 DSP Mode A Example

Figure 37 shows an example of DSP Mode B format. Channels 0 and 1 are allocated 2 timeslots each, whilst channels 2 and 3 are allocated 1 timeslot per LRCLK frame. This configuration would be suitable for 16kHz data (channel 0 and 1) and 8kHz data (channel 2 and 3).

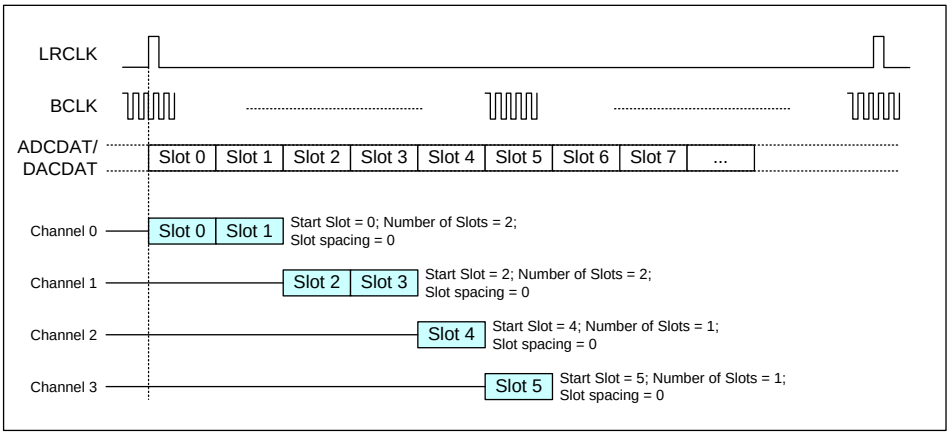


Figure 37 DSP Mode B Example

Figure 38 shows an example of I2S format. Channels 0, 1, 2 and 3 are each allocated 1 timeslot per LRCLK frame. This configuration would be suitable for four audio channels at the same sample rate.

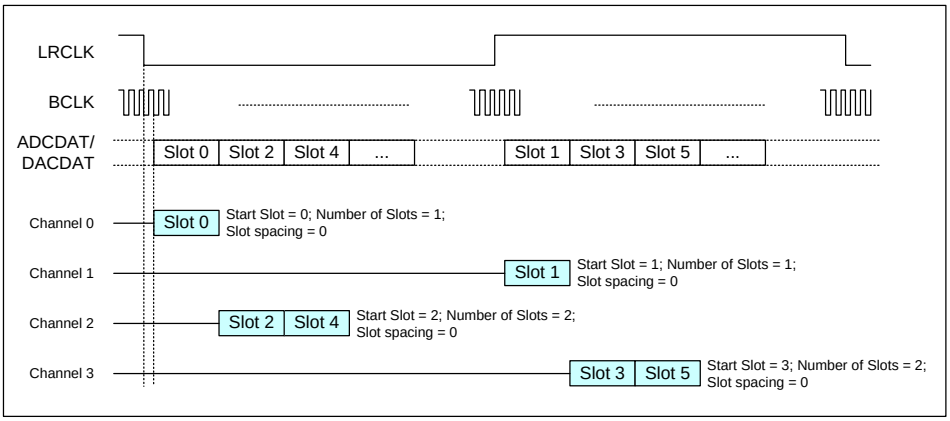


Figure 38 I2S Example

Figure 39 shows an example of Left Justified format. Channels 0 and 1 are allocated 1 timeslot each, whilst channels 2 and 3 are allocated 2 timeslots per LRCLK frame. This configuration would be suitable for 16kHz data (channel 0 and 1) and 32kHz data (channel 2 and 3).

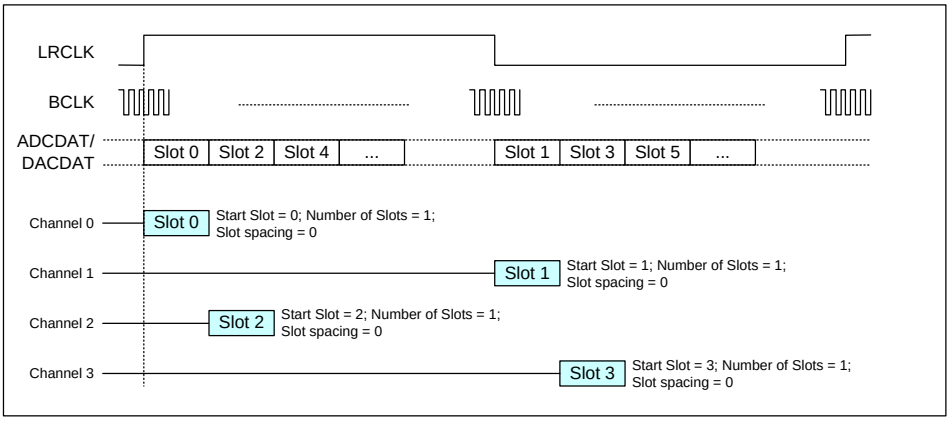


Figure 39 Left Justifed Example

TDM OPERATION BETWEEN THREE OR MORE DEVICES

The AIF operation described above illustrates how multiple audio channels can be interleaved on a single ADCDAT or DACDAT pin. The interface uses Time Division Multiplexing (TDM) to allocate time periods to each of the audio channels in turn.

In its simplest form, TDM is implemented between two devices, using the electrical connections illustrated in Figure 30 or Figure 31.

It is also possible to implement TDM between three or more devices. This allows one CODEC to receive audio data from two other devices simultaneously on a single audio interface, as illustrated in Figure 40, Figure 41 and Figure 42.

The WM8915 provides full support for TDM operation. The ADCDAT can be tri-stated when not transmitting data, in order to allow other devices to transmit on the same wire. The behaviour of the ADCDAT pin is configurable, to allow maximum flexibility to interface with other devices in this way.

Typical configurations of TDM operation between three devices are illustrated in Figure 40, Figure 41 and Figure 42.

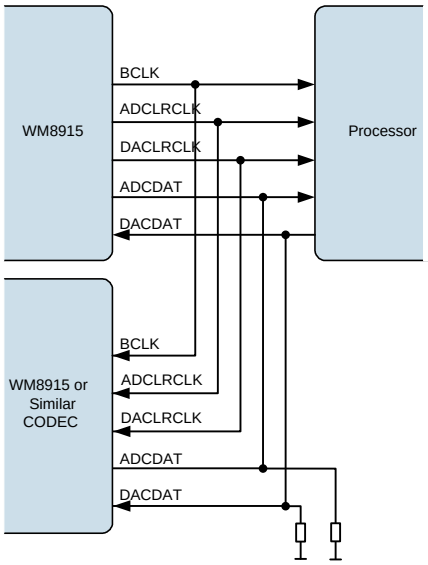


Figure 40 TDM with WM8915 as Master

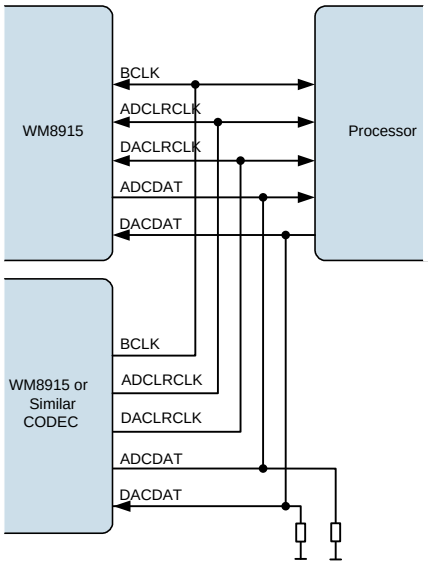


Figure 41 TDM with Other CODEC as Master

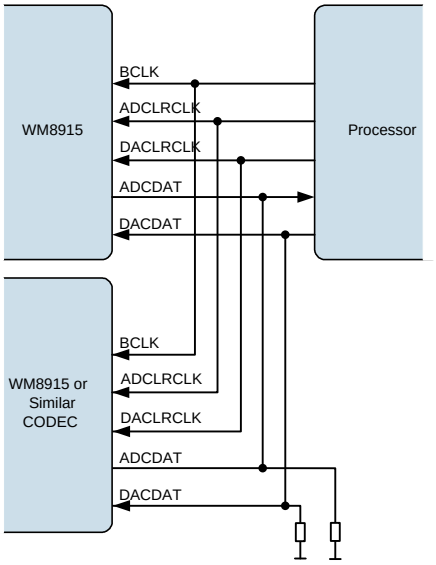


Figure 42 TDM with Processor as Master

Note: The WM8915 is a 24-bit device. If the user operates the WM8915 in 32-bit mode then the 8 LSBs will be ignored on the receiving side and not driven on the transmitting side. It is therefore recommended to add a pull-down resistor if necessary to the DACDAT line and the ADCDAT line in TDM mode.

DIGITAL AUDIO INTERFACE CONTROL

This section describes the configuration of the WM8915 digital audio interface paths.

AIF1 supports up to 3 stereo pairs of input and output signal paths; AIF2 supports 1 stereo pair of input and output signal paths. Each interface can be configured as Master or Slave using the BCLK and LRCLK controls; mixed master/slave configurations are also possible.

Each input and output signal path can be independently enabled or disabled. The AIF output (digital record) and AIF input (digital playback) paths can use a common LRCLK frame clock, or can use separate DACLRCLK and ADCLRCLK signals if required.

Each interface supports flexible data formats, selectable word-length, channel inversion, mono mode, dithering and tri-state control.

The digital audio interface signal paths are illustrated in Figure 43.

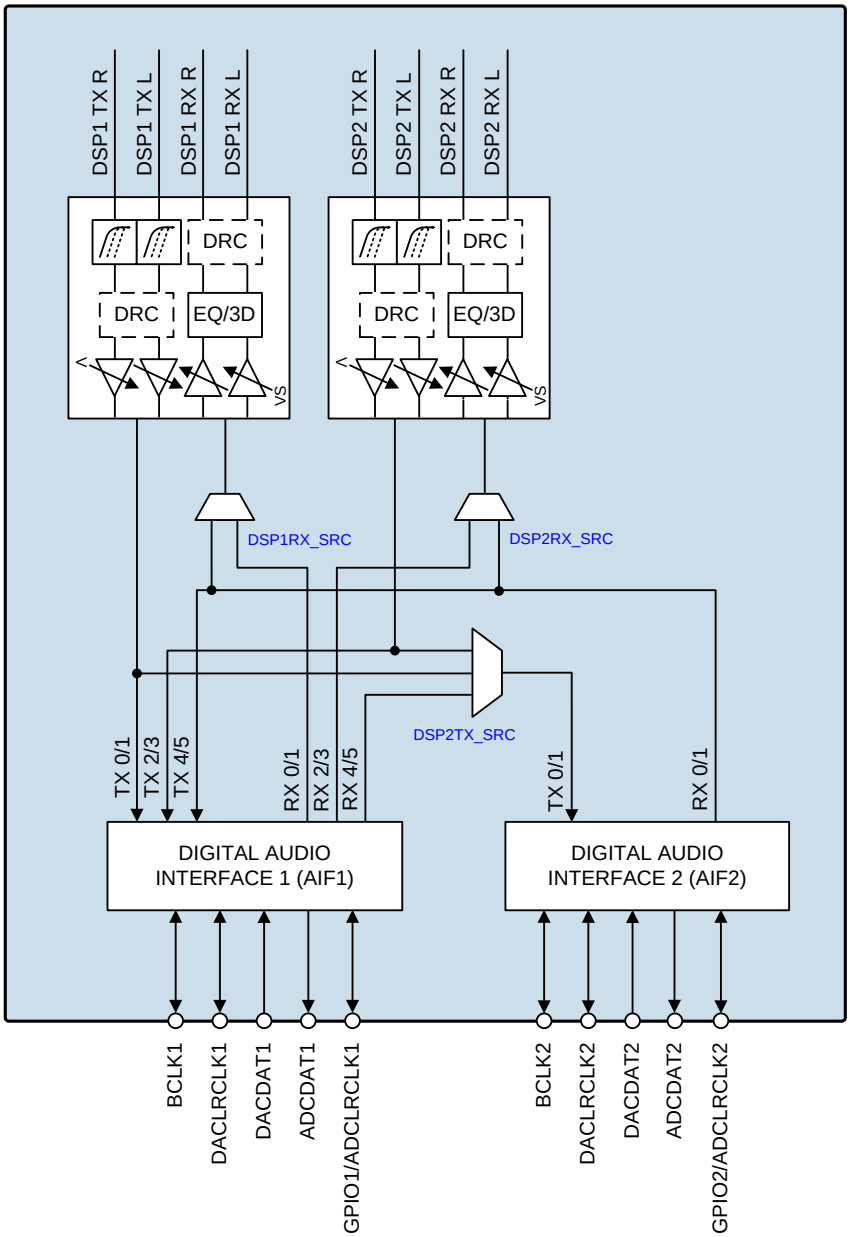


Figure 43 Digital Audio Interface Signal Paths

AIF1 / DSP1 SIGNAL PATHS ENABLE

The AIF1 interface supports up to 6 input channels and up to 6 output channels. Each of these channels can be enabled or disabled using the register bits defined in Table 57.

The AIF1 output channels 0 and 1 are sourced from the DSP1 output signals.

The AIF1 output channels 2 and 3 are sourced from the DSP2 output signals.

The AIF1 output channels 4 and 5 are sourced from the AIF2 input channels.

The DSP1 input signal paths may be sourced from AIF1 input channels 0 and 1, or else from AIF2 input channels 0 and 1. This is selected using the DSP1RX_SRC register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (0003h) Power Management (3)	9	DSP1RXL_ENA	0	Enable DSP1 (Left) input path 0 = Disabled 1 = Enabled
	8	DSP1RXR_ENA	0	Enable DSP1 (Right) input path 0 = Disabled 1 = Enabled
R4 (0004h) Power Management (4)	5	AIF1RX_CHAN5_ENA	0	Enable AIF1 input channel 5 0 = Disabled 1 = Enabled
	4	AIF1RX_CHAN4_ENA	0	Enable AIF1 input channel 4 0 = Disabled 1 = Enabled
	3	AIF1RX_CHAN3_ENA	0	Enable AIF1 input channel 3 0 = Disabled 1 = Enabled
	2	AIF1RX_CHAN2_ENA	0	Enable AIF1 input channel 2 0 = Disabled 1 = Enabled
	1	AIF1RX_CHAN1_ENA	0	Enable AIF1 input channel 1 0 = Disabled 1 = Enabled
	0	AIF1RX_CHAN0_ENA	0	Enable AIF1 input channel 0 0 = Disabled 1 = Enabled
R5 (0005h) Power Management (5)	9	DSP1TXL_ENA	0	Enable DSP1 (Left) output path 0 = Disabled 1 = Enabled
	8	DSP1TXR_ENA	0	Enable DSP1 (Right) output path 0 = Disabled 1 = Enabled
R6 (0006h) Power Management (6)	5	AIF1TX_CHAN5_ENA	0	Enable AIF1 output channel 5 0 = Disabled 1 = Enabled
	4	AIF1TX_CHAN4_ENA	0	Enable AIF1 output channel 4 0 = Disabled 1 = Enabled
	3	AIF1TX_CHAN3_ENA	0	Enable AIF1 output channel 3 0 = Disabled 1 = Enabled
	2	AIF1TX_CHAN2_ENA	0	Enable AIF1 output channel 2 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	AIF1TX_CHAN1_ENA	0	Enable AIF1 output channel 1 0 = Disabled 1 = Enabled
	0	AIF1TX_CHAN0_ENA	0	Enable AIF1 output channel 0 0 = Disabled 1 = Enabled
R8 (0008h) Power Management (8)	0	DSP1RX_SRC	0	Selects source for DSP1 input 0 = AIF1 input (channels 0 and 1) 1 = AIF2 input

Table 57 AIF1 / DSP1 Signal Paths Enable

AIF1 - BCLK AND LRCLK CONTROL

The AIF1 interface bit rate is controlled by the BCLK1 frequency. In Master mode, BCLK1 is an output from the WM8915; in Slave mode, BCLK1 is an input to the WM8915. Master mode is selected for the BCLK1 pin by setting the AIF1_BCLK_MSTR bit.

In Master mode, the BCLK1 frequency is controlled relative to AIFCLK by the AIF1_BCLK_DIV divider. (Note that AIFCLK is the same frequency as SYSCLK; it is enabled using AIFCLK_ENA. See “Clocking and Sample Rates” for details of the system clocks.)

In Master mode, the BCLK1 output is generated by the WM8915 when any of the AIF1 channels is enabled. In Slave mode, the BCLK1 output is disabled by default to allow another digital audio interface to drive this pin.

It is also possible to force the BCLK1 signal to be output, using the AIF1_BCLK_FRC bit, allowing mixed master and slave modes. When AIF1_BCLK_FRC is set, the BCLK1 signal is generated at all times in Master and Slave modes.

The BCLK1 signal can be inverted in Master or Slave modes using the AIF1_BCLK_INV register.

The AIF1 input uses the DACLRCLK1 signal to define the start of each frame of input (DACDAT1) data. In Master mode, DACLRCLK1 is an output from the WM8915; in Slave mode, DACLRCLK1 is an input to the WM8915. Master mode is selected for the DACLRCLK1 pin by setting the AIF1RX_LRCLK_MSTR bit.

In Master mode, the DACLRCLK1 frequency is controlled relative to BCLK1 by the AIF1RX_RATE divider.

In Master mode, the DACLRCLK1 output is generated by the WM8915 when any of the AIF1 channels is enabled. (Note that, when GPIO1 is configured as ADCLRCLK1, then only the AIF1 RX/input channels will cause DACLRCLK1 to be output.)

In Slave mode, the DACLRCLK1 output is disabled by default to allow another digital audio interface to drive this pin.

It is also possible to force the DACLRCLK1 signal to be output, using the AIF1RX_LRCLK_FRC bit, allowing mixed master and slave modes. When AIF1RX_LRCLK_FRC is set, the DACLRCLK1 signal is generated at all times in Master and Slave modes.

Note that the DACLRCLK1 signal is derived from BCLK1, and either an internal or external BCLK1 signal must be present to generate DACLRCLK1 output.

The DACLRCLK1 signal can be inverted in Master or Slave modes using the AIF1RX_LRCLK_INV register.

Under default conditions, the AIF1 output paths also use the DACLRCLK1 signal as the frame synchronisation clock. The AIF1 output interface uses a separate ADCLRCLK1 signal when selected using the AIF1TX_LRCLK_MODE bit.

The ADCLRCLK1 function must be selected on the GPIO1/ADCLRCLK1 pin as described in the “General Purpose Input/Output” section.

The ADCLRCLK1 pin can operate in Master or Slave mode, and is controlled similarly to the DACLRCLK1 function using the register bits described in Table 58.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R769 (0301h) AIF1 BCLK	10	AIF1_BCLK_INV	0	BCLK1 Invert 0 = BCLK1 not inverted 1 = BCLK1 inverted
	9	AIF1_BCLK_FRC	0	Force BCLK1 output in Master and Slave modes 0 = Normal 1 = BCLK1 enabled at all times (including when all AIF1 channels are disabled)
	8	AIF1_BCLK_MSTR	0	Select BCLK1 Master mode 0 = Slave Mode 1 = Master Mode
	3:0	AIF1_BCLK_DIV	0000	BCLK1 Rate 0000 = AIFCLK 0001 = AIFCLK / 2 0010 = AIFCLK / 3 0011 = AIFCLK / 4 0100 = AIFCLK / 6 0101 = AIFCLK / 8 0110 = AIFCLK / 12 0111 = AIFCLK / 16 1000 = AIFCLK / 24 1001 = AIFCLK / 32 1010 = AIFCLK / 48 1011 = AIFCLK / 64 1100 = AIFCLK / 96 1101 = AIFCLK / 96 1110 = AIFCLK / 96 1111 = AIFCLK / 96 All other codes are Reserved
R770 (0302h) AIF1 TX LRCLK(1)	10:0	AIF1TX_RATE [10:0]	080h	ADCLRCLK1 Rate ADCLRCLK1 clock output = BCLK1 / AIF1TX_RATE Integer (LSB = 1) Valid from 8..2047
R771 (0303h) AIF1 TX LRCLK(2)	3	AIF1TX_LRCLK_MODE	1	AIF1 output path LRCLK select 0 = Use ADCLRCLK1 1 = Use DACLRCLK1
	2	AIF1TX_LRCLK_INV	0	ADCLRCLK1 Invert 0 = ADCLRCLK1 not inverted 1 = ADCLRCLK1 inverted
	1	AIF1TX_LRCLK_FRC	0	Force ADCLRCLK1 output in Master and Slave modes 0 = Normal 1 = ADCLRCLK1 enabled at all times (including when all AIF1 channels are disabled) Note that an internal or external BCLK1 signal must be present for ADCLRCLK1 output.
	0	AIF1TX_LRCLK_MSTR	0	Select ADCLRCLK1 Master mode 0 = Slave Mode 1 = Master Mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R772 (0304h) AIF1 RX LRCLK(1)	10:0	AIF1RX_RATE [10:0]	080h	DACLRCLK1 Rate DACLRCLK1 clock output = BCLK1 / AIF1RX_RATE Integer (LSB = 1) Valid from 8..2047
R773 (0305h) AIF1 RX LRCLK	2	AIF1RX_LRCLK_INV	0	DACLRCLK1 Invert 0 = DACLRCLK1 not inverted 1 = DACLRCLK1 inverted
	1	AIF1RX_LRCLK_FRC	0	Force DACLRCLK1 output in Master and Slave modes 0 = Normal 1 = DACLRCLK1 enabled at all times (including when all AIF1 channels are disabled) Note that an internal or external BCLK1 signal must be present for DACLRCLK1 output.
	0	AIF1RX_LRCLK_MSTR	0	Select DACLRCLK1 Master mode 0 = Slave Mode 1 = Master Mode

Table 58 AIF1 BCLK and LRCLK Control

AIF1 - DIGITAL AUDIO DATA CONTROL

The register bits controlling the audio data format, slot lengths and word lengths for AIF1 are described in Table 59.

Note that Left-Justified and DSP-B modes are valid in Master mode only (ie. BCLK and LRCLK are outputs from the WM8915).

The AIF slot length is the number of BCLK cycles in one timeslot within the overall LRCLK frame. The word length is the number of valid data bits within each timeslot. (If the word length is less than the slot length, then there will be unused BCLK cycles at the end of each timeslot.) The AIF1 word length and slot length is independently selectable for the input (RX) and output (TX) paths.

For each AIF1 output (TX) channel, the number and position of the audio data samples within the ADCLRCLK1 frame is configurable.

The _START_SLOT registers define the timeslot position of the first audio sample for the associated audio channel. Valid selections are Slot 0 upwards. The timeslots are numbered as illustrated in Figure 32 through to Figure 35.

Note that, in DSP modes, the slots are arranged in numerical sequence from Slot 0 upwards. In I2S and LJ modes, all of the even-numbered slots occur before the odd-numbered slots.

The _SLOTS registers define how many audio data samples of the associated audio channel are present within the LRCLK frame. Valid selections are 1 or more.

The _SPACING registers define how many timeslots are present between successive audio samples of the associated audio channel. Valid selectsions are 0 upwards.

Note that, if there are no timeslots used by any audio channel, the associated audio channel must be disabled using the registers described in Table 57. In this case, the slot configuration registers for that channel will have no effect.

Each AIF1 input and output channel can be digitally inverted using the _DAT_INV registers.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R768 (0300h) AIF1 Control	1:0	AIF1_FMT [1:0]	10	AIF1 Digital Audio Interface Format 00 = DSP Mode A 01 = DSP Mode B 10 = I^2S mode 11 = Left Justified mode
R774 (0306h) AIF1TX Data Configuration (1)	15:8	AIF1TX_WL [7:0]	18h	AIF1 TX Word Length Coded as integer (LSB = 1) Default is 24 bits
	7:0	AIF1TX_SLOT_LEN [7:0]	18h	AIF1 TX Slot Length Coded as integer (LSB = 1) Default is 24 bits
R776 (0308h) AIF1RX Data Configuration	15:8	AIF1RX_WL [7:0]	18h	AIF1 RX Word Length Coded as integer (LSB = 1) Default is 24 bits
	7:0	AIF1RX_SLOT_LEN [7:0]	18h	AIF1 RX Slot Length Coded as integer (LSB = 1) Default is 24 bits
R777 (0309h) AIF1TX Channel 0 Configuration to R782 (030Eh) AIF1TX Channel 5 Configuration	15	AIF1TX_CHANn_DAT_INV	0	AIF1 TX Channel n Invert 0 = Not inverted 1 = Inverted
	14:9	AIF1TX_CHANn_SPACING [5:0]	00h	AIF1 TX Channel n Slot Spacing Defines the number of slots between successive samples of channel n Integer (LSB=1); Valid from 0 to 63
	8:6	AIF1TX_CHANn_SLOTS [2:0]	000	AIF1 TX Channel n Number of Slots Defines the number of audio samples of channel n within the LRCLK frame 000 = TX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1TX_CHANn_ENA = 1.
	5:0	AIF1TX_CHANn_START_SLOT [5:0]	00h	AIF1 TX Channel n Start Slot position Defines the timeslot position of the first audio sample of channel n Integer (LSB=1); Valid from 0 to 63
R783 (030Fh) AIF1RX Channel 0 Configuration to	15	AIF1RX_CHANn_DAT_INV	0	AIF1 RX Channel n Invert 0 = Not inverted 1 = Inverted
	14:9	AIF1RX_CHANn_SPACING [5:0]	00h	AIF1 RX Channel n Slot Spacing Defines the number of slots between successive samples of channel n Integer (LSB=1); Valid from 0 to 63

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R788 (0314h) AIF1RX Channel 5 Configuration	8:6	AIF1RX_CHANn_SLOTS [2:0]	000	AIF1 RX Channel n Number of Slots Defines the number of audio samples of channel n within the LRCLK frame 000 = RX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1RX_CHANn_ENA = 1.
	5:0	AIF1RX_CHANn_START_SLOT [5:0]	00h	AIF1 RX Channel n Start Slot position Defines the timeslot position of the first audio sample of channel n Integer (LSB=1); Valid from 0 to 63
Note: *n* is a number 0 to 5 that identifies the individual input or output channel.				

Table 59 AIF1 Digital Audio Data Control

AIF1 - MONO MODE AND DITHER CONTROL

A mono mode can be selected on the AIF1 input channels.

When AIF1RX_CHAN0_MONO_MODE is set, then the audio input on Channel 0 is copied onto input Channel 1. Note that AIF1RX_CHAN1_ENA must be set to 0 when the Channel 0 mono mode is selected.

When AIF1RX_CHAN2_MONO_MODE is set, then the audio input on Channel 2 is copied onto input Channel 3. Note that AIF1RX_CHAN3_ENA must be set to 0 when the Channel 2 mono mode is selected.

When AIF1RX_CHAN4_MONO_MODE is set, then the audio input on Channel 4 is copied onto input Channel 5. Note that AIF1RX_CHAN5_ENA must be set to 0 when the Channel 4 mono mode is selected.

Dithering is enabled by default in 16-bit mode. This function improves the accuracy of the AIF1 output channels when 16-bit word-length is selected. Dithering is not applied for other selections of the data word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R789 (0315h) AIF1 RX Mono Configuration	2	AIF1RX_CHAN4_MONO_MODE	0	AIF1 RX Channels 4-5 Mono Mode 0 = Disabled 1 = Enabled When enabled, then RX channel 4 is copied onto RX channel 5. Note that channel 5 must be disabled (AIF1RX_CHAN5_ENA = 0).
	1	AIF1RX_CHAN2_MONO_MODE	0	AIF1 RX Channels 2-3 Mono Mode 0 = Disabled 1 = Enabled When enabled, then RX channel 2 is copied onto RX channel 3. Note that channel 3 must be disabled (AIF1RX_CHAN3_ENA = 0).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	AIF1RX_CHAN0_MONO_MODE	0	AIF1 RX Channels 0-1 Mono Mode 0 = Disabled 1 = Enabled When enabled, then RX channel 0 is copied onto RX channel 1. Note that channel 1 must be disabled (AIF1RX_CHAN1_ENA = 0).
R794 (031Ah) AIF1TX Test	2	AIF1TX45_DITHER_ENA	1	AIF1 TX Channels 4-5 Dither 0 = Disabled 1 = Enabled in 16-bit mode
	1	AIF1TX23_DITHER_ENA	1	AIF1 TX Channels 2-3 Dither 0 = Disabled 1 = Enabled in 16-bit mode
	0	AIF1TX01_DITHER_ENA	1	AIF1 TX Channels 0-1 Dither 0 = Disabled 1 = Enabled in 16-bit mode

Table 60 AIF1 Mono Mode and Dither Control

AIF1 - TDM AND TRI-STATE CONTROL

The AIF1 output pins are tri-stated when the AIF1_TRI register is set. Note that, when the GPIO1/ADCLRCLK1 pin is configured as a GPIO, this pin is not affected by the AIF1_TRI register.

Under default conditions, the ADCDAT1 output is held a logic 0 when the WM8915 is not transmitting data (ie. during timeslots that are not enabled for output by the WM8915). When the AIF1TX_DAT_TRI is set, the WM8915 tri-states the ADCDAT1 pin when not transmitting data, allowing other devices to drive the ADCDAT1 connection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R768 (0300h) AIF1 Control	2	AIF1_TRI	0	AIF1 Tri-State Control 0 = Disabled (normal operation) 1 = Enabled (all AIF1 outputs tri-stated)
R775 (0307h) AIF1TX Data Configuration (2)	0	AIF1TX_DAT_TRI	0	ADCDAT1 Tri-State Control 0 = ADCDAT1 is logic 0 during disabled timeslots 1 = ADCDAT1 is tri-stated during disabled timeslots

Table 61 AIF1 TDM and Tri-State Control

AIF2 / DSP2 SIGNAL PATHS ENABLE

The AIF2 interface supports 2 input channels and 2 output channels. Each of these channels can be enabled or disabled using the register bits defined in Table 62.

The AIF2 output signal paths may be sourced from the DSP2 output signals, or from the DSP1 output signals, or from the AIF1 input channels 4 and 5. This is selected using the AIF2TX_SRC register.

The DSP2 input signal paths may be sourced from the AIF2 input channels, or else from AIF1 input channels 2 and 3. This is selected using the DSP2RX_SRC register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (0003h) Power Management (3)	11	DSP2RXL_ENA	0	Enable DSP2 (Left) input path 0 = Disabled 1 = Enabled
	10	DSP2RXR_ENA	0	Enable DSP2 (Right) input path 0 = Disabled 1 = Enabled
R4 (0004h) Power Management (4)	9	AIF2RX_CHAN1_ENA	0	Enable AIF2 input channel 1 0 = Disabled 1 = Enabled
	8	AIF2RX_CHAN0_ENA	0	Enable AIF2 input channel 0 0 = Disabled 1 = Enabled
R5 (0005h) Power Management (5)	11	DSP2TXL_ENA	0	Enable DSP2 (Left) output path 0 = Disabled 1 = Enabled
	10	DSP2TXR_ENA	0	Enable DSP2 (Right) output path 0 = Disabled 1 = Enabled
R6 (0006h) Power Management (6)	9	AIF2TX_CHAN1_ENA	0	Enable AIF2 output channel 1 0 = Disabled 1 = Enabled
	8	AIF2TX_CHAN1_ENA	0	Enable AIF2 output channel 0 0 = Disabled 1 = Enabled
R8 (0008h) Power Management (8)	7:6	AIF2TX_SRC [1:0]	00	Selects source for AIF2 output 00 = DSP2 output 01 = DSP1 output 10 = AIF1 input (channels 4 and 5) 11 = Reserved
	4	DSP2RX_SRC	0	Selects source for DSP2 input 0 = AIF2 input 1 = AIF1 input (channels 2 and 3)

Table 62 AIF2 / DSP2 Signal Paths Enable

AIF2 - BCLK AND LRCLK CONTROL

The AIF2 interface bit rate is controlled by the BCLK2 frequency. In Master mode, BCLK2 is an output from the WM8915; in Slave mode, BCLK2 is an input to the WM8915. Master mode is selected for the BCLK2 pin by setting the AIF2_BCLK_MSTR bit.

In Master mode, the BCLK2 frequency is controlled relative to AIFCLK by the AIF2_BCLK_DIV divider. (Note that AIFCLK is the same frequency as SYSCLK; it is enabled using AIFCLK_ENA. See “Clocking and Sample Rates” for details of the system clocks.)

In Master mode, the BCLK2 output is generated by the WM8915 when either of the AIF2 channels is enabled. In Slave mode, the BCLK2 output is disabled by default to allow another digital audio interface to drive this pin.

It is also possible to force the BCLK2 signal to be output, using the AIF2_BCLK_FRC bit, allowing mixed master and slave modes. When AIF2_BCLK_FRC is set, the BCLK2 signal is generated at all times in Master and Slave modes.

The BCLK2 signal can be inverted in Master or Slave modes using the AIF2_BCLK_INV register.

The AIF2 input uses the DACLRCLK2 signal to define the start of each frame of input (DACDAT2) data. In Master mode, DACLRCLK2 is an output from the WM8915; in Slave mode, DACLRCLK2 is an input to the WM8915. Master mode is selected for the DACLRCLK2 pin by setting the AIF2RX_LRCLK_MSTR bit.

In Master mode, the DACLRCLK2 frequency is controlled relative to BCLK2 by the AIF2RX_RATE divider.

In Master mode, the DACLRCLK2 output is generated by the WM8915 when either of the AIF2 channels is enabled. (Note that, when GPIO2 is configured as ADCLRCLK2, then only the AIF2 RX/input channels will cause DACLRCLK2 to be output.)

In Slave mode, the DACLRCLK2 output is disabled by default to allow another digital audio interface to drive this pin.

It is also possible to force the DACLRCLK2 signal to be output, using the AIF2RX_LRCLK_FRC bit, allowing mixed master and slave modes. When AIF2RX_LRCLK_FRC is set, the DACLRCLK2 signal is generated at all times in Master and Slave modes.

Note that the DACLRCLK2 signal is derived from BCLK2, and either an internal or external BCLK2 signal must be present to generate DACLRCLK2 output.

The DACLRCLK2 signal can be inverted in Master or Slave modes using the AIF2RX_LRCLK_INV register.

Under default conditions, the AIF2 output paths also use the DACLRCLK2 signal as the frame synchronisation clock. The AIF2 output interface uses a separate ADCLRCLK2 signal when selected using the AIF2TX_LRCLK_MODE bit.

The ADCLRCLK2 function must be selected on the GPIO2/ADCLRCLK2 pin as described in the “General Purpose Input/Output” section.

The ADCLRCLK2 pin can operate in Master or Slave mode, and is controlled similarly to the DACLRCLK2 function using the register bits described in Table 63.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R801 (0321h) AIF2 BCLK	10	AIF2_BCLK_INV	0	BCLK2 Invert 0 = BCLK2 not inverted 1 = BCLK2 inverted
	9	AIF2_BCLK_FRC	0	Force BCLK2 output in Master and Slave modes 0 = Normal 1 = BCLK2 enabled at all times (including when both AIF2 channels are disabled)
	8	AIF2_BCLK_MSTR	0	Select BCLK2 Master mode 0 = Slave Mode 1 = Master Mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	AIF2_BCLK_DIV	0000	BCLK2 Rate 0000 = AIFCLK 0001 = AIFCLK / 2 0010 = AIFCLK / 3 0011 = AIFCLK / 4 0100 = AIFCLK / 6 0101 = AIFCLK / 8 0110 = AIFCLK / 12 0111 = AIFCLK / 16 1000 = AIFCLK / 24 1001 = AIFCLK / 32 1010 = AIFCLK / 48 1011 = AIFCLK / 64 1100 = AIFCLK / 96 1101 = AIFCLK / 96 1110 = AIFCLK / 96 1111 = AIFCLK / 96 All other codes are Reserved
R802 (0322h) AIF2 TX LRCLK(1)	10:0	AIF2TX_RATE [10:0]	080h	ADCLRCLK2 Rate ADCLRCLK2 clock output = BCLK2 / AIF2TX_RATE Integer (LSB = 1) Valid from 8..2047
R803 (0323h) AIF2 TX LRCLK(2)	3	AIF2TX_LRCLK_MODE	1	AIF2 output path LRCLK select 0 = Use ADCLRCLK2 1 = Use DACLRCLK2
	2	AIF2TX_LRCLK_INV	0	ADCLRCLK2 Invert 0 = ADCLRCLK2 not inverted 1 = ADCLRCLK2 inverted
	1	AIF2TX_LRCLK_FRC	0	Force ADCLRCLK2 output in Master and Slave modes 0 = Normal 1 = ADCLRCLK2 enabled at all times (including when both AIF2 channels are disabled) Note that an internal or external BCLK2 signal must be present for ADCLRCLK2 output.
	0	AIF2TX_LRCLK_MSTR	0	Select ADCLRCLK2 Master mode 0 = Slave Mode 1 = Master Mode
R804 (0324h) AIF2 RX LRCLK(1)	10:0	AIF2RX_RATE [10:0]	080h	DACLRCLK2 Rate DACLRCLK2 clock output = BCLK2 / AIF2RX_RATE Integer (LSB = 1) Valid from 8..2047
R805 (0325h) AIF2 RX LRCLK	2	AIF2RX_LRCLK_INV	0	DACLRCLK2 Invert 0 = DACLRCLK2 not inverted 1 = DACLRCLK2 inverted

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	AIF2RX_LRCLK_FRC	0	Force DACLRCLK2 output in Master and Slave modes 0 = Normal 1 = DACLRCLK2 enabled at all times (including when both AIF2 channels are disabled) Note that an internal or external BCLK2 signal must be present for DACLRCLK2 output.
	0	AIF2RX_LRCLK_MSTR	0	Select DACLRCLK2 Master mode 0 = Slave Mode 1 = Master Mode

Table 63 AIF2 BCLK and LRCLK Control

AIF2 - DIGITAL AUDIO DATA CONTROL

The register bits controlling the audio data format, slot lengths and word lengths for AIF2 are described in Table 64.

Note that Left-Justified and DSP-B modes are valid in Master mode only (ie. BCLK and LRCLK are outputs from the WM8915).

The AIF slot length is the number of BCLK cycles in one timeslot within the overall LRCLK frame. The word length is the number of valid data bits within each timeslot. (If the word length is less than the slot length, then there will be unused BCLK cycles at the end of each timeslot.) The AIF2 word length and slot length is independently selectable for the input (RX) and output (TX) paths.

For each AIF2 output (TX) channel, the number and position of the audio data samples within the ADCLRCLK2 frame is configurable.

The _START_SLOT registers define the timeslot position of the first audio sample for the associated audio channel. Valid selections are Slot 0 upwards. The timeslots are numbered as illustrated in Figure 32 through to Figure 35.

Note that, in DSP modes, the slots are arranged in numerical sequence from Slot 0 upwards. In I2S and LJ modes, all of the even-numbered slots occur before the odd-numbered slots.

The _SLOTS registers define how many audio data samples of the associated audio channel are present within the LRCLK frame. Valid selections are 1 or more.

The _SPACING registers define how many timeslots are present between successive audio samples of the associated audio channel. Valid selectsions are 0 upwards.

Note that, if there are no timeslots used by any audio channel, the associated audio channel must be disabled using the registers described in Table 62. In this case, the slot configuration registers for that channel will have no effect.

Each AIF2 input and output channel can be digitally inverted using the _DAT_INV registers.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R800 (0320h) AIF2 Control	1:0	AIF2_FMT [1:0]	10	AIF2 Digital Audio Interface Format 00 = DSP Mode A 01 = DSP Mode B 10 = I^2S mode 11 = Left Justified mode
R806 (0326h) AIF2TX Data Configuration (1)	15:8	AIF2TX_WL [7:0]	18h	AIF2 TX Word Length Coded as integer (LSB = 1) Default is 24 bits
	7:0	AIF2TX_SLOT_LEN [7:0]	18h	AIF2 TX Slot Length Coded as integer (LSB = 1) Default is 24 bits

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R808 (0328h) AIF2RX Data Configuration	15:8	AIF2RX_WL [7:0]	18h	AIF2 RX Word Length Coded as integer (LSB = 1) Default is 24 bits
	7:0	AIF2RX_SLOT_LEN [7:0]	18h	AIF2 RX Slot Length Coded as integer (LSB = 1) Default is 24 bits
R809 (0329h) AIF2TX Channel 0 Configuration and R810 (032Ah) AIF2TX Channel 1 Configuration	15	AIF2TX_CHANn_DAT_INV	0	AIF2 TX Channel n Invert 0 = Not inverted 1 = Inverted
	14:9	AIF2TX_CHANn_SPACING [5:0]	00h	AIF2 TX Channel n Slot Spacing Defines the number of slots between successive samples of channel n Integer (LSB=1); Valid from 0 to 63
	8:6	AIF2TX_CHANn_SLOTS [2:0]	000	AIF2 TX Channel n Number of Slots Defines the number of audio samples of channel n within the LRCLK frame 000 = TX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF2TX_CHANn_ENA = 1.
	5:0	AIF2TX_CHANn_START_SLOT [5:0]	00h	AIF2 TX Channel n Start Slot position Defines the timeslot position of the first audio sample of channel n Integer (LSB=1); Valid from 0 to 63
R811 (032Bh) AIF2RX Channel 0 Configuration and R812 (032Ch) AIF1RX Channel 1 Configuration	15	AIF2RX_CHANn_DAT_INV	0	AIF2 RX Channel n Invert 0 = Not inverted 1 = Inverted
	14:9	AIF2RX_CHANn_SPACING [5:0]	00h	AIF2 RX Channel n Slot Spacing Defines the number of slots between successive samples of channel n Integer (LSB=1); Valid from 0 to 63
	8:6	AIF2RX_CHANn_SLOTS [2:0]	000	AIF2 RX Channel n Number of Slots Defines the number of audio samples of channel n within the LRCLK frame 000 = RX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF2RX_CHANn_ENA = 1.
	5:0	AIF2RX_CHANn_START_SLOT [5:0]	00h	AIF2 RX Channel n Start Slot position Defines the timeslot position of the first audio sample of channel n Integer (LSB=1); Valid from 0 to 63
Note: *n* is a number 0 or 1 that identifies the individual input or output channel.				

Table 64 AIF2 Digital Audio Data Control

AIF2 - MONO MODE AND DITHER CONTROL

A mono mode can be selected on the AIF2 input channels.

When AIF2RX_CHAN0_MONO_MODE is set, then the audio input on Channel 0 is copied onto input Channel 1. Note that AIF2RX_CHAN1_ENA must be set to 0 when the Channel 0 mono mode is selected.

Dithering is enabled by default in 16-bit mode. This function improves the accuracy of the AIF2 output channels when 16-bit word-length is selected. Dithering is not applied for other selections of the data word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R813 (032Dh) AIF2 RX Mono Configuration	0	AIF2RX_CHAN0_MONO_MODE	0	AIF2 RX Mono Mode 0 = Disabled 1 = Enabled When enabled, then RX channel 1 is copied onto RX channel 0. Note that channel 1 must be disabled (AIF2RX_CHAN1_ENA = 0).
R815 (032Fh) AIF2TX Test	0	AIF2TX_DITHER_ENA	1	AIF2 TX Dither 0 = Disabled 1 = Enabled in 16-bit mode

Table 65 AIF2 Mono Mode and Dither Control

AIF2 - TDM AND TRI-STATE CONTROL

The AIF2 output pins are tri-stated when the AIF2_TRI register is set. Note that, when the GPIO2/ADCLRCLK2 pin is configured as a GPIO, this pin is not affected by the AIF2_TRI register.

Under default conditions, the ADCDAT2 output is held a logic 0 when the WM8915 is not transmitting data (ie. during timeslots that are not enabled for output by the WM8915). When the AIF2TX_DAT_TRI is set, the WM8915 tri-states the ADCDAT2 pin when not transmitting data, allowing other devices to drive the ADCDAT2 connection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R800 (0320h) AIF2 Control	2	AIF2_TRI	0	AIF2 Tri-State Control 0 = Disabled (normal operation) 1 = Enabled (all AIF2 outputs tri-stated)
R807 (0327h) AIF2TX Data Configuration (2)	0	AIF2TX_DAT_TRI	0	ADCDAT2 Tri-State Control 0 = ADCDAT2 is logic 0 during disabled timeslots 1 = ADCDAT2 is tri-stated during disabled timeslots

Table 66 AIF2 TDM and Tri-State Control

DIGITAL PULL-UP AND PULL-DOWN

The WM8915 provides integrated pull-up and pull-down resistors on each of the DACDAT, DACLRCLK and BCLK pins for AIF1 and AIF2. This provides a flexible capability for interfacing with other devices. Each of the pull-up and pull-down resistors can be configured independently using the register bits described in Table 67.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1824 (0720h) Pull Control (1)	5	DACDAT1_PU	0	DACDAT1 Pull-up enable 0 = Disabled 1 = Enabled
	4	DACDAT1_PD	0	DACDAT1 Pull-down enable 0 = Disabled 1 = Enabled
	3	DACLRCLK1_PU	0	DACLRCLK1 Pull-up enable 0 = Disabled 1 = Enabled
	2	DACLRCLK1_PD	0	DACLRCLK1 Pull-down enable 0 = Disabled 1 = Enabled
	1	BCLK1_PU	0	BCLK1 Pull-up enable 0 = Disabled 1 = Enabled
	0	BCLK1_PD	0	BCLK1 Pull-down enable 0 = Disabled 1 = Enabled
R1825 (0721h) Pull Control (2)	5	DACDAT2_PU	0	DACDAT2 Pull-up enable 0 = Disabled 1 = Enabled
	4	DACDAT2_PD	0	DACDAT2 Pull-down enable 0 = Disabled 1 = Enabled
	3	DACLRCLK2_PU	0	DACLRCLK2 Pull-up enable 0 = Disabled 1 = Enabled
	2	DACLRCLK2_PD	0	DACLRCLK2 Pull-down enable 0 = Disabled 1 = Enabled
	1	BCLK2_PU	0	BCLK2 Pull-up enable 0 = Disabled 1 = Enabled
	0	BCLK2_PD	0	BCLK2 Pull-down enable 0 = Disabled 1 = Enabled

Table 67 Digital Pull-Up and Pull-Down Control

CLOCKING AND SAMPLE RATES

The internal clocks for the WM8915 are all derived from a common internal clock source, SYSCLK. This clock is the reference for the ADCs, DACs, DSP functions, Digital Audio Interface, Control Write Sequencer, Charge Pump, DC Servo control and other internal functions.

SYSCLK can be derived directly from MCLK1 or MCLK2, or may be generated from a Frequency Locked Loop (FLL) using MCLK1, MCLK2, BCLK1 or DACLRCLK1 as a reference. Many commonly-used audio sample rates can be derived directly from typical MCLK frequencies; for additional flexibility, the WM8915 incorporates a Frequency Locked Loop (FLL) circuit to perform frequency conversion and filtering. To avoid audible glitches, all clock configurations must be set up before enabling playback.

The SYSCLK frequency will support 48kHz (and related) sample rates or 44.1kHz (and related) sample rates, but not both together. Device operation at other SYSCLK frequencies is undefined.

When SYSCLK = 12.288MHz, the WM8915 supports 48kHz (and related) sample rates.

When SYSCLK = 11.2896MHz, the WM8915 supports 44.1kHz (and related) sample rates.

In AIF Slave modes, it is important to ensure that SYSCLK is synchronised with the external LRCLK signal. This can be achieved by selecting an MCLK input that is derived from the same reference as the LRCLK, or can be achieved by selecting the external BCLK1 or LRCLK1 signals as a reference input to the FLL, as a source for SYSCLK.

If SYSCLK is not synchronised with the LRCLK, then clicks arising from dropped or repeated audio samples will occur, due to the inherent tolerances of multiple, asynchronous, system clocks.

A low frequency clocking mode is provided, allowing the accessory detection functions to be supported in a low power device configuration, using only a 32kHz clock.

The FLL can be used to generate a free-running clock in the absence of an external reference source; see “Frequency Locked Loop” for further details.

The ADCs, DACs and digital mixing functions operate at a sample rate (fs) of 48kHz (12.288MHz SYSCLK frequency), or 44.1kHz (11.2896MHz SYSCLK frequency). The sample rates of the DSP signal paths to/from the digital audio interface are independently selectable, using the DSP1_DIV and DSP2_DIV registers.

A GPIO Clock, OPCLK, can be derived from CLK_SYS and output on the GPIO1 pin to provide clocking to other devices. This clock is enabled by OPCLK_ENA and controlled by OPCLK_DIV.

A slow clock, TOCLK, is used to set the timeout period for volume updates when zero-cross detect is used. This clock is enabled by TOCLK_ENA and controlled by TOCLK_DIV.

A de-bounce clock, DBCLK, is used to de-bounce the GPIO button / accessory-detect inputs. This clock is controlled by DBCLK_DIV.

In AIF master mode, the BCLK and LRCLK signals are derived from SYSCLK using programmable dividers. The BCLK and LRCLK signals can also be output in AIF slave mode, allowing mixed master/slave operation. See “Digital Audio Interface” for further details.

The control registers associated with Clocking and Sample Rates are shown in Table 68 to Table 75.

The overall clocking scheme for the WM8915 is illustrated in Figure 44.

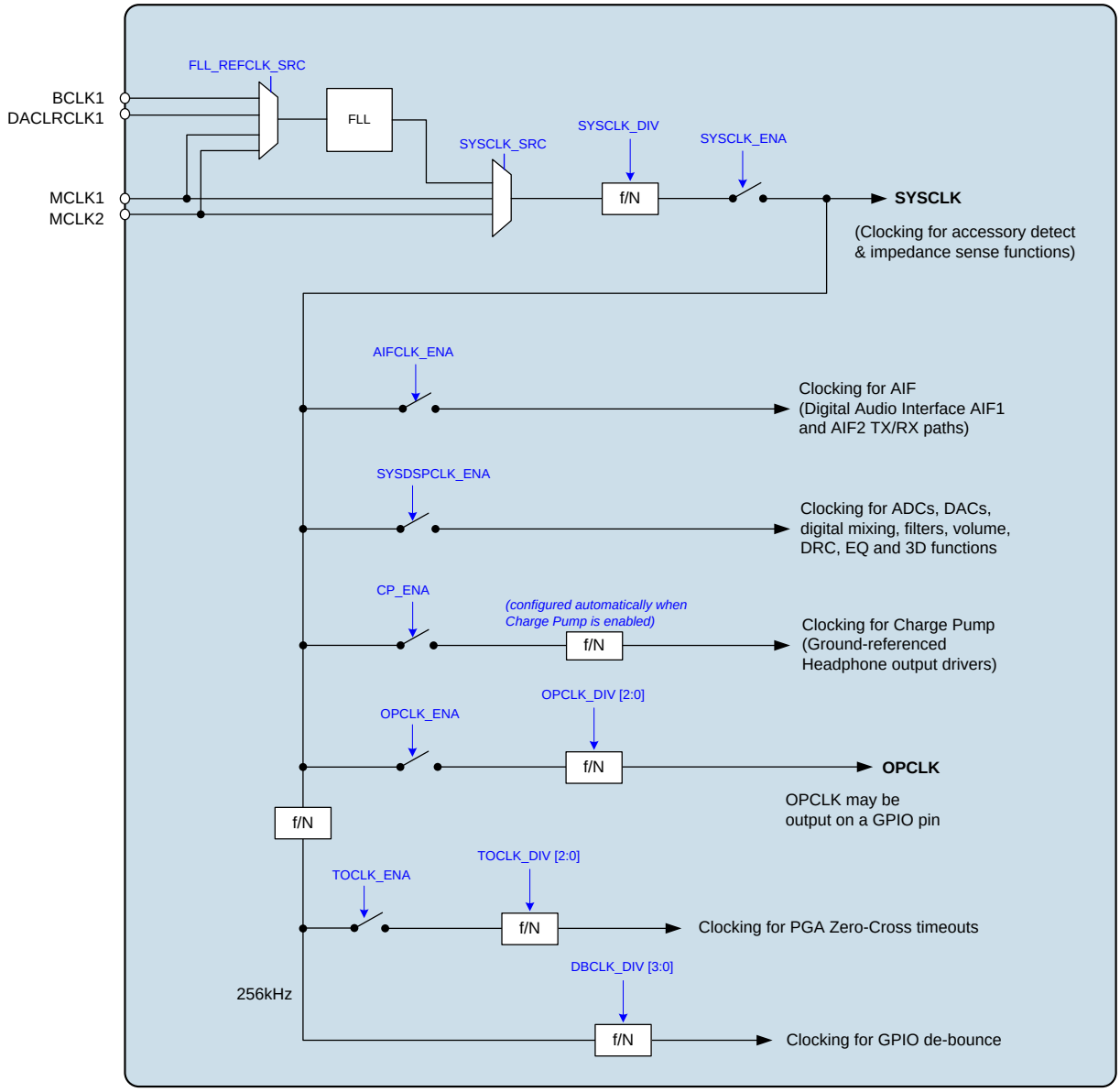


Figure 44 Clocking Scheme

MCLK AND SYSCLK CONTROL

The SYSCLK_SRC register is used to select the SYSCLK source. The source may be MCLK1, MCLK2 or the FLL output. The selected source may be inverted using the SYSCLK_INV register, and may also be adjusted by the SYSCLK_DIV divider if required.

The SYSCLK signal is enabled by the register bit SYSCLK_ENA. This bit should be set to 0 when reconfiguring the clock sources. It is not recommended to change SYSCLK_SRC while the SYSCLK_ENA bit is set.

Under normal operating conditions, the WM8915 clocking configuration should be set to provide a SYSCLK frequency of 12.288MHz (for 48kHz-related sample rates) or 11.2896MHz (for 44.1kHz-related sample rates). In these cases, the SYSCLK_RATE register must be set to 1.

Limited functionality can also be supported with a 6.144MHz (or 5.6448MHz) SYSCLK, allowing a reduction in power consumption. The 6.144MHz (or 5.6448MHz) clock frequency supports digital audio playback from AIF1 to the HPOUT1 and HPOUT2 headphone outputs, provided that the DRC, EQ and 3D functions are all disabled. In this case, the SYSCLK_RATE register must be set to 0.

The WM8915 also supports a low frequency clocking mode, allowing the accessory detection functions to be supported using a 32kHz SYSCLK. The low frequency clocking mode is enabled by LFCLK_ENA. This provides a low power standby condition - note that the digital audio functions are not supported in this mode.

The WM8915 provides integrated pull-up and pull-down resistors on the MCLK1 and MCLK2 pins. This provides a flexible capability for interfacing with other devices.

The MCLK and SYSCLK control register fields are defined in Table 68.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R512 (0200h) AIF Clocking (1)	4:3	SYSCLK_SRC	00	SYSCLK Source Select 00 = MCLK1 01 = MCLK2 10 = FLL 11 = Reserved
	2	SYSCLK_INV	0	SYSCLK Invert 0 = SYSCLK not inverted 1 = SYSCLK inverted
	1	SYSCLK_DIV	0	SYSCLK Divider 0 = SYSCLK 1 = SYSCLK / 2
	0	SYSCLK_ENA	0	SYSCLK Enable 0 = Disabled 1 = Enabled
R520 (0208h) Clocking (1)	5	LFCLK_ENA	0	Low Frequency Clocking Mode 0 = Disabled 1 = Enabled
R528 (0210h) AIF Rate	0	SYSCLK_RATE	1	SYSCLK Rate 0 = 6.144MHz (or 5.6448MHz) 1 = 12.288MHz (or 11.2896MHz) Note that the device is limited when SYSCLK_RATE=0. This is a power saving mode, which supports AIF1 playback to Headphone outputs, provided the DRC, EQ and 3D functions are all disabled.
R1824 (0720h) Pull Control (1)	9	MCLK2_PU	0	MCLK2 Pull-up enable 0 = Disabled 1 = Enabled
	8	MCLK2_PD	0	MCLK2 Pull-down enable 0 = Disabled 1 = Enabled
	7	MCLK1_PU	0	MCLK1 Pull-up enable 0 = Disabled 1 = Enabled
	6	MCLK1_PD	0	MCLK1 Pull-down resstor enable 0 = Disabled 1 = Enabled

Table 68 MCLK and SYSCLK Control

AIF CLOCK CONTROL

The SYSCLK signal provides clocking for the digital audio interfaces (AIF1 and AIF2). The audio interface clock is enabled by the register bit AIFCLK_ENA.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R520 (0208h) Clocking (1)	2	AIFCLK_ENA	0	AIF Clock Enable 0 = Disabled 1 = Enabled

Table 69 AIF Clock Control

DSP CLOCK CONTROL

The SYSCLK signal provides clocking for the ADC, DAC, digital mixing, filter, volume, DRC, EQ and 3D functions. The DSP clock is enabled by the register bit SYSDSPCLK_ENA.

The ADCs, DACs and digital mixing functions operate at a sample rate (fs) of 48kHz (12.288MHz SYSCLK frequency), or 44.1kHz (11.2896MHz SYSCLK frequency). The sample rates of the DSP signal paths to/from the digital audio interface are independently selectable, using the DSP1_DIV and DSP2_DIV registers.

The audio sample rate for the DSP1 signal paths is set by DSP1_DIV. The supported sample rates are 48kHz, 32kHz, 16kHz and 8kHz (assuming a SYSCLK frequency of 12.288MHz).

The audio sample rate for the DSP2 signal paths is set by DSP2_DIV. The supported sample rates are 48kHz, 32kHz, 16kHz and 8kHz (assuming a SYSCLK frequency of 12.288MHz).

Note that 44.1kHz sample rate is also supported, when the SYSCLK frequency is 11.2896MHz. In this case, the supported sample rates are 44.1kHz, 29.4kHz, 14.7kHz and 7.35kHz).

Note that the digital audio interface (AIF) supports multi-channel operation, including mixed sample rates. However, only one pair of stereo input/output paths is supported between the AIF and DSP1, which determines the DSP1_DIV setting. Similarly, only one pair of stereo input/output paths is supported between the AIF and DSP2, which determines the DSP2_DIV setting.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R513 (0201h) AIF Clocking (2)	4:3	DSP2_DIV [1:0]	00	Selects the sample rate for the AIF/DSP2 paths 00 = 48kHz (44.1kHz) 01 = 32kHz (29.4kHz) 10 = 16kHz (14.7kHz) 11 = 8kHz (7.35kHz) The 48kHz-related sample rates assume SYSCLK=12.288MHz. The figures in brackets apply for SYSCLK=11.2896MHz.
	1:0	DSP1_DIV [1:0]	00	Selects the sample rate for the AIF/DSP1 paths 00 = 48kHz (44.1kHz) 01 = 32kHz (29.4kHz) 10 = 16kHz (14.7kHz) 11 = 8kHz (7.35kHz) The 48kHz-related sample rates assume SYSCLK=12.288MHz. The figures in brackets apply for SYSCLK=11.2896MHz.
R520 (0208h) Clocking (1)	1	SYSDSPCLK_ ENA	0	DSP Clock Enable 0 = Disabled 1 = Enabled

Table 70 DSP Clock Control

MISCELLANEOUS CLOCKING CONTROL

Clocking is required to support a variety of other functions on the WM8915, including the Charge Pump, DC Servo and the Control Write Sequencer. Many of these are configured automatically; some are controlled by the registers described in this section.

The Charge Pump clock is derived from SYSCLK whenever the Charge Pump is enabled. This clock is required whenever the ground-referenced headphone outputs (HPOUT1L, HPOUT1R, HPOUT2L and HPOUT2R) are enabled. The Charge Pump clock division is configured automatically.

A clock output (OPCLK) derived from SYSCLK may be output on a GPIO pin. This clock is enabled by register big OPCLK_ENA, and its frequency of this clock is controlled by OPCLK_DIV. See “General Purpose Input/Output” to configure a GPIO pin for this function.

A slow clock (TOCLK) is derived internally in order to control volume update timeouts when the zero-cross option is selected. This clock is enabled by register bit TOCLK_ENA, and its frequency is controlled by TOCLK_DIV.

A de-bounce control is provided for GPIO inputs and for other functions that may be selected as GPIO outputs. The de-bounced clock frequency is controlled by DBCLK_DIV.

A high performance mode of ADC operation can be selected by setting the ADC_OSR128 bit; this bit selects 128x oversampling. Audio performance is improved, but power consumption is also increased.

The high performance mode of DAC operation is selected by default. A low-power mode of DAC operation can be selected using the DAC_OSR128 bit; the low-power mode selects 64x oversampling.

The clocking rate of the digital speaker (SPDM) circuit can be controlled by the SPK_OSR128 bit. This bit is enabled by default, giving best audio performance. De-selecting this bit gives 64x oversampling, resulting in decreased power consumption.

The clocking rate of the digital microphone (DMIC) interface circuit can be controlled by the DMIC_OSR64 bit. This bit is enabled by default, giving best audio performance. De-selecting this bit gives 32x oversampling, resulting in decreased power consumption.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (0002h) Power Management (2)	11	OPCLK_ENA	0	GPIO Clock Output (OPCLK) Enable 0 = Disabled 1 = Enabled
R520 (0208h) Clocking (1)	4	TOCLK_ENA	0	Slow Clock (TOCLK) Enable 0 = Disabled 1 = Enabled This clock is required for zero-cross timeout.
R521 (0209h) Clocking (2)	10:8	TOCLK_DIV [2:0]	000	Slow Clock (TOCLK) Divider (Sets TOCLK rate relative to 256kHz.) 000 = Divide by 256 (1kHz) 001 = Divide by 512 (500Hz) 010 = Divide by 1024 (250Hz) 011 = Divide by 2048 (125Hz) 100 = Divide by 4096 (62.5Hz) 101 = Divide by 8192 (31.2Hz) 110 = Divide by 16384 (15.6Hz) 111 = Divide by 32768 (7.8Hz)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:4	DBCLK_DIV [3:0]	0000	De-bounce Clock (DBCLK) Divider (Sets DBCLK rate relative to 256kHz. The de-bounce time, quoted in brackets, corresponds to 2 cycles of DBCLK) 0000 = Divide by 16 (125us) 0001 = Divide by 32 (250us) 0010 = Divide by 64 (500us) 0011 = Divide by 128 (1ms) 0100 = Divide by 256 (2ms) 0101 = Divide by 512 (4ms) 0110 = Divide by 1024 (8ms) 0111 = Divide by 2048 (16ms) 1000 = Divide by 4096 (32ms) 1001 = Divide by 8192 (64ms) 1010 = Divide by 16384 (128ms) 1011 = Divide by 32768 (256ms) 1100 = Divide by 65536 (512ms) When LFCLK_ENA = 1, the DBCLK rate is set relative to SYSCLK. In this case, with 32kHz SYSCLK, the de-bounce times above are multiplied by 8.
	2:0	OPCLK_DIV [2:0]	000	GPIO Output Clock (OPCLK) Divider 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16
R1568 (0620h) Oversampling	3	SPK_OSR128	1	Digital Speaker (SPDM) Oversample Rate Select 0 = 64fs 1 = 128fs
	2	DMIC_OSR64	1	Digital Microphone (DMIC) Oversample Rate Select 0 = 32fs 1 = 64fs
	1	ADC_OSR128	0	ADC Oversample Rate Select 0 = 64fs 1 = 128fs
	0	DAC_OSR128	1	DAC Oversample Rate Select 0 = 64fs 1 = 128fs

Table 71 Miscellaneous Clocking Controls

BCLK AND LRCLK CONTROL

The digital audio interfaces (AIF1 and AIF2) use BCLK and LRCLK signals for synchronisation. In master mode, these are output signals, generated by the WM8915. In slave mode, these are input signals to the WM8915. It is also possible to support mixed master/slave operation.

The BCLK and LRCLK signals are controlled as illustrated in Figure 45. See the “Digital Audio Interface Control” section for further details of the relevant control registers.

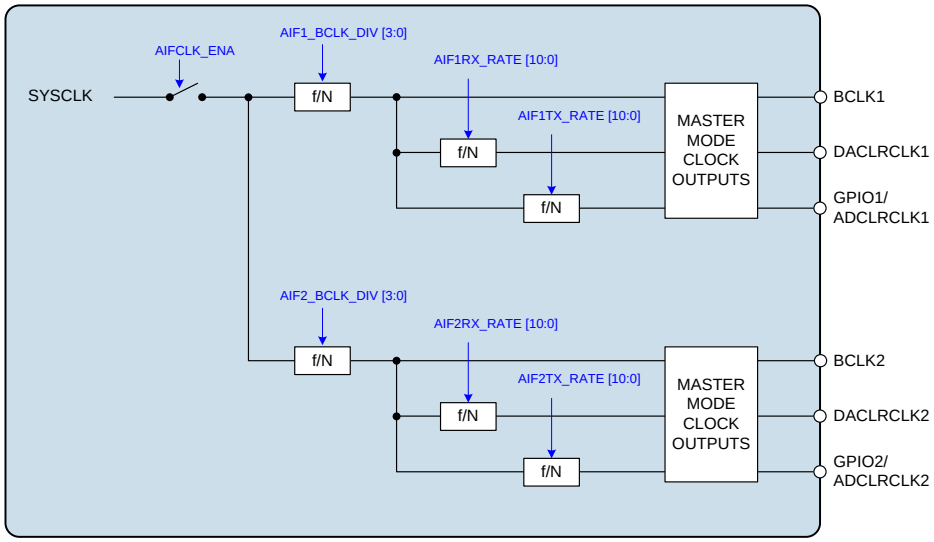


Figure 45 BCLK and LRCLK Control

CONTROL INTERFACE CLOCKING

Register map access is possible with or without a system clock (SYSCLK). Register writes are internally synchronised to SYSCLK whenever SYSCLK_ENA is set. This ensures best operation of any cross-clock domain functions.

When SYSCLK_ENA = 1, then an active clock source for SYSCLK must be present for control interface clocking. If the SYSCLK source is stopped, then SYSCLK_ENA must be set to 0 for control register access.

FREQUENCY LOCKED LOOP (FLL)

The WM8915 incorporates a Frequency Locked Loop (FLL) circuit. The FLL uses a highly accurate and configurable Exact Fractional Synthesis (EFS) circuit to generate SYSCLK from a wide variety of different reference sources and frequencies. The FLL can use MCLK1, MCLK2, BCLK1 or DACLRCLK1 as its reference; this is selected using the FLL_REFCLK_SRC register.

The FLL input reference may be a high frequency (eg. 24MHz) or low frequency (eg. 32kHz). The FLL is tolerant of jitter and may be used to generate a stable SYSCLK from a less stable input signal. The FLL characteristics are summarised in “Electrical Characteristics”.

Note that the FLL can be used to generate a free-running clock in the absence of an external reference source. This is described in the “Free-Running FLL Clock” section below.

The FLL control registers are illustrated in Figure 46.

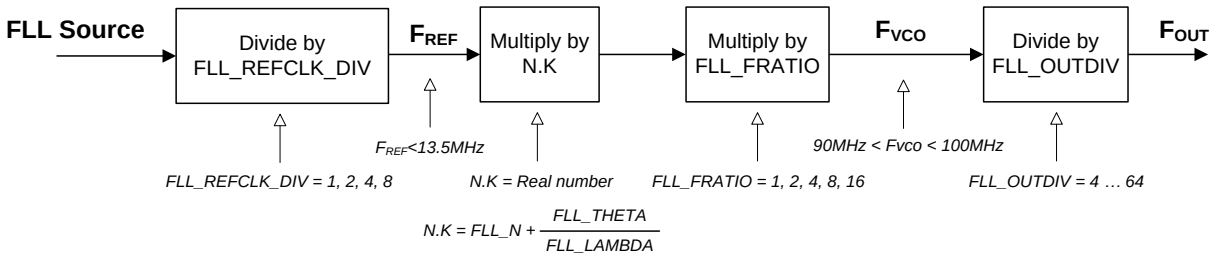


Figure 46 FLL Configuration

The FLL is enabled using the FLL_ENA register bit.

Note that the WM8915 bandgap reference is required by the FLL circuit (see “Reference Voltages and Master Bias”). When the bandgap is enabled, a delay of 1ms should be allowed for bandgap start-up before enabling the FLL.

When the FLL is enabled, any writes to the FLL control registers will be loaded into the respective control registers, but will not actually change the FLL output frequency. The FLL configuration is updated when a 1 is written to FLL_SWITCH_CLK; this enables a glitch-free transition to a new input reference clock, provided that the selected output frequency is not changed.

The active FLL clock source is indicated in the read-only register FLL_REFCLK_SRC_STS. Completion of the transition to a new FLL input reference clock can be indicated via a GPIO output or used to trigger an Interrupt event. Note that, for a successful transition, the old and the new input reference clocks must both be present until after the FLL_SW_CLK_DONE_EINT interrupt has been set.

When changing FLL settings to a new output frequency, it is recommended that the digital circuit is disabled via FLL_ENA and then re-enabled after the other register settings have been updated.

The field FLL_REFCLK_DIV provides the option to divide the input reference (MCLK1, MCLK2, BCLK1 or DACLRCLK1) by 1, 2 or 4. This field should be set to bring the reference down to 13.5MHz or below. For best performance, it is recommended that the highest possible frequency - within the 13.5MHz limit - should be selected.

The FLL_REF_FREQ register should be set as described in Table 74.

The FLL_LOOP_GAIN register should be set as described in Table 74.

The FLL output frequency is directly determined from FLL_FRATIO, FLL_OUTDIV and the real number represented by N.K.

The integer value, N, is held in the FLL_N register field. The fractional portion, K, is determined by the ratio FLL_THETA / FLL_LAMBDA.

Note that the FLL_EFS_ENA register bit must be enabled in fractional mode (ie. whenever FLL_THETA > 0).

The FLL output frequency is generated according to the following equation:

$$F_{OUT} = (F_{VCO} / FLL\_OUTDIV)$$

The FLL operating frequency, F_{VCO} is set according to the following equation:

$$F_{VCO} = (F_{REF} \times N.K \times FLL\_FRATIO)$$

F_{REF} is the input frequency, as determined by FLL_REFCLK_DIV.

F_{VCO} must be in the range 90-100 MHz. Frequencies outside this range cannot be supported.

Note that the output frequencies that do not lie within the ranges quoted above cannot be guaranteed across the full range of device operating conditions.

In order to follow the above requirements for F_{VCO}, the value of FLL_OUTDIV should be selected according to the desired output F_{OUT}. The FLL_OUTDIV register must be set so that F_{VCO} is in the range 90-100MHz. The available ratios are integers from 2 to 64. Some typical settings of FLL_OUTDIV are noted in Table 72.

OUTPUT FREQUENCY F_{OUT}	FLL_OUTDIV
5.625 MHz - 6.25 MHz	001111 (F_{OUT} clock ratio = 16)
11.25 MHz - 12.5 MHz	000111 (F_{OUT} clock ratio = 8)

Table 72 Selection of FLL_OUTDIV

The value of FLL_FRATIO should be selected as described in Table 73.

REFERENCE FREQUENCY F_{REF}	FLL_FRATIO
1MHz - 13.5MHz	0h (F_{VCO} clock ratio = 1)
256kHz - 1MHz	1h (F_{VCO} clock ratio = 2)
128kHz - 256kHz	2h (F_{VCO} clock ratio = 4)
64kHz - 128kHz	3h (F_{VCO} clock ratio = 8)
Less than 64kHz	4h (F_{VCO} clock ratio = 16)

Table 73 Selection of FLL_FRATIO

In order to determine the remaining FLL parameters, the FLL operating frequency, F_{VCO}, must be calculated, as given by the following equation:

$$F_{VCO} = (F_{OUT} \times FLL\_OUTDIV)$$

The value of N.K can then be determined as follows:

$$N.K = F_{VCO} / (FLL\_FRATIO \times F_{REF})$$

Note that, in the above equations:

FLL_OUTDIV is the F_{OUT} clock ratio (8 or 16).

F_{REF} is the input frequency, after division by FLL_REFCLK_DIV, where applicable.

FLL_FRATIO is the F_{VCO} clock ratio (1, 2, 4, 8 or 16).

The value of N is held in the FLL_N register field.

The value of K is determined by the ratio FLL_THETA / FLL_LAMBDA.

The FLL_N, FLL_THETA and FLL_LAMBDA fields are all coded as integers (LSB = 1).

In Fractional Mode (FLL_THETA > 0 and FLL_EFS_ENA = 1), the register fields FLL_THETA and FLL_LAMBDA can be calculated as follows:

Calculate GCD(FLL) using the 'Greatest Common Denominator' function:

$$GCD(FLL) = GCD(FLL\_FRATIO \times F_{REF}, F_{VCO})$$

where GCD(x, y) is the greatest common denominator of x and y

Next, calculate FLL_THETA and FLL_LAMBDA using the following equations:

$$FLL\_THETA = (F_{VCO} - (FLL\_N \times FLL\_FRATIO \times F_{REF})) / GCD(FLL)$$

$$FLL\_LAMBDA = (FLL\_FRATIO \times F_{REF}) / GCD(FLL)$$

Note that, in Fractional Mode, the values of FLL_THETA and FLL_LAMBDA must be co-prime (ie. not divisible by any common integer). The calculation above ensures that the values will be co-prime.

The value of K must be a fraction less than 1 (ie. FLL_THETA must be less than FLL_LAMBDA).

In Fractional Mode, it is recommended to set the EFS Dither Mode select field as described in Table 74 (ie. FLL_LFSR_SEL = 11).

The FLL control registers are described in Table 74. An example FLL calculation is provided at the end of this section. Example settings for a variety of reference frequencies and output frequencies are shown in Table 76.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R544 (0220h) FLL Control (1)	0	FLL_ENA	0	FLL Enable 0 = Disabled 1 = Enabled
R545 (0221h) FLL Control (2)	13:8	FLL_OUTDIV [5:0]	000000	FLL F_{OUT} clock ratio 000000 = Reserved 000001 = 2 000010 = 3 000011 = 4 000100 = 5 000101 = 6 … 111110 = 63 111111 = 64 (F_{OUT} = F_{VCO} / FLL_OUTDIV)
	2:0	FLL_FRATIO [2:0]	000	FLL F_{VCO} clock ratio 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16
R546 (0222h) FLL Control (3)	15:0	FLL_THETA [15:0]	0000h	FLL Fractional multiply for F_{REF} This field sets the numerator (multiply) part of the FLL_THETA / FLL_LAMBDA ratio. Coded as LSB = 1.
R547 (0223h) FLL Control (4)	14:5	FLL_N [9:0]	2EEh	FLL Integer multiply for F_{REF} (LSB = 1)
	3:0	FLL_LOOP_GAIN [3:0]	0000	Gain applied to error 0000 = x 1 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that this should be set to 0101 (x32) when the input reference frequency is 3MHz or higher. Recommended that this should be set to 0000 (x1) in all other cases.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R548 (0224h) FLL Control (5)	4:3	FLL_REFCLK_DIV [1:0]	00	FLL Clock Reference Divider 00 = MCLK / 1 01 = MCLK / 2 10 = MCLK / 4 11 = MCLK / 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	2	FLL_REF_FREQ	1	Low frequency reference locking 0 = High frequency reference locking (recommended for reference clock > 48kHz) 1 = Lock frequency reference locking (recommended for reference clock <= 48kHz)
	1:0	FLL_REFCLK_SRC [1:0]	00	FLL Clock source 00 = MCLK1 01 = MCLK2 10 = DACLRCLK1 11 = BCLK1
R549 (0225h) FLL Control (6)	3:2	FLL_REFCLK_SRC_STS [1:0]	0	FLL Clock Source (Read Only) 00 = MCLK1 01 = MCLK2 10 = DACLRCLK1 11 = BCLK1 Writing to FLL_REFCLK_SRC while the FLL is enabled will not change the FLL Clock source until a 1 is written to FLL_SWITCH_CLK. The read-only FLL_REFCLK_SRC_STS field indicates the active FLL Clock source.
	0	FLL_SWITCH_CLK	0	FLL Clock Switch Writing a 1 to this bit will cause the FLL configuration to be updated. (Updates to the FLL control registers while the FLL is enabled will not change the FLL output frequency until a 1 is written to FLL_SWITCH_CLK.)
R550 (0226h) FLL EFS 1	15:0	FLL_LAMBDA [15:0]	0000h	FLL Fractional multiply for F_{REF} This field sets the denominator (dividing) part of the FLL_THETA / FLL_LAMBDA ratio. Coded as LSB = 1.
R551 (0227h) FLL EFS 2	2:1	FLL_LFSR_SEL [1:0]	01	FLL EFS Dither Mode select 11 is recommended when FLL_EFS_ENA = 1.
	0	FLL_EFS_ENA	0	FLL Fractional Mode EFS enable 0 = Integer Mode 1 = Fractional Mode This bit should be set to 1 when FLL_THETA > 0.

Table 74 FLL Register Map

FREE-RUNNING FLL CLOCK

The FLL can generate a clock signal even when no external reference is available. However, it should be noted that the accuracy of this clock is reduced, and a reference source should always be used where possible. The free-running FLL modes are not sufficiently accurate for hi-fi ADC or DAC operations, but are suitable for clocking most other functions, including the Control Write Sequencer, Charge Pump and DC Servo. The free-running FLL operation is ideal for clocking the accessory detection function during low-power standby operating conditions (see “External Accessory Detection”).

If an accurate reference clock is initially available, then the FLL should be configured as described above. The FLL will continue to generate a stable output clock after the reference input is stopped or disconnected.

If no reference clock is available at the time of starting up the FLL, then an internal clock frequency of approximately 12MHz can be generated by implementing the following sequence:

- Enable the FLL Analogue Oscillator (FLL_OSC_ENA = 1)
- Set the F_{OUT} clock divider to divide by 8 (FLL_OUTDIV = 000111)
- Configure the oscillator frequency by setting FLL_FRC_NCO = 1 and FLL_FRC_NCO_VAL = 19h

Note that the free-running FLL mode is not suitable for hi-fi CODEC applications. In the absence of any reference clock, the FLL output is subject to a very wide tolerance; see “Electrical Characteristics” for details of the FLL accuracy.

Note that the free-running FLL clock is selected as SYSCLK using the SYSCLK_SRC register, as illustrated in Figure 44.

The control registers applicable to FLL free-running modes are described in Table 75.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R544 (0220h) FLL Control (1)	1	FLL_OSC_ENA	0	FLL Oscillator enable 0 = Disabled 1 = Enabled (Note that this field is required for free-running FLL modes only)
R548 (0224h) FLL Control (5)	12:7	FLL_FRC_NCO_VAL [5:0]	19h	FLL Forced oscillator value Valid range is 000000 to 111111 0x19h (011001) = 12MHz approx (Note that this field is required for free-running FLL modes only)
	6	FLL_FRC_NCO	0	FLL Forced control select 0 = Normal 1 = FLL oscillator controlled by FLL_FRC_NCO_VAL (Note that this field is required for free-running FLL modes only)

Table 75 FLL Free-Running Mode

GPIO OUTPUTS FROM FLL

The WM8915 supports glitch-free transition between input reference clocks (provided that the selected output frequency is not changed). The internal signal indicating the FLL Clock Switch transition status is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

The FLL Clock Switch transition status can be output directly on a GPIO pin as an external indication of the FLL Clock Switch transition. See “General Purpose Input/Output” for details of how to configure a GPIO pin to output the FLL Clock Switch signal.

The WM8915 has an internal signal which indicates whether the FLL Lock has been achieved. The FLL Lock status is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

The FLL Lock signal can be output directly on a GPIO pin as an external indication of FLL Lock. See “General Purpose Input/Output” for details of how to configure a GPIO pin to output the FLL Lock signal.

The FLL Clock can be output directly on a GPIO pin as a clock signal for other circuits. Note that the FLL Clock may be output even if the FLL is not selected as the WM8915 SYSCLK source. The FLL clocking configuration is illustrated in Figure 44. See “General Purpose Input/Output” for details of how to configure a GPIO pin to output the FLL Clock.

EXAMPLE FLL CALCULATION

The following example illustrates how to derive the FLL registers to generate 12.288 MHz output (F_{OUT}) from a 13.000 MHz reference clock (F_{REF}):

- Set FLL_REFCLK_DIV in order to generate F_{REF} <=13.5MHz:
  FLL_REFCLK_DIV = 00 (divide by 1)
- Set FLL_OUTDIV for the required output frequency as shown in Table 72:-
  F_{OUT} = 12.288 MHz, therefore FLL_OUTDIV = 07h (F_{OUT} clock ratio = 8)
- Set FLL_FRATIO for the given reference frequency as shown in Table 73:
  F_{REF} = 13MHz, therefore FLL_FRATIO = 0h (F_{VCO} clock ratio = 1)
- Calculate F_{VCO} as given by $F_{VCO} = F_{OUT}$ x FLL_OUTDIV:-
  F_{VCO} = 12.288 x 8 = 98.304MHz
- Calculate N.K as given by N.K = F_{VCO} / (FLL_FRATIO x F_{REF}):
  N.K = 98.304 / (1 x 13) = 7.561846
- Determine FLL_N from the integer portion of N.K:-
  FLL_N = 7 (007h)
- Confirm that N.K is a fractional quantity and set FLL_EFS_ENA:
  N.K is fractional. Set FLL_EFS_ENA = 1.
- Determine GCD(FLL), as given by GCD(FLL) = GCD(FLL_FRATIO x F_{REF}, F_{VCO}):
  GCD(FLL) = GCD(1 x 13000000, 98304000) = 8000
- Determine FLL_THETA, as given by
  FLL_THETA = (F_{VCO} - (FLL_N x FLL_FRATIO x F_{REF})) / GCD(FLL):
  FLL_THETA = (98304000 - (7 x 1 x 13000000)) / 8000
  FLL_THETA = 913 (0391h)
- Determine FLL_LAMBDA, as given by
  FLL_LAMBDA = (FLL_FRATIO x F_{REF}) / GCD(FLL):
  FLL_LAMBDA = (1 x 13000000) / 8000
  FLL_LAMBDA = 1625 (0659h)

EXAMPLE FLL SETTINGS

Table 76 provides example FLL settings for generating SYSCLK from a variety of low and high frequency reference inputs.

F_{REF}	F_{OUT}	FLL_ REFCLK_DIV	F_{VCO}	FLL_N	FLL_EFS_ENA	FLL_ THETA	FLL_ LAMBDA	FLL_ FRATIO	FLL_ OUTDIV
32.000 kHz	12.288 MHz	Divide by 1 (0h)	98.304 MHz	192 (0C0h)	0	0 (0000h)	0 (0000h)	16 (4h)	8 (7h)
32.000 kHz	11.2896 MHz	Divide by 1 (0h)	90.3168 MHz	176 (0B0h)	0	2 (0002h)	5 (0005h)	16 (4h)	8 (7h)
32.768 kHz	12.288 MHz	Divide by 1 (0h)	98.304 MHz	187 (0BBh)	1	1 (0001h)	2 (0002h)	16 (4h)	8 (7h)
32.768 kHz	11.2896 MHz	Divide by 1 (0h)	90.3168 MHz	172 (0ACh)	1	17 (0011h)	64 (0040h)	16 (4h)	8 (7h)
48 kHz	12.288 MHz	Divide by 1 (0h)	98.304 MHz	128 (080h)	0	0 (0000h)	0 (0000h)	16 (4h)	8 (7h)
48 kHz	11.2896 MHz	Divide by 1 (0h)	90.3168 MHz	117 (075h)	0	3 (0003h)	5 (0005h)	16 (4h)	8 (7h)
12.000 MHz	12.288 MHz	Divide by 1 (0h)	98.3040 MHz	8 (008h)	1	24 (0018h)	125 (007Dh)	1 (0h)	8 (7h)
12.000 MHz	11.2896 MHz	Divide by 1 (0h)	90.3168 MHz	7 (007h)	1	329 (0149h)	625 (0271h)	1 (0h)	8 (7h)
12.288 MHz	12.288 MHz	Divide by 1 (0h)	98.304 MHz	8 (008h)	0	0 (0000h)	0 (0000h)	1 (0h)	8 (7h)
12.288 MHz	11.2896 MHz	Divide by 1 (0h)	90.3168 MHz	7 (007h)	0	7 (0007h)	20 (0014h)	1 (0h)	8 (7h)
13.000 MHz	12.288 MHz	Divide by 1 (0h)	98.3040 MHz	7 (007h)	1	913 (0391h)	1625 (0659h)	1 (0h)	8 (7h)
13.000 MHz	11.2896 MHz	Divide by 1 (0h)	90.3168 MHz	6 (006h)	1	7698 (1E12h)	8125 (1FBDh)	1 (0h)	8 (7h)
19.200 MHz	12.288 MHz	Divide by 2 (1h)	98.3039 MHz	10 (00Ah)	1	6 (0006h)	25 (0019h)	1 (0h)	8 (7h)
19.200 MHz	11.2896 MHz	Divide by 2 (1h)	90.3168 MHz	9 (009h)	1	51 (0033h)	125 (007Dh)	1 (0h)	8 (7h)

Table 76 Example FLL Settings

CONTROL INTERFACE

The WM8915 is controlled by writing to registers through a 2-wire serial control interface. Readback is available for all registers, including Chip ID, power management status and GPIO status.

Note that the Control Interface function can be supported with or without system clocking. Where possible, the register map access is synchronised with SYSCLK in order to ensure best operation of any cross-clock domain functions. See “Clocking and Sample Rates” for further details of Control Interface clocking.

The WM8915 is a slave device on the control interface; SCLK is a clock input, while SDA is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8915 transmits logic 1 by tri-stating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single 2-wire control bus, every device on the bus has a unique 8-bit device ID (this is not the same as the 16-bit address of each register in the WM8915).

The device ID is selectable on the WM8915, using the ADDR pin as shown in Table 77. The LSB of the Device ID is the Read/Write bit; this bit is set to logic 1 for “Read” and logic 0 for “Write”.

ADDR	DEVICE ID
Low	0011 010x = 34h (write) / 35h (read)
High	0011 011x = 36h (write) / 37h (read)

Table 77 Control Interface Device ID

The WM8915 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDA while SCLK remains high. This indicates that a device ID, register address and data will follow. The WM8915 responds to the start condition and shifts in the next eight bits on SDA (8-bit device ID, including Read/Write bit, MSB first). If the device ID received matches the device ID of the WM8915, then the WM8915 responds by pulling SDA low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is set incorrectly, the WM8915 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM8915, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDA while SCLK remains high. After receiving a complete address and data sequence the WM8915 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDA changes while SCLK is high), the device returns to the idle condition.

The WM8915 supports the following read and write operations:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

The sequence of signals associated with a single register write operation is illustrated in Figure 47.

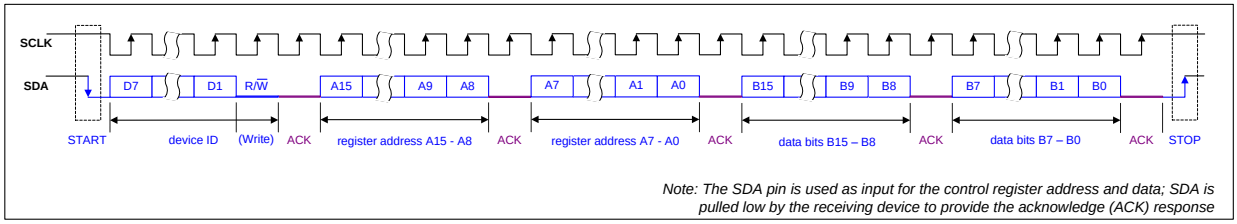


Figure 47 Control Interface 2-wire (I2C) Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 48.

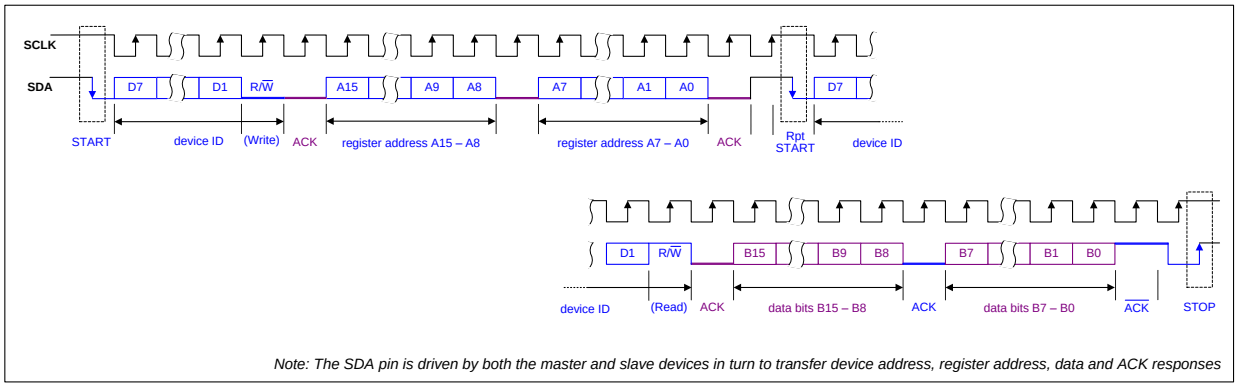


Figure 48 Control Interface 2-wire (I2C) Register Read

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 78.

Note that, for multiple write and multiple read operations, the auto-increment option must be enabled. This feature is enabled by default, as noted in Table 79.

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge (SDA Low)	
$\overline{A}$	Not Acknowledge (SDA High)	
P	Stop Condition	
R/$\overline{W}$	ReadNotWrite	0 = Write 1 = Read
[White field]	Data flow from bus master to WM8915	
[Grey field]	Data flow from WM8915 to bus master	

Table 78 Control Interface Terminology

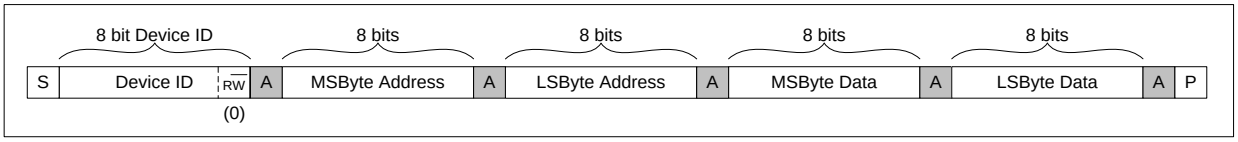


Figure 49 Single Register Write to Specified Address

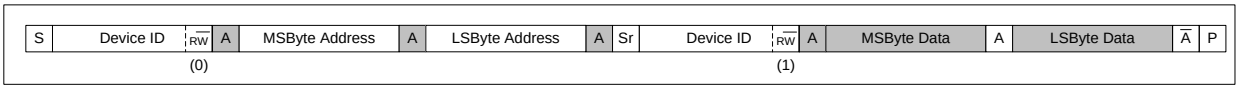


Figure 50 Single Register Read from Specified Address

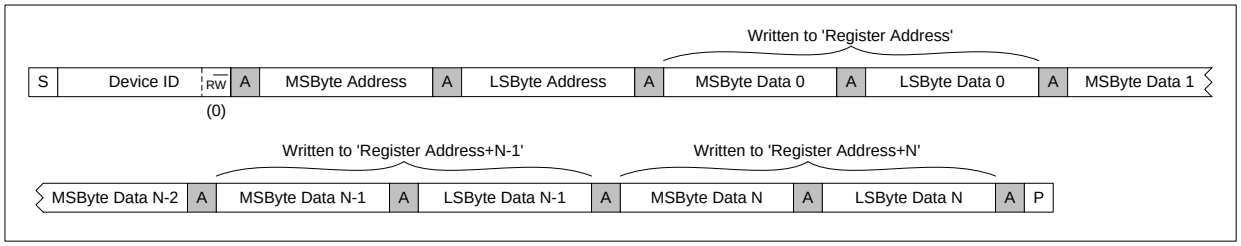


Figure 51 Multiple Register Write to Specified Address using Auto-increment

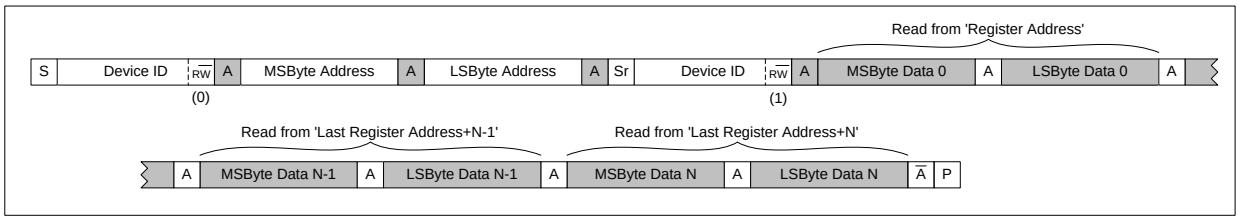


Figure 52 Multiple Register Read from Specified Address using Auto-increment

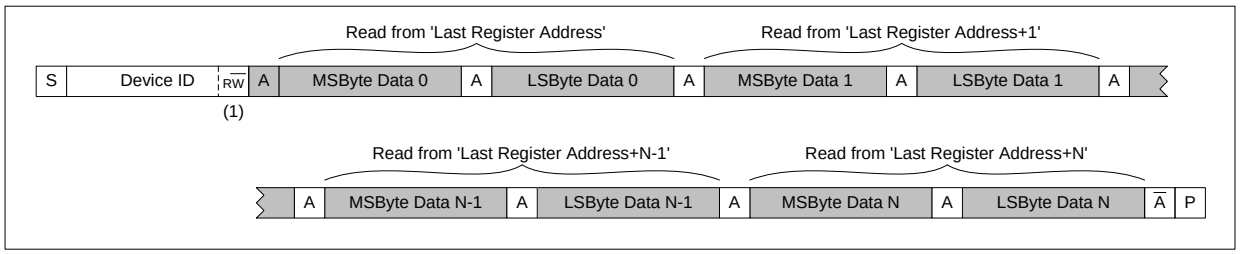


Figure 53 Multiple Register Read from Last Address using Auto-increment

In 2-wire (I2C) Control Interface mode, Auto-Increment mode may be selected. This enables multiple write and multiple read operations to be scheduled faster than is possible with single register operations. The auto-increment option is enabled when the AUTO_INC register bit is set. This bit is defined in Table 79. Auto-increment is enabled by default.

A pull-down resistor is provided on the ADDR pin; this is configurable using the ADDR_PD register. The pull-down resistor is enabled by default.

The Control Interface configuration bits are described in Table 79.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R257 (0101h) Control Interface (1)	2	AUTO_INC	1	Enables address auto-increment 0 = Disabled 1 = Enabled
R1825 (0721h) Pull Control (2)	6	ADDR_PD	1	ADDR Pull-down enable 0 = Disabled 1 = Enabled

Table 79 Control Interface Configuration

CONTROL WRITE SEQUENCER

The Control Write Sequencer is a programmable unit that forms part of the WM8915 control interface logic. It provides the ability to perform a sequence of register write operations with the minimum of demands on the host processor - the sequence may be initiated by a single operation from the host processor and then left to execute independently.

Default sequences for Start-Up and Shut-Down of each headphone output driver are provided (see "Default Sequences" section). It is recommended that these default sequences are used unless changes become necessary.

When a sequence is initiated, the sequencer performs a series of pre-defined register writes. The host processor informs the sequencer of the start index of the required sequence within the sequencer's memory. At each step of the sequence, the contents of the selected register fields are read from the sequencer's memory and copied into the WM8915 control registers. This continues sequentially through the sequencer's memory until an "End of Sequence" bit is encountered; at this point, the sequencer stops and an Interrupt status flag is asserted. For cases where the timing of the write sequence is important, a programmable delay can be set for specific steps within the sequence.

Note that the Control Write Sequencer's internal clock is derived from the internal clock SYSCLK which must be enabled as described in "Clocking and Sample Rates". The clock division from SYSCLK is handled transparently by the WM8915 without user intervention, provided that SYSCLK is configured as specified in "Clocking and Sample Rates".

INITIATING A SEQUENCE

The Register fields associated with running the Control Write Sequencer are described in Table 80. Note that the operation of the Control Write Sequencer also requires the internal clock SYSCLK to be configured as described in "Clocking and Sample Rates".

The Write Sequencer is enabled by setting the WSEQ_ENA bit. The start index of the required sequence must be written to the WSEQ_START_INDEX field.

The Write Sequencer stores up to 128 register write commands. These are defined in Registers R12288 to R12799. There are 4 registers used to define each of the 128 possible commands. The value of WSEQ_START_INDEX selects the registers applicable to the first write command in the selected sequence.

Setting the WSEQ_START bit initiates the sequencer at the given start index. The Write Sequencer can be interrupted by writing a logic 1 to the WSEQ_ABORT bit.

The current status of the Write Sequencer can be read using two further register fields - when the WSEQ_BUSY bit is asserted, this indicates that the Write Sequencer is busy. Note that, whilst the Control Write Sequencer is running a sequence (indicated by the WSEQ_BUSY bit), normal read/write operations to the Control Registers cannot be supported. The index of the current step in the Write Sequencer can be read from the WSEQ_CURRENT_INDEX field; this is an indicator of the sequencer's progress. On completion of a sequence, this field holds the index of the last step within the last commanded sequence.

When the Write Sequencer reaches the end of a sequence, it asserts the WSEQ_DONE_EINT flag in Register R1841 (see Table 56). This flag can be used to generate an Interrupt Event on completion of the sequence. Note that the WSEQ_DONE_EINT flag is asserted to indicate that the WSEQ is NOT Busy.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R272 (0110h) Write Sequencer Ctrl (1)	15	WSEQ_ENA	0	Write Sequencer Enable 0 = Disabled 1 = Enabled
	9	WSEQ_ABORT	0	Writing a 1 to this bit aborts the current sequence and returns control of the device back to the serial control interface.
	8	WSEQ_START	0	Writing a 1 to this bit starts the write sequencer at the index location selected by WSEQ_START_INDEX. The sequence continues until it reaches an "End of sequence" flag. At the end of the sequence, this bit will be reset by the Write Sequencer.
	6:0	WSEQ_START_INDEX [6:0]	000_0000	Sequence Start Index. This field determines the memory location of the first command in the selected sequence. There are 127 Write Sequencer RAM addresses: 00h = WSEQ_ADDR0 (R12288) 01h = WSEQ_ADDR1 (R12292) 02h = WSEQ_ADDR2 (R12296) …. 7Fh = WSEQ_ADDR127 (R12796)
R273 (0111h) Write Sequencer Ctrl (2)	8	WSEQ_BUSY (read only)	0	Sequencer Busy flag (Read Only). 0 = Sequencer idle 1 = Sequencer busy Note: it is not possible to write to control registers via the control interface while the Sequencer is Busy.
	6:0	WSEQ_CURRENT_INDEX [6:0] (read only)	000_0000	Sequence Current Index. This indicates the memory location of the most recently accessed command in the write sequencer memory. Coding is the same as WSEQ_START_INDEX.

Table 80 Write Sequencer Control - Initiating a Sequence

PROGRAMMING A SEQUENCE

A sequence consists of write operations to data bits (or groups of bits) within the control registers. Each write operation is defined by a block of 4 registers, which contain 6 fields as described in this section.

The block of 4 registers is the same for up to 128 steps held in the sequencer memory. Multiple sequences can be held in the memory at the same time; each sequence occupies its own range within the 128 available register blocks.

The following 6 fields are replicated 128 times - one for each of the sequencer's 128 steps. In the following descriptions, the term '*n*' is used to denote the step number, from 0 to 127.

WSEQ_ADDR*n* is a 14-bit field containing the Control Register Address in which the data should be written.

WSEQ_DATA*n* is an 8-bit field which contains the data to be written to the selected Control Register. The WSEQ_DATA_WIDTH*n* field determines how many of these bits are written to the selected register; the most significant bits (above the number indicated by WSEQ_DATA_WIDTH*n*) are ignored.

WSEQ_DATA_START*n* is a 4-bit field which identifies the LSB position within the selected Control Register to which the data should be written. For example, setting WSEQ_DATA_START*n* = 0100 will select bit 4 as the LSB position; in this case, 4-bit data would be written to bits 7:4.

WSEQ_DATA_WIDTH*n* is a 3-bit field which identifies the width of the data block to be written. This enables selected portions of a Control Register to be updated without any concern for other bits within the same register, eliminating the need for read-modify-write procedures. Values of 0 to 7 correspond to data widths of 1 to 8 respectively. For example, setting WSEQ_DATA_WIDTH*n* = 010 will cause a 3-bit data block to be written. Note that the maximum value of this field corresponds to an 8-bit data block; writing to register fields greater than 8 bits wide must be performed using two separate operations of the Control Write Sequencer.

WSEQ_DELAY*n* is a 4-bit field which controls the waiting time between the current step and the next step in the sequence i.e. the delay occurs after the write in which it was called. The total delay time per step (including execution) is defined below, giving a useful range of execution/delay times from 562µs up to 2.048s per step:

$$T = k \times (2^{WSEQ\_DELAY} + 8)$$

where k = 62.5µs (under recommended operating conditions)

WSEQ_EOS*n* is a 1-bit field which indicates the End of Sequence. If this bit is set, then the Control Write Sequencer will automatically stop after this step has been executed.

The register definitions for Step 0 are described in Table 81. The equivalent definitions also apply to Step 1 through to Step 127, in the subsequent register address locations.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12288 (3000h) Write Sequencer 0	13:0	WSEQ_ADDR 0 [13:0]	0000h	Control Register Address to be written to in this sequence step.
R12289 (3001h) Write Sequencer 1	7:0	WSEQ_DATA 0 [7:0]	00h	Data to be written in this sequence step. When the data width is less than 8 bits, then one or more of the MSBs of WSEQ_DATA*n* are ignored. It is recommended that unused bits be set to 0.
R12290 (3002h) Write Sequencer 2	10:8	WSEQ_DATA _WIDTH0 [2:0]	000	Width of the data block written in this sequence step. 000 = 1 bit 001 = 2 bits 010 = 3 bits 011 = 4 bits 100 = 5 bits 101 = 6 bits 110 = 7 bits 111 = 8 bits
	3:0	WSEQ_DATA _START0 [3:0]	0000	Bit position of the LSB of the data block written in this sequence step. 0000 = Bit 0 … 1111 = Bit 15
R12291 (3003h) Write Sequencer 3	8	WSEQ_EOS0	0	End of Sequence flag. This bit indicates whether the Control Write Sequencer should stop after executing this step. 0 = Not end of sequence 1 = End of sequence (Stop the sequencer after this step).
	3:0	WSEQ_DELA Y0 [3:0]	0000	Time delay after executing this step. Total time per step (including execution) = 62.5µs × (2^{WSEQ_DELAY} + 8)

Table 81 Write Sequencer Control - Programming a Sequence

Note that a 'Dummy' write can be inserted into a control sequence by commanding the sequencer to write a value of 0 to bit 0 of Register R255 (00FFh). This is effectively a write to a non-existent register location. This can be used in order to create placeholders ready for easy adaptation of a control sequence. For example, a sequence could be defined to power-up a mono signal path from DACL to headphone, with a 'dummy' write included to leave space for easy modification to a stereo signal path configuration. Dummy writes can also be used in order to implement additional time delays between register writes.

In summary, the Control Register to be written is set by the WSEQ_ADDR*n* field. The data bits that are written are determined by a combination of WSEQ_DATA_START*n*, WSEQ_DATA_WIDTH*n* and WSEQ_DATA*n*. This is illustrated below for an example case of writing to the INL_MODE field within Register R18 (0012h).

In this example, the Start Position is bit 02 (WSEQ_DATA_START*n* = 0010b) and the Data width is 2 bits (WSEQ_DATA_WIDTH*n* = 0001b). With these settings, the Control Write Sequencer would update the Control Register R18 [3:2] with the contents of WSEQ_DATA*n* [1:0].

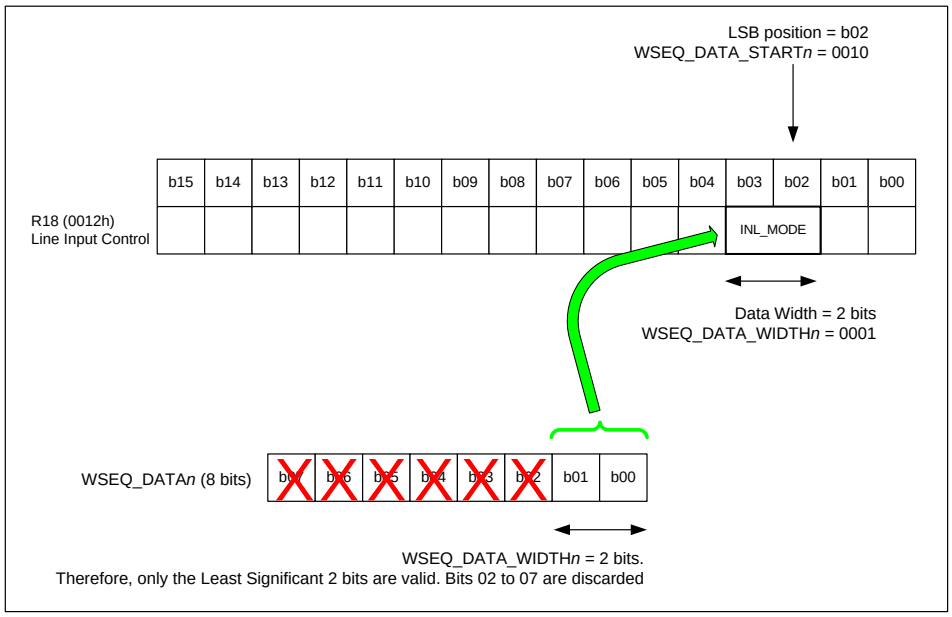


Figure 54 Control Write Sequencer Example

DEFAULT SEQUENCES

When the WM8915 is powered up, a number of Control Write Sequences are available through default settings in the sequencer memory locations. The pre-programmed default settings include Start-Up and Shut-Down sequences for each of the headphone output drivers. Note that the default sequences do not include audio signal path or gain setting configuration; this must be implemented prior to scheduling any of the default Start-Up sequences.

The entire sequencer memory may be programmed to users' own settings at any time, as described in "Programming a Sequence". Users' own settings remain in memory regardless of WSEQ_ENA, and are not affected by software resets (i.e. writing to Register R0). However, any non-default sequences are lost when the device is powered down.

The following default control sequences are provided:

1. Headphone 1 Cold Start-Up - This sequence powers up the HPOUT1L and HPOUT1R headphone drivers and charge pump. It commands the DC Servo to perform offset correction. It enables the master bias required for analogue functions. This sequence is intended for enabling the headphone output after initial power-on, when DC offset correction has not previously been run.

2. Headphone 1 Warm Start-Up - This sequence is similar to the Headphone 1 Cold Start-Up, but does not include the DC Servo operation. This sequence is intended for fast enabling of the headphone output when DC offset correction has previously been scheduled and provided the analogue gain settings have not been updated since scheduling the DC offset correction.

3. Headphone 2 Cold Start-Up - This sequence powers up the HPOUT2L and HPOUT2R headphone drivers and charge pump. It commands the DC Servo to perform offset correction. It enables the master bias required for analogue functions. This sequence is intended for enabling the headphone output after initial power-on, when DC offset correction has not previously been run.

4. Headphone 2 Warm Start-Up - This sequence is similar to the Headphone 2 Cold Start-Up, but does not include the DC Servo operation. This sequence is intended for fast enabling of the headphone output when DC offset correction has previously been scheduled and provided the analogue gain settings have not been updated since scheduling the DC offset correction.

5. Headphone 1 Shut-Down - This sequence powers down the HPOUT1L and HPOUT1R headphone drivers. The DC Servo is disabled on these channels, but the Charge Pump remains enabled.

6. Headphone 2 Shut-Down - This sequence powers down the HPOUT2L and HPOUT2R headphone drivers. The DC Servo is disabled on these channels, but the Charge Pump remains enabled.

7. Headphone 1 & 2 Shut-Down - This sequence powers down all of the headphone drivers and DC Servo channels. The Charge Pump and Bandgap reference are also disabled.

Specific details of each of these sequences is provided below.

Headphone 1 Cold Start-Up

The Headphone 1 Cold Start-Up sequence is initiated by writing 8100h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 0 (00h) and executes the sequence defined in Table 82.

This sequence takes approximately 76ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
0 (00h)	R1 (0001h)	1 bit	Bit 0	01h	6h	0b	BG_ENA = 1 (delay = 4.5ms)
1 (01h)	R64 (0040h)	1 bit	Bit 15	01h	6h	0b	CP_ENA = 1 (delay = 4.5ms)
2 (02h)	R1 (0001h)	2 bits	Bit 4	03h	0h	0b	HPOUT1L_ENA = 1 HPOUT1R_ENA = 1 (delay = 0.5625ms)
3 (03h)	R96 (0060h)	5 bits	Bit 1	11h	0h	0b	HPOUT1L_DLY = 1 HPOUT1R_DLY = 1 (delay = 0.5625ms)
4 (04h)	R80 (0050h)	2 bits	Bit 0	03h	0h	0b	DCS_ENA_CHAN_1 = 1 DCS_ENA_CHAN_0 = 1 (delay = 0.5625ms)
5 (05h)	R81 (0051h)	2 bits	Bit 4	03h	Ah	0b	DCS_TRIG_STARTUP_1 = 1 DCS_TRIG_STARTUP_0 = 1 (delay = 64.5ms)
6 (06h)	R96 (0060h)	6 bits	Bit 2	3Bh	0h	1b	HPOUT1L_RMV_SHORT = 1 HPOUT1L_OUTP = 1 HPOUT1R_RMV_SHORT = 1 HPOUT1R_OUTP = 1 (delay = 0.5625ms)

Table 82 Headphone 1 Cold Start-Up Default Sequence

Headphone 1 Warm Start-Up

The Headphone 1 Warm Start-Up sequence can be initiated by writing 8110h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 16 (10h) and executes the sequence defined in Table 83.

This sequence takes approximately 12ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
16 (10h)	R1 (0001h)	1 bit	Bit 0	01h	6h	0b	BG_ENA = 1 (delay = 4.5ms)
17 (11h)	R64 (0040h)	1 bit	Bit 15	01h	6h	0b	CP_ENA = 1 (delay = 4.5ms)
18 (12h)	R1 (0001h)	2 bits	Bit 4	03h	0h	0b	HPOUT1L_ENA = 1 HPOUT1R_ENA = 1 (delay = 0.5625ms)
19 (13h)	R96 (0060h)	5 bits	Bit 1	11h	0h	0b	HPOUT1L_DLY = 1 HPOUT1R_DLY = 1 (delay = 0.5625ms)
20 (14h)	R80 (0050h)	2 bits	Bit 0	03h	0h	0b	DCS_ENA_CHAN_1 = 1 DCS_ENA_CHAN_0 = 1 (delay = 0.5625ms)
21 (15h)	R96 (0060h)	6 bits	Bit 2	3Bh	0h	1b	HPOUT1L_RMV_SHORT = 1 HPOUT1L_OUTP = 1 HPOUT1R_RMV_SHORT = 1 HPOUT1R_OUTP = 1 (delay = 0.5625ms)

Table 83 Headphone 1 Warm Start-Up Default Sequence

Headphone 2 Cold Start-Up

The Headphone 2 Cold Start-Up sequence can be initiated by writing 8120h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 32 (20h) and executes the sequence defined in Table 84.

This sequence takes approximately 76ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
32 (20h)	R1 (0001h)	1 bit	Bit 0	01h	6h	0b	BG_ENA = 1 (delay = 4.5ms)
33 (21h)	R64 (0040h)	1 bit	Bit 15	01h	6h	0b	CP_ENA = 1 (delay = 4.5ms)
34 (22h)	R1 (0001h)	2 bits	Bit 6	03h	0h	0b	HPOUT2L_ENA = 1 HPOUT2R_ENA = 1 (delay = 0.5625ms)
35 (23h)	R97 (0061h)	5 bits	Bit 1	11h	0h	0b	HPOUT2L_DLY = 1 HPOUT2R_DLY = 1 (delay = 0.5625ms)
36 (24h)	R80 (0050h)	2 bits	Bit 2	03h	0h	0b	DCS_ENA_CHAN_3 = 1 DCS_ENA_CHAN_2 = 1 (delay = 0.5625ms)
37 (25h)	R81 (0051h)	2 bits	Bit 6	03h	Ah	0b	DCS_TRIG_STARTUP_3 = 1 DCS_TRIG_STARTUP_2 = 1 (delay = 64.5ms)

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
38 (26h)	R97 (0061h)	6 bits	Bit 2	3Bh	0h	1b	HPOUT2L_RMV_SHORT = 1 HPOUT2L_OUTP = 1 HPOUT2R_RMV_SHORT = 1 HPOUT2R_OUTP = 1 (delay = 0.5625ms)

Table 84 Headphone 2 Cold Start-Up Default Sequence

Headphone 2 Warm Start-Up

The Headphone 2 Warm Start-Up sequence can be initiated by writing 8130h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 48 (30h) and executes the sequence defined in Table 86.

This sequence takes approximately 12ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
48 (30h)	R1 (0001h)	1 bit	Bit 0	01h	6h	0b	BG_ENA = 1 (delay = 4.5ms)
49 (31h)	R64 (0040h)	1 bit	Bit 15	01h	6h	0b	CP_ENA = 1 (delay = 4.5ms)
50 (32h)	R1 (0001h)	2 bits	Bit 6	03h	0h	0b	HPOUT2L_ENA = 1 HPOUT2R_ENA = 1 (delay = 0.5625ms)
51 (33h)	R97 (0061h)	5 bits	Bit 1	11h	0h	0b	HPOUT2L_DLY = 1 HPOUT2R_DLY = 1 (delay = 0.5625ms)
52 (34h)	R80 (0050h)	2 bits	Bit 2	03h	0h	0b	DCS_ENA_CHAN_3 = 1 DCS_ENA_CHAN_2 = 1 (delay = 0.5625ms)
53 (35h)	R97 (0061h)	6 bits	Bit 2	3Bh	0h	1b	HPOUT2L_RMV_SHORT = 1 HPOUT2L_OUTP = 1 HPOUT2R_RMV_SHORT = 1 HPOUT2R_OUTP = 1 (delay = 0.5625ms)

Table 85 Headphone 2 Warm Start-Up Default Sequence

Headphone 1 Shut-Down

The Headphone 1 Shut-Down sequence can be initiated by writing 8140h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 64 (40h) and executes the sequence defined in Table 86.

This sequence takes approximately 2ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
64 (40h)	R96 (0060h)	7 bits	Bit 1	00h	0h	0b	HPOUT1L_RMV_SHORT = 0 HPOUT1L_OUTP = 0 HPOUT1L_DLY = 0 HPOUT1R_RMV_SHORT = 0 HPOUT1R_OUTP = 0 HPOUT1R_DLY = 0 (delay = 0.5625ms)
65 (41h)	R80 (0050h)	2 bits	Bit 0	00h	0h	0b	DCS_ENA_CHAN_1 = 0 DCS_ENA_CHAN_0 = 0 (delay = 0.5625ms)
66 (42h)	R1 (0001h)	2 bits	Bit 4	00h	0h	1b	HPOUT1L_ENA = 0 HPOUT1R_ENA = 0 (delay = 0.5625ms)

Table 86 Headphone 1 Shut-Down Default Sequence

Headphone 2 Shut-Down

The Headphone 2 Shut-Down sequence can be initiated by writing 8150h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 80 (50h) and executes the sequence defined in Table 87.

This sequence takes approximately 2ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
80 (50h)	R97 (0061h)	7 bits	Bit 1	00h	0h	0b	HPOUT2L_RMV_SHORT = 0 HPOUT2L_OUTP = 0 HPOUT2L_DLY = 0 HPOUT2R_RMV_SHORT = 0 HPOUT2R_OUTP = 0 HPOUT2R_DLY = 0 (delay = 0.5625ms)
81 (51h)	R80 (0050h)	2 bits	Bit 2	00h	0h	0b	DCS_ENA_CHAN_3 = 0 DCS_ENA_CHAN_2 = 0 (delay = 0.5625ms)
82 (52h)	R1 (0001h)	2 bits	Bit 6	00h	0h	1b	HPOUT2L_ENA = 0 HPOUT2R_ENA = 0 (delay = 0.5625ms)

Table 87 Headphone 2 Shut-Down Default Sequence

Headphone 1 and 2 Shut-Down

The Headphone 1 and 2 Shut-Down sequence can be initiated by writing 8160h to Register 272 (0110h). This single operation starts the Control Write Sequencer at Index Address 96 (60h) and executes the sequence defined in Table 88.

This sequence takes approximately 4ms to run.

WSEQ INDEX	REGISTER ADDRESS	WIDTH	START	DATA	DELAY	EOS	DESCRIPTION
96 (60h)	R96 (0060h)	7 bits	Bit 1	00h	0h	0b	HPOUT1L_RMV_SHORT = 0 HPOUT1L_OUTP = 0 HPOUT1L_DLY = 0 HPOUT1R_RMV_SHORT = 0 HPOUT1R_OUTP = 0 HPOUT1R_DLY = 0 (delay = 0.5625ms)
97 (61h)	R97 (0061h)	7 bits	Bit 1	00h	0h	0b	HPOUT2L_RMV_SHORT = 0 HPOUT2L_OUTP = 0 HPOUT2L_DLY = 0 HPOUT2R_RMV_SHORT = 0 HPOUT2R_OUTP = 0 HPOUT2R_DLY = 0 (delay = 0.5625ms)
98 (62h)	R80 (0050h)	4 bits	Bit 0	00h	0h	0b	DCS_ENA_CHAN_3 = 0 DCS_ENA_CHAN_2 = 0 DCS_ENA_CHAN_1 = 0 DCS_ENA_CHAN_0 = 0 (delay = 0.5625ms)
99 (63h)	R1 (0001h)	4 bits	Bit 4	00h	0h	0b	HPOUT2L_ENA = 0 HPOUT2R_ENA = 0 HPOUT1L_ENA = 0 HPOUT1R_ENA = 0 (delay = 0.5625ms)
100 (64h)	R64 (0040h)	1 bit	Bit 15	00h	0h	0b	CP_ENA = 0 (delay = 0.5625ms)
101 (65h)	R1 (0001h)	1 bit	Bit 0	00h	0h	1b	BG_ENA = 0 (delay = 0.5625ms)

Table 88 Headphone 1 and 2 Shut-Down Default Sequence

LDO REGULATORS

The WM8915 provides two integrated Low Drop-Out Regulators (LDOs). These are provided in order to generate the appropriate power supplies for internal circuits, simplifying and reducing the requirements for external supplies and associated components. A reference circuit powered by AVDD2 ensures the accuracy of the LDO regulator voltage settings.

LDO1 is intended for generating the DCVDD power domain which supplies the digital core functions on the WM8915. LDO1 is powered by DBVDD and is enabled when a logic '1' is applied to the LDO1ENA pin. The logic level is determined with respect to the DBVDD voltage domain.

The LDO1 start-up time is dependent on the external DCVDD and VREFC capacitors; see "Electrical Characteristics" for details of the start-up time under recommended external component conditions.

A pull-down resistor is provided on the LDO1ENA pin; this is configurable using the LDO1ENA_PD register. The pull-down resistor is enabled by default.

When LDO1 is enabled, the output voltage is controlled by the LDO1_VSEL register field.

When LDO1 is disabled, the output can be left floating or can be actively discharged, depending on the LDO1_DISCH control bit.

For normal operation of LDO1, the bandgap reference must be enabled (see “Reference Voltages and Master Bias”). If the bandgap reference is not enabled, then LDO1 operates in bypass mode; LDO1 is bypassed and DCVDD is connected directly to DBVDD.

It is possible to supply DCVDD from an external supply. If DCVDD is supplied externally, then LDO1 should be disabled, and the LDO1 output left floating (LDO1_DISCH = 0). Note that the DBVDD1 voltage must be greater than or equal to DCVDD; this ensures that there is no leakage path through the LDO for the external supply.

LDO2 is intended for generating MICVDD - the bias voltage for external microphones (analogue or digital). The MICVDD domain also provides power for the accessory detection circuit - see “External Accessory Detection”. LDO2 is powered by AVDD1 and is enabled using the LDO2_ENA register bit.

The LDO2 start-up time is dependent on the external MICVDD and VREFC capacitors; see “Electrical Characteristics” for details of the start-up time under recommended external component conditions.

When LDO2 is enabled, the output voltage is controlled by the LDO2_VSEL register field. Note that the AVDD1 voltage must be at least 300mV higher than the desired LDO2 output voltage.

When LDO2 is disabled, the output can be left floating or can be actively discharged, depending on the LDO2_DISCH control bit.

For normal operation of LDO2, the bandgap reference must be enabled (see “Reference Voltages and Master Bias”). If the bandgap reference is not enabled, then LDO2 operates in bypass mode; LDO2 is bypassed and MICVDD is connected directly to AVDD1.

It is possible to supply MICVDD from an external supply. If MICVDD is supplied externally, then LDO2 should be disabled, and the LDO2 output left floating (LDO2_DISCH = 0). Note that the AVDD1 voltage must be greater than or equal to MICVDD; this ensures that there is no leakage path through the LDO for the external supply.

In normal operation, both LDOs use the bandgap reference (see “Reference Voltages and Master Bias”). When the bandgap is disabled, the LDOs operate in bypass mode, where the LDO input is connected directly to the LDO output. The operating mode of the LDOs is reported via the read-only LDO1_MODE and LDO2_MODE registers, as described in Table 89.

Decoupling capacitors should be connected to the voltage reference pin, VREFC, and also to the LDO outputs - MICVDD and DCVDD. See “Applications Information” for further details.

The LDO Regulator connections and controls are illustrated in Figure 55. The register controls are defined in Table 89.

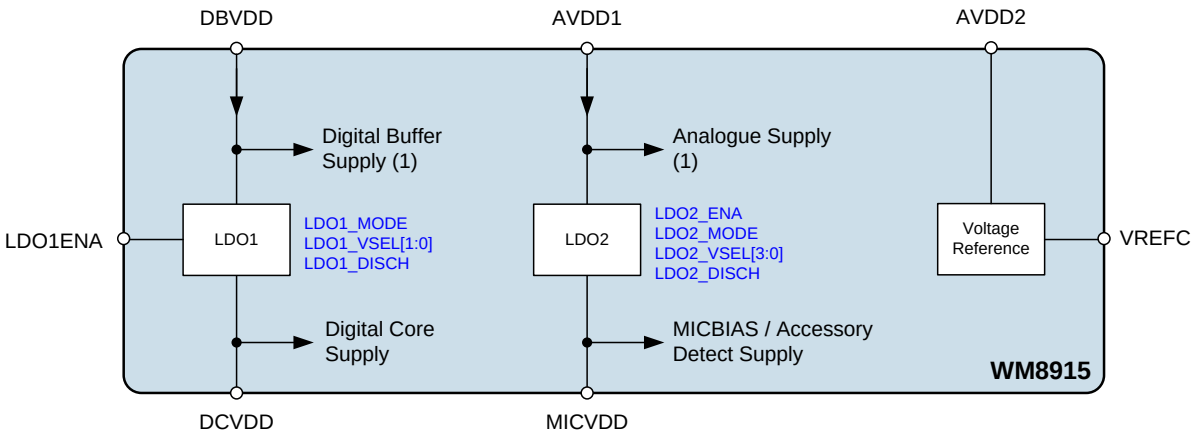


Figure 55 LDO Regulators

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (0002h) Power Management (2)	1	LDO2_ENA	0	LDO2 Enable 0 = Disabled 1 = Enabled
R40 (0028h) LDO 1	5	LDO1_MODE	0	LDO1 Mode (read only) 0 = Regulator mode (DCVDD is controlled by LDO1_VSEL) 1 = Bypass mode (DCVDD is connected to DBVDD)
	2:1	LDO1_VSEL [1:0]	01	LDO1 Output Voltage Select 0.9V to 1.2V in 100mV steps 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
	0	LDO1_DISCH	1	LDO1 Discharge Select 0 = LDO1 floating when disabled 1 = LDO1 discharged when disabled
R41 (0029h) LDO 2	5	LDO2_MODE	0	LDO2 Mode (read only) 0 = Regulator mode (MICVDD is controlled by LDO2_VSEL) 1 = Bypass mode (MICVDD is connected to AVDD1)
	4:1	LDO2_VSEL [3:0]	1001	LDO2 Output Voltage Select 1.7V to in 100mV steps 0000 = 1.7V 0001 = 1.8V 0010 = 1.9V 0011 = 2.0V 0100 = 2.1V 0101 = 2.2V 0110 = 2.3V 0111 = 2.4V 1000 = 2.5V 1001 = 2.6V 1010 = 2.7V 1011 = 2.8V 1100 to 1111 = Reserved
	0	LDO2_DISCH	1	LDO2 Discharge Select 0 = LDO2 floating when disabled 1 = LDO2 discharged when disabled
R1825 (0721h) Pull Control (2)	8	LDO1ENA_PD	1	LDO1ENA Pull-down enable 0 = Disabled 1 = Enabled

Table 89 LDO Regulator Control

REFERENCE VOLTAGES AND MASTER BIAS

The analogue circuits in the WM8915 require a reference voltage, VREF. This reference is connected to the VREFC pin for external decoupling, as described in the “Applications Information” section. The analogue circuits in the WM8915 also require a bias current.

The reference voltage and bias circuits use an internal bandgap reference, which is enabled using the BG_ENA register bit.

For normal operation, the bandgap reference must be enabled (BG_ENA = 1).

When the bandgap is enabled, a delay of 1ms should be allowed for bandgap start-up before enabling other circuits that use the bandgap reference. Note that this delay is particularly important before enabling the Frequency Locked Loop (FLL) circuit (see “Clocking and Sample Rates”).

Note that Microphone / Accessory detection functions can still be supported when the bandgap reference is disabled. This allows reduced power consumption in a low-power standby state when BG_ENA = 0. See “External Accessory Detection” for details of the Microphone / Accessory detection functions.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (0001h) Power Management (1)	0	BG_ENA	0	Internal Bandgap Reference Enable (required for normal operation) 0 = Disabled 1 = Enabled Note that the Microphone / Accessory detect function can be supported when BG_ENA = 0.

Table 90 Internal Bandgap Reference Control

POWER MANAGEMENT

The WM8915 has control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To minimise pop or click noise, it is important to enable or disable functions in the correct order. See “Control Write Sequencer” for details of default control sequences.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (0001h) Power Management (1)	9	MICB2_ENA	0	Microphone Bias 2 Enable 0 = Disabled 1 = Enabled
	8	MICB1_ENA	0	Microphone Bias 1 Enable 0 = Disabled 1 = Enabled
	7	HPOUT2L_ENA	0	Enables HPOUT2L input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT2L Enable sequence.
	6	HPOUT2R_ENA	0	Enables HPOUT2R input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT2R Enable sequence.
	5	HPOUT1L_ENA	0	Enables HPOUT1L input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT1L

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				Enable sequence.
	4	HPOUT1R_ENA	0	Enables HPOUT1R input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT1R Enable sequence.
	0	BG_ENA	0	Internal Bandgap Reference Enable (required for normal operation) 0 = Disabled 1 = Enabled Note that the Microphone / Accessory detect function can be supported when BG_ENA = 0.
R2 (0002h) Power Management (2)	11	OPCLK_ENA	0	GPIO Clock Output (OPCLK) Enable 0 = Disabled 1 = Enabled
	5	INL_ENA	0	INL Input PGA Enable 0 = Disabled 1 = Enabled
	4	INR_ENA	0	INR Input PGA Enable 0 = Disabled 1 = Enabled
	1	LDO2_ENA	0	LDO2 Enable 0 = Disabled 1 = Enabled
R3 (0003h) Power Management (3)	11	DSP2RXL_ENA	0	Enable DSP2 (Left) input path 0 = Disabled 1 = Enabled
	10	DSP2RXR_ENA	0	Enable DSP2 (Right) input path 0 = Disabled 1 = Enabled
	9	DSP1RXL_ENA	0	Enable DSP1 (Left) input path 0 = Disabled 1 = Enabled
	8	DSP1RXR_ENA	0	Enable DSP1 (Right) input path 0 = Disabled 1 = Enabled
	5	DMIC2L_ENA	0	Digital microphone DMICDAT2 Left channel enable 0 = Disabled 1 = Enabled
	4	DMIC2R_ENA	0	Digital microphone DMICDAT2 Right channel enable 0 = Disabled 1 = Enabled
	3	DMIC1L_ENA	0	Digital microphone DMICDAT1 Left channel enable 0 = Disabled 1 = Enabled
	2	DMIC1R_ENA	0	Digital microphone DMICDAT1 Right channel enable 0 = Disabled 1 = Enabled
	1	ADCL_ENA	0	Left ADC Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				0 = ADC disabled 1 = ADC enabled
	0	ADCR_ENA	0	Right ADC Enable 0 = ADC disabled 1 = ADC enabled
R4 (0004h) Power Management (4)	9	AIF2RX_CHAN1_ ENA	0	Enable AIF2 input channel 1 0 = Disabled 1 = Enabled
	8	AIF2RX_CHAN0_ ENA	0	Enable AIF2 input channel 0 0 = Disabled 1 = Enabled
	5	AIF1RX_CHAN5_ ENA	0	Enable AIF1 input channel 5 0 = Disabled 1 = Enabled
	4	AIF1RX_CHAN4_ ENA	0	Enable AIF1 input channel 4 0 = Disabled 1 = Enabled
	3	AIF1RX_CHAN3_ ENA	0	Enable AIF1 input channel 3 0 = Disabled 1 = Enabled
	2	AIF1RX_CHAN2_ ENA	0	Enable AIF1 input channel 2 0 = Disabled 1 = Enabled
	1	AIF1RX_CHAN1_ ENA	0	Enable AIF1 input channel 1 0 = Disabled 1 = Enabled
	0	AIF1RX_CHAN0_ ENA	0	Enable AIF1 input channel 0 0 = Disabled 1 = Enabled
R5 (0005h) Power Management (5)	11	DSP2TXL_ENA	0	Enable DSP2 (Left) output path 0 = Disabled 1 = Enabled
	10	DSP2TXR_ENA	0	Enable DSP2 (Right) output path 0 = Disabled 1 = Enabled
	9	DSP1TXL_ENA	0	Enable DSP1 (Left) output path 0 = Disabled 1 = Enabled
	8	DSP1TXR_ENA	0	Enable DSP1 (Right) output path 0 = Disabled 1 = Enabled
	3	DAC2L_ENA	0	Left DAC2 Enable 0 = DAC disabled 1 = DAC enabled
	2	DAC2R_ENA	0	Right DAC2 Enable 0 = DAC disabled 1 = DAC enabled
	1	DAC1L_ENA	0	Left DAC1 Enable 0 = DAC disabled 1 = DAC enabled
	0	DAC1R_ENA	0	Right DAC1 Enable 0 = DAC disabled 1 = DAC enabled
R6 (0006h)	9	AIF2TX_CHAN1_	0	Enable AIF2 output channel 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Power Management (6)		ENA		0 = Disabled 1 = Enabled
	8	AIF2TX_CHAN1_ENA	0	Enable AIF2 output channel 0 0 = Disabled 1 = Enabled
	5	AIF1TX_CHAN5_ENA	0	Enable AIF1 output channel 5 0 = Disabled 1 = Enabled
	4	AIF1TX_CHAN4_ENA	0	Enable AIF1 output channel 4 0 = Disabled 1 = Enabled
	3	AIF1TX_CHAN3_ENA	0	Enable AIF1 output channel 3 0 = Disabled 1 = Enabled
	2	AIF1TX_CHAN2_ENA	0	Enable AIF1 output channel 2 0 = Disabled 1 = Enabled
	1	AIF1TX_CHAN1_ENA	0	Enable AIF1 output channel 1 0 = Disabled 1 = Enabled
	0	AIF1TX_CHAN0_ENA	0	Enable AIF1 output channel 0 0 = Disabled 1 = Enabled
R56 (0038h) Mic Detect 1	0	MICD_ENA	0	Mic Detect Enable 0 = Disabled 1 = Enabled
R64 (0040h) Charge Pump (1)	15	CP_ENA	0	Charge Pump Enable 0 = Disabled 1 = Enabled
R80 (0050h) DC Servo (1)	3	DCS_ENA_CHAN_3	0	DC Servo enable for HPOUT2R 0 = Disabled 1 = Enabled
	2	DCS_ENA_CHAN_2	0	DC Servo enable for HPOUT2L 0 = Disabled 1 = Enabled
	1	DCS_ENA_CHAN_1	0	DC Servo enable for HPOUT1R 0 = Disabled 1 = Enabled
	0	DCS_ENA_CHAN_0	0	DC Servo enable for HPOUT1L 0 = Disabled 1 = Enabled
R272 (0110h) Write Sequencer Ctrl (1)	8	WSEQ_ENA	0	Write Sequencer Enable 0 = Disabled 1 = Enabled
R512 (0200h) AIF Clocking (1)	0	SYSCLK_ENA	0	SYSCLK Enable 0 = Disabled 1 = Enabled
R520 (0208h) Clocking (1)	4	TOCLK_ENA	0	Slow Clock (TOCLK) Enable 0 = Disabled 1 = Enabled This clock is required for zero-cross timeout.
	2	AIFCLK_ENA	0	AIFCLK Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				0 = Disabled 1 = Enabled
	1	SYSDSPCLK_ENA	0	DSP1 and DSP2 Clock Enable 0 = Disabled 1 = Enabled
R544 (0220h) FLL Control (1)	0	FLL_ENA	0	FLL Enable 0 = Disabled 1 = Enabled

Table 91 Power Management

POWER ON RESET

The WM8915 will remain in the reset state until DCVDD and DBVDD are supplied. The reset threshold for DCVDD is nominally 0.6V; the reset threshold for DBVDD is nominally 1.2V.

Provided both of these reset thresholds are exceeded, then it is possible to communicate with the WM8915 using the control interface. All other blocks will remain in reset until the respective supplies are above 1.2V.

Note that specified device performance is not assured outside the voltage ranges defined in the "Recommended Operating Conditions" section.

Table 92 describes the status of the WM8915 input and output pins when the Power On Reset has completed, prior to any register writes. The same conditions apply on completion of a Software Reset (described in the following section).

PIN NO	NAME	TYPE	RESET STATUS
A1	LDO1ENA	Digital Input	Pull-down to DBGND
A2	IN2RN/ DMICDAT2	Analogue Input / Digital Input	High impedance input
A3	IN2LN/ DMICDAT1	Analogue Input / Digital Input	High impedance input
A4	MICVDD	Supply / Analogue Output	N/A
A5	IN1LN	Analogue Input	High impedance input
A6	AVDD2	Supply	N/A
A7	IN1RN	Analogue Input	High impedance input
B1	DCVDD	Supply / Analogue Output	N/A
B2	IN2RP/ DMICCLK2	Analogue Input / Digital Output	High impedance input
B3	IN2LP/ DMICCLK1	Analogue Input / Digital Output	High impedance input
B4	MICBIAS2	Analogue Output	Pull-down to AGND
B5	AGND	Supply	N/A
B6	VREFC	Analogue Output	N/A
B7	HPDETR	Analogue Input / Output	High impedance input
C1	SPKCLK	Digital Output	Pull-down to DBGND
C2	SPKDAT	Digital Output	Pull-down to DBGND
C3	MICBIAS1	Analogue Output	Pull-down to AGND
C4	IN1LP	Analogue Input	High impedance input
C5	IN1RP	Analogue Input	High impedance input
C6	HPDETL	Analogue Input / Output	High impedance input
C7	HPOUT1FB1/ MICDET2	Analogue Input	High impedance input
D1	ADCDAT1	Digital Output	Undriven high impedance output
D2	ADCDAT2	Digital Output	Undriven high impedance output

PIN NO	NAME	TYPE	RESET STATUS
D5	AVDD1	Supply	N/A
D6	MICDET1/ HPOUT1FB2	Analogue Input	High impedance input
D7	HPOUT1R	Analogue Output	Pull-down to AGND
E1	SCLK	Digital Input	High impedance input
E2	DBVDD	Supply	N/A
E6	HPOUT1L	Analogue Output	Pull-down to AGND
E7	HPOUT2R	Analogue Output	Pull-down to AGND
F1	MCLK2	Digital Input	High impedance input
F2	ADDR	Digital Input	Pull-down to DBGND
F6	HPOUT2FB	Analogue Input	High impedance input
F7	HPOUT2L	Analogue Output	Pull-down to AGND
G1	DACDAT1	Digital Input	High impedance input
G2	DACDAT2	Digital Input	High impedance input
G3	MCLK1	Digital Input	High impedance input
G5	GPIO1/ ADCLRCLK1	Digital Input / Output	Pull-down to DBGND
G6	CPVOUTP	Analogue Output	N/A
G7	CPVOUTN	Analogue Output	N/A
H1	GPIO3	Digital Input / Output	Pull-down to DBGND
H2	SDA	Digital Input / Output	High impedance input
H3	BCLK2	Digital Input / Output	High impedance input
H4	GPIO2/ ADCLRCLK2	Digital Input / Output	Pull-down to DBGND
H5	BCLK1	Digital Input / Output	High impedance input
H6	CPCB	Analogue Output	N/A
H7	CPGND	Supply	N/A
J1	GPIO5	Digital Input / Output	Pull-down to DBGND
J2	GPIO4	Digital Input / Output	Pull-down to DBGND
J3	DACLRCLK2	Digital Input / Output	High impedance input
J4	DGND	Supply	N/A
J5	DACLRCLK1	Digital Input / Output	High impedance input
J6	CPVDD	Supply	N/A
J7	CPCA	Analogue Output	N/A

Table 92 WM8915 Pin Status in Reset State

SOFTWARE RESET AND CHIP ID

The Chip ID can be read back from Register R0. Writing to this register will reset the device.

The software reset causes most control registers to be reset to their default state. Note that the Control Write Sequencer registers R12288 (3000h) through to R12799 (31FFh) are not affected by a software reset; the Control Sequences defined in these registers are retained unchanged.

The status of the WM8915 input and output pins following a software reset is described in Table 92.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (0000h) Software Reset	15:0	SW_RESET [15:0]	8915h	Writing to this register resets all registers to their default state. (Note - Control Write Sequencer registers are not affected by Software Reset.) Reading from this register will indicate Chip ID 8915h.

Table 93 Chip Reset and ID

REGISTER MAP

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R0 (0h)	Software Reset	SW_RESET [15:0]																0000h
R1 (1h)	Power Management (1)	0	0	0	0	0	0	MICB2_ENA	MICB1_ENA	HPOUT2L_ENA	HPOUT2R_ENA	HPOUT1L_ENA	HPOUT1R_ENA	0	0	0	BG_ENA	0000h
R2 (2h)	Power Management (2)	0	0	0	0	OPCLK_ENA	0	0	0	0	0	INL_ENA	INR_ENA	0	0	LDO2_ENA	0	0000h
R3 (3h)	Power Management (3)	0	0	0	0	DSP2RXL_ENA	DSP2RXR_ENA	DSP1RXL_ENA	DSP1RXR_ENA	0	0	DMIC2L_ENA	DMIC2R_ENA	DMIC1L_ENA	DMIC1R_ENA	ADCL_ENA	ADCR_ENA	0000h
R4 (4h)	Power Management (4)	0	0	0	0	0	0	AIF2RX_CHAN1_ENA	AIF2RX_CHAN0_ENA	0	0	AIF1RX_CHAN5_ENA	AIF1RX_CHAN4_ENA	AIF1RX_CHAN3_ENA	AIF1RX_CHAN2_ENA	AIF1RX_CHAN1_ENA	AIF1RX_CHAN0_ENA	0000h
R5 (5h)	Power Management (5)	0	0	0	0	DSP2TXL_ENA	DSP2TXR_ENA	DSP1TXL_ENA	DSP1TXR_ENA	0	0	0	0	DAC2L_ENA	DAC2R_ENA	DAC1L_ENA	DAC1R_ENA	0000h
R6 (6h)	Power Management (6)	0	0	0	0	0	0	AIF2TX_CHAN1_ENA	AIF2TX_CHAN0_ENA	0	0	AIF1TX_CHAN5_ENA	AIF1TX_CHAN4_ENA	AIF1TX_CHAN3_ENA	AIF1TX_CHAN2_ENA	AIF1TX_CHAN1_ENA	AIF1TX_CHAN0_ENA	0000h
R7 (7h)	Power Management (7)	0	0	0	0	0	0	DMIC2_FN	DMIC1_FN	ADC_DMIC_DSP2R_ENA	ADC_DMIC_DSP2L_ENA	ADC_DMIC_SRC2 [1:0]		ADC_DMIC_DSP1R_ENA	ADC_DMIC_DSP1L_ENA	ADC_DMIC_SRC1 [1:0]		0010h
R8 (8h)	Power Management (8)	0	0	0	0	0	0	0	0	AIF2TX_SRC [1:0]		0	DSP2RX_SRC	0	0	0	DSP1RX_SRC	0000h
R16 (10h)	Left Line Input Volume	0	0	0	0	0	0	0	0	IN_VU	0	INL_ZC	INL_VOL [4:0]					0000h
R17 (11h)	Right Line Input Volume	0	0	0	0	0	0	0	0	IN_VU	0	INR_ZC	INR_VOL [4:0]					0000h
R18 (12h)	Line Input Control	0	0	0	0	0	0	0	0	0	0	0	0	INL_MODE [1:0]		INR_MODE [1:0]		0000h
R21 (15h)	DAC1 HPOUT1 Volume	0	0	0	0	0	0	0	0	DAC1R_HPOUT1R_VOL [3:0]				DAC1L_HPOUT1L_VOL [3:0]				0088h
R22 (16h)	DAC2 HPOUT2 Volume	0	0	0	0	0	0	0	0	DAC1R_HPOUT2R_VOL [3:0]				DAC1R_HPOUT2L_VOL [3:0]				0088h
R23 (17h)	Output Volume Control 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OUT_VOL_SHARED	0000h
R24 (18h)	DAC1 Left Volume	0	0	0	0	0	0	DAC1L_MUTE	DAC1_VU	DAC1L_VOL [7:0]								02C0h
R25 (19h)	DAC1 Right Volume	0	0	0	0	0	0	DAC1R_MUTE	DAC1_VU	DAC1R_VOL [7:0]								02C0h
R26 (1Ah)	DAC2 Left Volume	0	0	0	0	0	0	DAC2L_MUTE	DAC2_VU	DAC2L_VOL [7:0]								02C0h
R27 (1Bh)	DAC2 Right Volume	0	0	0	0	0	0	DAC2R_MUTE	DAC2_VU	DAC2R_VOL [7:0]								02C0h
R28 (1Ch)	Output1 Left Volume	0	0	0	0	0	0	0	DAC1_VU	HPOUT1L_ZC	0	0	0	HPOUT1L_VOL [3:0]				0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R29 (1Dh)	Output1 Right Volume	0	0	0	0	0	0	0	DAC1_VU	HPOUT1R_ZC	0	0	0	HPOUT1R_VOL [3:0]				0080h
R30 (1Eh)	Output2 Left Volume	0	0	0	0	0	0	0	DAC2_VU	HPOUT2L_ZC	0	0	0	HPOUT2L_VOL [3:0]				0080h
R31 (1Fh)	Output2 Right Volume	0	0	0	0	0	0	0	DAC2_VU	HPOUT2R_ZC	0	0	0	HPOUT2R_VOL [3:0]				0080h
R32 (20h)	MICBIAS (1)	0	0	0	0	0	0	0	0	0	0	MICB1_RATE	MICB1_MODE	MICB1_LVL [2:0]			MICB1_DISCH	0039h
R33 (21h)	MICBIAS (2)	0	0	0	0	0	0	0	0	0	0	MICB2_RATE	MICB2_MODE	MICB2_LVL [2:0]			MICB2_DISCH	0039h
R40 (28h)	LDO 1	0	0	0	0	0	0	0	0	0	0	LDO1_MODE	0	0	LDO1_VSEL [1:0]		LDO1_DISCH	0003h
R41 (29h)	LDO 2	0	0	0	0	0	0	0	0	0	0	LDO2_MODE	LDO2_VSEL [3:0]				LDO2_DISCH	0013h
R48 (30h)	Accessory Detect Mode 1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	JD_MODE [1:0]		0004h
R49 (31h)	Accessory Detect Mode 2	0	0	0	0	0	0	0	0	0	0	0	0	0	HPOUT1FB_SRC	MICD_SRC	MICD_BIAS_SRC	0000h
R52 (34h)	Headphone Detect 1	0	0	0	0	0	0	0	0	HP_HOLDTIME [2:0]			HP_CLK_DIV [1:0]		0	HP_STEP_SIZE	HP_POLL	0020h
R53 (35h)	Headphone Detect 2	0	0	0	0	0	0	0	0	HP_DONE	HP_LVL [6:0]							0000h
R56 (38h)	Mic Detect 1	MICD_BIAS_STARTTIME [3:0]				MICD_RATE [3:0]				0	0	0	0	0	0	MICD_DBTIME	MICD_ENA	7600h
R57 (39h)	Mic Detect 2	0	0	0	0	0	0	0	0	MICD_LVL_SEL [7:0]								00BFh
R58 (3Ah)	Mic Detect 3	0	0	0	0	0	MICD_LVL [8:0]									MICD_VALID	MICD_STS	0000h
R64 (40h)	Charge Pump (1)	CP_ENA	0	0	1	1	1	1	1	0	0	1	0	0	1	0	1	1F25h
R65 (41h)	Charge Pump (2)	CP_DISCH	0	1	0	1	0	1	1	0	0	0	1	1	0	0	1	AB19h
R80 (50h)	DC Servo (1)	0	0	0	0	0	0	0	0	0	0	0	0	DCS_ENA_CHAN_3	DCS_ENA_CHAN_2	DCS_ENA_CHAN_1	DCS_ENA_CHAN_0	0000h
R81 (51h)	DC Servo (2)	DCS_TRIG_SINGLE_3	DCS_TRIG_SINGLE_2	DCS_TRIG_SINGLE_1	DCS_TRIG_SINGLE_0	DCS_TRIG_SERIES_3	DCS_TRIG_SERIES_2	DCS_TRIG_SERIES_1	DCS_TRIG_SERIES_0	DCS_TRIG_START UP_3	DCS_TRIG_START UP_2	DCS_TRIG_START UP_1	DCS_TRIG_START UP_0	DCS_TRIG_DAC_WR_3	DCS_TRIG_DAC_WR_2	DCS_TRIG_DAC_WR_1	DCS_TRIG_DAC_WR_0	0000h
R82 (52h)	DC Servo (3)	0	0	0	0	DCS_TIMER_PERIOD_23 [3:0]				0	0	0	0	DCS_TIMER_PERIOD_01 [3:0]				0000h
R84 (54h)	DC Servo (5)	0	DCS_SERIES_NO_23 [6:0]							0	DCS_SERIES_NO_01 [6:0]							2A2Ah
R85 (55h)	DC Servo (6)	DCS_DAC_WR_VAL_3 [7:0]								DCS_DAC_WR_VAL_2 [7:0]								0000h
R86 (56h)	DC Servo (7)	DCS_DAC_WR_VAL_1 [7:0]								DCS_DAC_WR_VAL_0 [7:0]								0000h
R87 (57h)	DC Servo Readback 0	0	0	0	0	DCS_CAL_COMPLETE [3:0]				DCS_DAC_WR_COMPLETE [3:0]				DCS_STARTUP_COMPLETE [3:0]				0000h
R96 (60h)	Analogue HP (1)	0	0	0	0	0	0	0	0	HPOUT1L_RMV_SHORT	HPOUT1L_OUTP	HPOUT1L_DLY	0	HPOUT1R_RMV_SHORT	HPOUT1R_OUTP	HPOUT1R_DLY	0	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R97 (61h)	Analogue HP (2)	0	0	0	0	0	0	0	0	HPOUT2L_RMV_SHORT	HPOUT2L_OUTP	HPOUT2L_DLY	0	HPOUT2R_RMV_SHORT	HPOUT2R_OUTP	HPOUT2R_DLY	0	0000h
R256 (100h)	Chip Revision	0	0	0	0	0	0	0	0	0	0	0	0	CHIP_REV [3:0]				0000h
R257 (101h)	Control Interface (1)	REG_SYNC	0	0	0	0	0	0	0	0	0	0	0	0	AUTO_INC	0	0	8004h
R272 (110h)	Write Sequencer Ctrl (1)	WSEQ_ENA	0	0	0	0	0	WSEQ_ABORT	WSEQ_START	0	WSEQ_START_INDEX [6:0]							0000h
R273 (111h)	Write Sequencer Ctrl (2)	0	0	0	0	0	0	0	WSEQ_BUSY	0	WSEQ_CURRENT_INDEX [6:0]							0000h
R512 (200h)	AIF Clocking (1)	0	0	0	0	0	0	0	0	0	0	0	SYSCLK_SRC [1:0]		SYSCLK_INV	SYSCLK_DIV	SYSCLK_ENA	0000h
R513 (201h)	AIF Clocking (2)	0	0	0	0	0	0	0	0	0	0	0	DSP2_DIV [1:0]		0	DSP1_DIV [1:0]		0000h
R520 (208h)	Clocking (1)	0	0	0	0	0	0	0	0	0	0	LFCLK_ENA	TOCLK_ENA	0	AIFCLK_ENA	SYSDSPCLK_ENA	0	0010h
R521 (209h)	Clocking (2)	0	0	0	0	0	TOCLK_DIV [2:0]			DBCLK_DIV [3:0]				0	OPCLK_DIV [2:0]			0000h
R528 (210h)	AIF Rate	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SYSCLK_RATE	0001h
R544 (220h)	FLL Control (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL_OSC_ENA	FLL_ENA	0000h
R545 (221h)	FLL Control (2)	0	0	FLL_OUTDIV [5:0]						0	0	0	0	0	FLL_FRATIO [2:0]			0000h
R546 (222h)	FLL Control (3)	FLL_THETA [15:0]																0000h
R547 (223h)	FLL Control (4)	0	FLL_N [9:0]										0	FLL_LOOP_GAIN [3:0]				5DC0h
R548 (224h)	FLL Control (5)	0	0	0	FLL_FRC_NCO_VAL [5:0]					FLL_FRC_NCO	0	FLL_REFCLK_DIV [1:0]			FLL_REF_FREQ	FLL_REFCLK_SRC [1:0]		0C84h
R549 (225h)	FLL Control (6)	0	0	0	0	0	0	0	0	0	0	0	0	FLL_REFCLK_SRC_STS [1:0]		0	FLL_SWITCH_CLK	0000h
R550 (226h)	FLL EFS 1	FLL_LAMBDA [15:0]																0000h
R551 (227h)	FLL EFS 2	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL_LFSR_SEL [1:0]		FLL_EFS_ENA	0002h
R768 (300h)	AIF1 Control	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1_TRI	AIF1_FMT [1:0]		0000h
R769 (301h)	AIF1 BCLK	0	0	0	0	0	AIF1_BCLK_INV	AIF1_BCLK_FRC	AIF1_BCLK_MSTR	0	0	0	0	AIF1_BCLK_DIV [3:0]				0000h
R770 (302h)	AIF1 TX LRCLK(1)	0	0	0	0	0	AIF1TX_RATE [10:0]											0080h
R771 (303h)	AIF1 TX LRCLK(2)	0	0	0	0	0	0	0	0	0	0	0	0	AIF1TX_LRCLK_MODE	AIF1TX_LRCLK_INV	AIF1TX_LRCLK_FRC	AIF1TX_LRCLK_MSTR	0008h
R772 (304h)	AIF1 RX LRCLK(1)	0	0	0	0	0	AIF1RX_RATE [10:0]											0080h
R773 (305h)	AIF1 RX LRCLK(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1RX_LRCLK_INV	AIF1RX_LRCLK_FRC	AIF1RX_LRCLK_MSTR	0000h
R774 (306h)	AIF1TX Data Configuration (1)	AIF1TX_WL [7:0]								AIF1TX_SLOT_LEN [7:0]								1818h
R775 (307h)	AIF1TX Data Configuration (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1TX_DAT_TRI	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R776 (308h)	AIF1RX Data Configuration	AIF1RX_WL [7:0]								AIF1RX_SLOT_LEN [7:0]								1818h
R777 (309h)	AIF1TX Channel 0 Configuration	AIF1TX_CHAN0_DAT_INV	AIF1TX_CHAN0_SPACING [5:0]						AIF1TX_CHAN0_SLOTS [2:0]			AIF1TX_CHAN0_START_SLOT [5:0]						0000h
R778 (30Ah)	AIF1TX Channel 1 Configuration	AIF1TX_CHAN1_DAT_INV	AIF1TX_CHAN1_SPACING [5:0]						AIF1TX_CHAN1_SLOTS [2:0]			AIF1TX_CHAN1_START_SLOT [5:0]						0000h
R779 (30Bh)	AIF1TX Channel 2 Configuration	AIF1TX_CHAN2_DAT_INV	AIF1TX_CHAN2_SPACING [5:0]						AIF1TX_CHAN2_SLOTS [2:0]			AIF1TX_CHAN2_START_SLOT [5:0]						0000h
R780 (30Ch)	AIF1TX Channel 3 Configuration	AIF1TX_CHAN3_DAT_INV	AIF1TX_CHAN3_SPACING [5:0]						AIF1TX_CHAN3_SLOTS [2:0]			AIF1TX_CHAN3_START_SLOT [5:0]						0000h
R781 (30Dh)	AIF1TX Channel 4 Configuration	AIF1TX_CHAN4_DAT_INV	AIF1TX_CHAN4_SPACING [5:0]						AIF1TX_CHAN4_SLOTS [2:0]			AIF1TX_CHAN4_START_SLOT [5:0]						0000h
R782 (30Eh)	AIF1TX Channel 5 Configuration	AIF1TX_CHAN5_DAT_INV	AIF1TX_CHAN5_SPACING [5:0]						AIF1TX_CHAN5_SLOTS [2:0]			AIF1TX_CHAN5_START_SLOT [5:0]						0000h
R783 (30Fh)	AIF1RX Channel 0 Configuration	AIF1RX_CHAN0_DAT_INV	AIF1RX_CHAN0_SPACING [5:0]						AIF1RX_CHAN0_SLOTS [2:0]			AIF1RX_CHAN0_START_SLOT [5:0]						0000h
R784 (310h)	AIF1RX Channel 1 Configuration	AIF1RX_CHAN1_DAT_INV	AIF1RX_CHAN1_SPACING [5:0]						AIF1RX_CHAN1_SLOTS [2:0]			AIF1RX_CHAN1_START_SLOT [5:0]						0000h
R785 (311h)	AIF1RX Channel 2 Configuration	AIF1RX_CHAN2_DAT_INV	AIF1RX_CHAN2_SPACING [5:0]						AIF1RX_CHAN2_SLOTS [2:0]			AIF1RX_CHAN2_START_SLOT [5:0]						0000h
R786 (312h)	AIF1RX Channel 3 Configuration	AIF1RX_CHAN3_DAT_INV	AIF1RX_CHAN3_SPACING [5:0]						AIF1RX_CHAN3_SLOTS [2:0]			AIF1RX_CHAN3_START_SLOT [5:0]						0000h
R787 (313h)	AIF1RX Channel 4 Configuration	AIF1RX_CHAN4_DAT_INV	AIF1RX_CHAN4_SPACING [5:0]						AIF1RX_CHAN4_SLOTS [2:0]			AIF1RX_CHAN4_START_SLOT [5:0]						0000h
R788 (314h)	AIF1RX Channel 5 Configuration	AIF1RX_CHAN5_DAT_INV	AIF1RX_CHAN5_SPACING [5:0]						AIF1RX_CHAN5_SLOTS [2:0]			AIF1RX_CHAN5_START_SLOT [5:0]						0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R789 (315h)	AIF1RX Mono Configuration	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1RX_CHAN4_MONO_MODE	AIF1RX_CHAN2_MONO_MODE	AIF1RX_CHAN0_MONO_MODE	0000h
R794 (31Ah)	AIF1TX Test	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1TX45_DITHER_ENA	AIF1TX23_DITHER_ENA	AIF1TX01_DITHER_ENA	0007h
R800 (320h)	AIF2 Control	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2_TRI	AIF2_FMT [1:0]		0000h
R801 (321h)	AIF2 BCLK	0	0	0	0	0	AIF2_BCLK_INV	AIF2_BCLK_FRC	AIF2_BCLK_MSTR	0	0	0	0	AIF2_BCLK_DIV [3:0]				0000h
R802 (322h)	AIF2 TX LRCLK(1)	0	0	0	0	0	AIF2TX_RATE [10:0]											0080h
R803 (323h)	AIF2 TX LRCLK(2)	0	0	0	0	0	0	0	0	0	0	0	0	AIF2TX_LRCLK_MODE	AIF2TX_LRCLK_INV	AIF2TX_LRCLK_FRC	AIF2TX_LRCLK_MSTR	0008h
R804 (324h)	AIF2 RX LRCLK(1)	0	0	0	0	0	AIF2RX_RATE [10:0]											0080h
R805 (325h)	AIF2 RX LRCLK(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2RX_LRCLK_INV	AIF2RX_LRCLK_FRC	AIF2RX_LRCLK_MSTR	0000h
R806 (326h)	AIF2TX Data Configuration (1)	AIF2TX_WL [7:0]								AIF2TX_SLOT_LEN [7:0]								1818h
R807 (327h)	AIF2TX Data Configuration (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2TX_DAT_TRI	0000h
R808 (328h)	AIF2RX Data Configuration	AIF2RX_WL [7:0]								AIF2RX_SLOT_LEN [7:0]								1818h
R809 (329h)	AIF2TX Channel 0 Configuration	AIF2TX_CHAN0_DAT_INV	AIF2TX_CHAN0_SPACING [5:0]						AIF2TX_CHAN0_SLOTS [2:0]		AIF2TX_CHAN0_START_SLOT [5:0]							0000h
R810 (32Ah)	AIF2TX Channel 1 Configuration	AIF2TX_CHAN1_DAT_INV	AIF2TX_CHAN1_SPACING [5:0]						AIF2TX_CHAN1_SLOTS [2:0]		AIF2TX_CHAN1_START_SLOT [5:0]							0000h
R811 (32Bh)	AIF2RX Channel 0 Configuration	AIF2RX_CHAN0_DAT_INV	AIF2RX_CHAN0_SPACING [5:0]						AIF2RX_CHAN0_SLOTS [2:0]		AIF2RX_CHAN0_START_SLOT [5:0]							0000h
R812 (32Ch)	AIF2RX Channel 1 Configuration	AIF2RX_CHAN1_DAT_INV	AIF2RX_CHAN1_SPACING [5:0]						AIF2RX_CHAN1_SLOTS [2:0]		AIF2RX_CHAN1_START_SLOT [5:0]							0000h
R813 (32Dh)	AIF2RX Mono Configuration	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2RX_CHAN0_MONO_MODE	0000h
R815 (32Fh)	AIF2TX Test	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2TX_DITHER_ENA	0001h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1024 (400h)	DSP1 TX Left Volume	0	0	0	0	0	0	0	DSP1TX_VU	DSP1TXL_VOL [7:0]								00C0h
R1025 (401h)	DSP1 TX Right Volume	0	0	0	0	0	0	0	DSP1TX_VU	DSP1TXR_VOL [7:0]								00C0h
R1026 (402h)	DSP1 RX Left Volume	0	0	0	0	0	0	0	DSP1RX_VU	DSP1RXL_VOL [7:0]								00C0h
R1027 (403h)	DSP1 RX Right Volume	0	0	0	0	0	0	0	DSP1RX_VU	DSP1RXR_VOL [7:0]								00C0h
R1040 (410h)	DSP1 TX Filters	0	0	DSP1TX_NF	DSP1TXL_HPF	DSP1TXR_HPF	0	0	0	0	0	0	DSP1TX_HPF_MODE [1:0]		DSP1TX_HPF_CUT [2:0]			2000h
R1056 (420h)	DSP1 RX Filters (1)	0	0	0	0	0	0	DSP1RX_MUTE	0	DSP1RX_MONO	0	DSP1RX_MUTERATE	DSP1RX_UNMUTE_RAMP	0	0	0	0	0200h
R1057 (421h)	DSP1 RX Filters (2)	0	0	DSP1RX_3D_GAIN [4:0]					DSP1RX_3D_ENA	0	0	0	1	0	0	0	0	0010h
R1088 (440h)	DSP1 DRC (1)	DSP1DRC_SIG_DET_RMS [4:0]					DSP1DRC_SIG_DET_PK [1:0]		DSP1DRC_NG_ENA	DSP1DRC_SIG_DET_MODE	DSP1DRC_SIG_DET	DSP1DRC_KNEE2_OP_ENA	DSP1DRC_QR	DSP1DRC_ANTICLIP	DSP1RX_DRC_ENA	DSP1TXL_DRC_ENA	DSP1TXR_DRC_ENA	0098h
R1089 (441h)	DSP1 DRC (2)	0	0	0	DSP1DRC_ATK [3:0]				DSP1DRC_DCY [3:0]				DSP1DRC_MINGAIN [2:0]			DSP1DRC_MAXGAIN [1:0]		0845h
R1090 (442h)	DSP1 DRC (3)	DSP1DRC_NG_MINGAIN [3:0]				DSP1DRC_NG_EXP [1:0]		DSP1DRC_QR_THR [1:0]		DSP1DRC_QR_DCY [1:0]		DSP1DRC_HI_COMP [2:0]			DSP1DRC_LO_COMP [2:0]			0000h
R1091 (443h)	DSP1 DRC (4)	0	0	0	0	0	DSP1DRC_KNEE_IP [5:0]						DSP1DRC_KNEE_OP [4:0]					0000h
R1092 (444h)	DSP1 DRC (5)	0	0	0	0	0	0	DSP1DRC_KNEE2_IP [4:0]					DSP1DRC_KNEE2_OP [4:0]					0000h
R1152 (480h)	DSP1 RX EQ Gains (1)	DSP1RX_EQ_B1_GAIN [4:0]					DSP1RX_EQ_B2_GAIN [4:0]					DSP1RX_EQ_B3_GAIN [4:0]					DSP1RX_EQ_ENA	6318h
R1153 (481h)	DSP1 RX EQ Gains (2)	DSP1RX_EQ_B4_GAIN [4:0]					DSP1RX_EQ_B5_GAIN [4:0]					0	0	0	0	0	0	6300h
R1154 (482h)	DSP1 RX EQ Band 1 A	DSP1RX_EQ_B1_A [15:0]																0FCAh
R1155 (483h)	DSP1 RX EQ Band 1 B	DSP1RX_EQ_B1_B [15:0]																0400h
R1156 (484h)	DSP1 RX EQ Band 1 PG	DSP1RX_EQ_B1_PG [15:0]																00D8h
R1157 (485h)	DSP1 RX EQ Band 2 A	DSP1RX_EQ_B2_A [15:0]																1EB5h
R1158 (486h)	DSP1 RX EQ Band 2 B	DSP1RX_EQ_B2_B [15:0]																F145h
R1159 (487h)	DSP1 RX EQ Band 2 C	DSP1RX_EQ_B2_C [15:0]																0B75h
R1160 (488h)	DSP1 RX EQ Band 2 PG	DSP1RX_EQ_B2_PG [15:0]																01C5h
R1161 (489h)	DSP1 RX EQ Band 3 A	DSP1RX_EQ_B3_A [15:0]																1C58h
R1162 (48Ah)	DSP1 RX EQ Band 3 B	DSP1RX_EQ_B3_B [15:0]																F373h
R1163 (48Bh)	DSP1 RX EQ Band 3 C	DSP1RX_EQ_B3_C [15:0]																0A54h
R1164 (48Ch)	DSP1 RX EQ Band 3 PG	DSP1RX_EQ_B3_PG [15:0]																0558h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1165 (48Dh)	DSP1 RX EQ Band 4 A	DSP1RX_EQ_B4_A [15:0]																168Eh
R1166 (48Eh)	DSP1 RX EQ Band 4 B	DSP1RX_EQ_B4_B [15:0]																F829h
R1167 (48Fh)	DSP1 RX EQ Band 4 C	DSP1RX_EQ_B4_C [15:0]																07ADh
R1168 (490h)	DSP1 RX EQ Band 4 PG	DSP1RX_EQ_B4_PG [15:0]																1103h
R1169 (491h)	DSP1 RX EQ Band 5 A	DSP1RX_EQ_B5_A [15:0]																0564h
R1170 (492h)	DSP1 RX EQ Band 5 B	DSP1RX_EQ_B5_B [15:0]																0559h
R1171 (493h)	DSP1 RX EQ Band 5 PG	DSP1RX_EQ_B5_PG [15:0]																4000h
R1280 (500h)	DSP2 TX Left Volume	0	0	0	0	0	0	0	DSP2TX_VU	DSP2TXL_VOL [7:0]								00C0h
R1281 (501h)	DSP2 TX Right Volume	0	0	0	0	0	0	0	DSP2TX_VU	DSP2TXR_VOL [7:0]								00C0h
R1282 (502h)	DSP2 RX Left Volume	0	0	0	0	0	0	0	DSP2RX_VU	DSP2RXL_VOL [7:0]								00C0h
R1283 (503h)	DSP2 RX Right Volume	0	0	0	0	0	0	0	DSP2RX_VU	DSP2RXR_VOL [7:0]								00C0h
R1296 (510h)	DSP2 TX Filters	0	0	DSP2TX_NF	DSP2TXL_HPF	DSP2TXR_HPF	0	0	0	0	0	0	DSP2TX_HPF_MODE [1:0]		DSP2TX_HPF_CUT [2:0]			2000h
R1312 (520h)	DSP2 RX Filters (1)	0	0	0	0	0	0	DSP2RX_MUTE	0	DSP2RX_MONO	0	DSP2RX_MUTERATE	DSP2RX_UNMUTE_RAMP	0	0	0	0	0200h
R1313 (521h)	DSP2 RX Filters (2)	0	0	DSP2RX_3D_GAIN [4:0]					DSP2RX_3D_ENA	0	0	0	1	0	0	0	0	0010h
R1344 (540h)	DSP2 DRC (1)	DSP2DRC_SIG_DET_RMS [4:0]					DSP2DRC_SIG_DET_PK [1:0]		DSP2DRC_NG_ENA	DSP2DRC_SIG_DET_MODE	DSP2DRC_SIG_DET	DSP2DRC_KNEE2_OP_ENA	DSP2DRC_QR	DSP2DRC_ANTICLIP	DSP2RX_DRC_ENA	DSP2TXL_DRC_ENA	DSP2TXR_DRC_ENA	0098h
R1345 (541h)	DSP2 DRC (2)	0	0	0	DSP2DRC_ATK [3:0]				DSP2DRC_DCY [3:0]				DSP2DRC_MINGAIN [2:0]			DSP2DRC_MAXGAIN [1:0]		0845h
R1346 (542h)	DSP2 DRC (3)	DSP2DRC_NG_MINGAIN [3:0]				DSP2DRC_NG_EXP [1:0]		DSP2DRC_QR_THR [1:0]		DSP2DRC_QR_DCY [1:0]		DSP2DRC_HI_COMP [2:0]			DSP2DRC_LO_COMP [2:0]			0000h
R1347 (543h)	DSP2 DRC (4)	0	0	0	0	0	DSP2DRC_KNEE_IP [5:0]						DSP2DRC_KNEE_OP [4:0]					0000h
R1348 (544h)	DSP2 DRC (5)	0	0	0	0	0	0	DSP2DRC_KNEE2_IP [4:0]					DSP2DRC_KNEE2_OP [4:0]					0000h
R1408 (580h)	DSP2 RX EQ Gains (1)	DSP2RX_EQ_B1_GAIN [4:0]					DSP2RX_EQ_B2_GAIN [4:0]					DSP2RX_EQ_B3_GAIN [4:0]					DSP2RX_EQ_ENA	6318h
R1409 (581h)	DSP2 RX EQ Gains (2)	DSP2RX_EQ_B4_GAIN [4:0]					DSP2RX_EQ_B5_GAIN [4:0]					0	0	0	0	0	0	6300h
R1410 (582h)	DSP2 RX EQ Band 1 A	DSP2RX_EQ_B1_A [15:0]																0FCAh
R1411 (583h)	DSP2 RX EQ Band 1 B	DSP2RX_EQ_B1_B [15:0]																0400h
R1412 (584h)	DSP2 RX EQ Band 1 PG	DSP2RX_EQ_B1_PG [15:0]																00D8h
R1413 (585h)	DSP2 RX EQ Band 2 A	DSP2RX_EQ_B2_A [15:0]																1EB5h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1414 (586h)	DSP2 RX EQ Band 2 B	DSP2RX_EQ_B2_B [15:0]																F145h
R1415 (587h)	DSP2 RX EQ Band 2 C	DSP2RX_EQ_B2_C [15:0]																0B75h
R1416 (588h)	DSP2 RX EQ Band 2 PG	DSP2RX_EQ_B2_PG [15:0]																01C5h
R1417 (589h)	DSP2 RX EQ Band 3 A	DSP2RX_EQ_B3_A [15:0]																1C58h
R1418 (58Ah)	DSP2 RX EQ Band 3 B	DSP2RX_EQ_B3_B [15:0]																F373h
R1419 (58Bh)	DSP2 RX EQ Band 3 C	DSP2RX_EQ_B3_C [15:0]																0A54h
R1420 (58Ch)	DSP2 RX EQ Band 3 PG	DSP2RX_EQ_B3_PG [15:0]																0558h
R1421 (58Dh)	DSP2 RX EQ Band 4 A	DSP2RX_EQ_B4_A [15:0]																168Eh
R1422 (58Eh)	DSP2 RX EQ Band 4 B	DSP2RX_EQ_B4_B [15:0]																F829h
R1423 (58Fh)	DSP2 RX EQ Band 4 C	DSP2RX_EQ_B4_C [15:0]																07ADh
R1424 (590h)	DSP2 RX EQ Band 4 PG	DSP2RX_EQ_B4_PG [15:0]																1103h
R1425 (591h)	DSP2 RX EQ Band 5 A	DSP2RX_EQ_B5_A [15:0]																0564h
R1426 (592h)	DSP2 RX EQ Band 5 B	DSP2RX_EQ_B5_B [15:0]																0559h
R1427 (593h)	DSP2 RX EQ Band 5 PG	DSP2RX_EQ_B5_PG [15:0]																4000h
R1536 (600h)	DAC1 Mixer Volumes	0	0	0	0	0	0	ADCR_DAC1_VOL [4:0]					ADCL_DAC1_VOL [4:0]					0000h
R1537 (601h)	DAC1 Left Mixer Routing	0	0	0	0	0	0	0	0	0	0	ADCR_TO_DAC1L	ADCL_TO_DAC1L	0	0	DSP2RXL_TO_DAC1L	DSP1RXL_TO_DAC1L	0000h
R1538 (602h)	DAC1 Right Mixer Routing	0	0	0	0	0	0	0	0	0	0	ADCR_TO_DAC1R	ADCL_TO_DAC1R	0	0	DSP2RXR_TO_DAC1R	DSP1RXR_TO_DAC1R	0000h
R1539 (603h)	DAC2 Mixer Volumes	0	0	0	0	0	0	ADCR_DAC2_VOL [4:0]					ADCL_DAC2_VOL [4:0]					0000h
R1540 (604h)	DAC2 Left Mixer Routing	0	0	0	0	0	0	0	0	0	0	ADCR_TO_DAC2L	ADCL_TO_DAC2L	0	0	DSP2RXL_TO_DAC2L	DSP1RXL_TO_DAC2L	0000h
R1541 (605h)	DAC2 Right Mixer Routing	0	0	0	0	0	0	0	0	0	0	ADCR_TO_DAC2R	ADCL_TO_DAC2R	0	0	DSP2RXR_TO_DAC2R	DSP1RXR_TO_DAC2R	0000h
R1542 (606h)	DSP1 TX Left Mixer Routing	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC1L_TO_DSP1TXL	DACL_TO_DSP1TXL	0000h
R1543 (607h)	DSP1 TX Right Mixer Routing	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC1R_TO_DSP1TXR	DACR_TO_DSP1TXR	0000h
R1544 (608h)	DSP2 TX Left Mixer Routing	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC2L_TO_DSP2TXL	DACL_TO_DSP2TXL	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1545 (609h)	DSP2 TX Right Mixer Routing	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC2R_TO_DSP2TXR	DACR_TO_DSP2TXR	0000h
R1546 (60Ah)	DSP TX Mixer Select	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAC_TO_DSPTX_SRC	0000h
R1552 (610h)	DAC Softmute	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAC_SOFTMUTEMODE	DAC_MUTERATE	0000h
R1568 (620h)	Oversampling	0	0	0	0	0	0	0	0	0	0	0	0	SPK_OSR128	DMIC_OSR64	ADC_OSR128	DAC_OSR128	000Dh
R1569 (621h)	Sidetone	0	0	0	ST_LPF	0	0	ST_HPF_CUT [2:0]			ST_HPF	0	0	0	0	STR_SEL	STL_SEL	1000h
R1792 (700h)	GPIO 1	GP1_DIR	GP1_PU	GP1_PD	0	0	GP1_POL	GP1_OP_CFG	GP1_DB	0	GP1_LVL	0	0	GP1_FN [3:0]				A101h
R1793 (701h)	GPIO 2	GP2_DIR	GP2_PU	GP2_PD	0	0	GP2_POL	GP2_OP_CFG	GP2_DB	0	GP2_LVL	0	0	GP2_FN [3:0]				A101h
R1794 (702h)	GPIO 3	GP3_DIR	GP3_PU	GP3_PD	0	0	GP3_POL	GP3_OP_CFG	GP3_DB	0	GP3_LVL	0	0	GP3_FN [3:0]				A101h
R1795 (703h)	GPIO 4	GP4_DIR	GP4_PU	GP4_PD	0	0	GP4_POL	GP4_OP_CFG	GP4_DB	0	GP4_LVL	0	0	GP4_FN [3:0]				A101h
R1796 (704h)	GPIO 5	GP5_DIR	GP5_PU	GP5_PD	0	0	GP5_POL	GP5_OP_CFG	GP5_DB	0	GP5_LVL	0	0	GP5_FN [3:0]				A101h
R1824 (720h)	Pull Control (1)	0	0	0	DMICDAT2_PD	0	DMICDAT1_PD	MCLK2_PU	MCLK2_PD	MCLK1_PU	MCLK1_PD	DACDAT1_PU	DACDAT1_PD	DACLRCLK1_PU	DACLRCLK1_PD	BCLK1_PU	BCLK1_PD	0000h
R1825 (721h)	Pull Control (2)	0	0	0	0	0	0	0	LDO1ENA_PD	0	ADDR_PD	DACDAT2_PU	DACDAT2_PD	DACLRCLK2_PU	DACLRCLK2_PD	BCLK2_PU	BCLK2_PD	0140h
R1840 (730h)	Interrupt Status 1	0	0	0	0	0	0	0	0	0	0	0	GP5_EINT	GP4_EINT	GP3_EINT	GP2_EINT	GP1_EINT	0000h
R1841 (731h)	Interrupt Status 2	0	0	0	DCS_DONE_23_EINT	DCS_DONE_01_EINT	WSEQ_DONE_EINT	FIFOS_ERR_EINT	0	DSP2DRC_SIG_DET_EINT	DSP1DRC_SIG_DET_EINT	0	0	FLL_SW_CLK_DONE_EINT	FLL_LOCK_EINT	HP_DONE_EINT	MICD_EINT	0000h
R1842 (732h)	Interrupt Raw Status 2	0	0	0	DCS_DONE_23_STS	DCS_DONE_01_STS	WSEQ_DONE_STS	FIFOS_ERR_STS	0	DSP2DRC_SIG_DET_STS	DSP1DRC_SIG_DET_STS	0	0	0	FLL_LOCK_STS	0	0	0000h
R1848 (738h)	Interrupt Status 1 Mask	0	0	0	0	0	0	0	0	0	0	0	IM_GP5_EINT	IM_GP4_EINT	IM_GP3_EINT	IM_GP2_EINT	IM_GP1_EINT	001Fh
R1849 (739h)	Interrupt Status 2 Mask	0	0	0	IM_DCS_DONE_23_EINT	IM_DCS_DONE_01_EINT	IM_WSEQ_DONE_EINT	IM_FIFOS_ERR_EINT	0	IM_DSP2DRC_SIG_DET_EINT	IM_DSP1DRC_SIG_DET_EINT	0	0	IM_FLL_SW_CLK_DONE_EINT	IM_FLL_LOCK_EINT	IM_HP_DONE_EINT	IM_MICD_EINT	1ECFh
R1856 (740h)	Interrupt Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IM_IRQ	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R2048 (800h)	Left PDM Speaker	0	0	0	0	0	0	0	0	0	0	0	SPKL_ENA	SPKL_MUTE	SPKL_MUTE_ZC	SPKL_SRC [1:0]		0000h
R2049 (801h)	Right PDM Speaker	0	0	0	0	0	0	0	0	0	0	0	SPKR_ENA	SPKR_MUTE	SPKR_MUTE_ZC	SPKR_SRC [1:0]		0001h
R2050 (802h)	PDM Speaker Mute Sequence	0	0	0	0	0	0	0	SPK_MUTE_ENDIAN	SPK_MUTE_SEQ1 [7:0]								0069h
R2051 (803h)	PDM Speaker Volume	SPK_FMT	0	0	0	0	0	0	0	SPKR_VOL [3:0]				SPKL_VOL [3:0]				0066h
R12288 (3000h)	Write Sequencer 0	0	0	WSEQ_ADDR0 [13:0]														0001h
R12289 (3001h)	Write Sequencer 1	0	0	0	0	0	0	0	0	WSEQ_DATA0 [7:0]								0001h
R12290 (3002h)	Write Sequencer 2	0	0	0	0	0	WSEQ_DATA_WIDTH0 [2:0]			0	0	0	0	WSEQ_DATA_START0 [3:0]				0000h
R12291 (3003h)	Write Sequencer 3	0	0	0	0	0	0	0	WSEQ_EOS0	0	0	0	0	WSEQ_DELAY0 [3:0]				0006h
R12292 (3004h)	Write Sequencer 4	0	0	WSEQ_ADDR1 [13:0]														0040h
R12293 (3005h)	Write Sequencer 5	0	0	0	0	0	0	0	0	WSEQ_DATA1 [7:0]								0001h
R12294 (3006h)	Write Sequencer 6	0	0	0	0	0	WSEQ_DATA_WIDTH1 [2:0]			0	0	0	0	WSEQ_DATA_START1 [3:0]				000Fh
R12295 (3007h)	Write Sequencer 7	0	0	0	0	0	0	0	WSEQ_EOS1	0	0	0	0	WSEQ_DELAY1 [3:0]				0006h
				(similar for WSEQ index 2 .. 126)														
R12796 (31FCh)	Write Sequencer 508	0	0	WSEQ_ADDR127 [13:0]														0000h
R12797 (31FDh)	Write Sequencer 509	0	0	0	0	0	0	0	0	WSEQ_DATA127 [7:0]								0000h
R12798 (31FEh)	Write Sequencer 510	0	0	0	0	0	WSEQ_DATA_WIDTH127 [2:0]			0	0	0	0	WSEQ_DATA_START127 [3:0]				0000h
R12799 (31FFh)	Write Sequencer 511	0	0	0	0	0	0	0	WSEQ_EOS127	0	0	0	0	WSEQ_DELAY127 [3:0]				0000h

REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) Software Reset	15:0	SW_RESET [15:0]	0000_0000_0000_0000	Writing to this register resets all registers to their default state. (Note - Control Write Sequencer registers are not affected by Software Reset.) Reading from this register will indicate Chip ID 8915h.	

Register 00h Software Reset

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1 (01h) Power Management (1)	9	MICB2_ENA	0	Microphone Bias 2 Enable 0 = Disabled 1 = Enabled	
	8	MICB1_ENA	0	Microphone Bias 1 Enable 0 = Disabled 1 = Enabled	
	7	HPOUT2L_ENA	0	Enables HPOUT2L input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT2L Enable sequence.	
	6	HPOUT2R_ENA	0	Enables HPOUT2R input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT2R Enable sequence.	
	5	HPOUT1L_ENA	0	Enables HPOUT1L input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT1L Enable sequence.	
	4	HPOUT1R_ENA	0	Enables HPOUT1R input stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set as the first step of the HPOUT1R Enable sequence.	
	0	BG_ENA	0	Internal Bandgap Reference Enable (required for normal operation) 0 = Disabled 1 = Enabled Note that the Microphone / Accessory detect function can be supported when BG_ENA = 0.	

Register 01h Power Management (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2 (02h) Power Management (2)	11	OPCLK_ENA	0	GPIO Clock Output (OPCLK) Enable 0 = Disabled 1 = Enabled	
	5	INL_ENA	0	INL Input PGA Enable 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4	INR_ENA	0	INR Input PGA Enable 0 = Disabled 1 = Enabled	
	1	LDO2_ENA	0	LDO2 Enable 0 = Disabled 1 = Enabled	

Register 02h Power Management (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R3 (03h) Power Management (3)	11	DSP2RXL_ENA	0	Enable DSP2 (Left) input path 0 = Disabled 1 = Enabled	
	10	DSP2RXR_ENA	0	Enable DSP2 (Right) input path 0 = Disabled 1 = Enabled	
	9	DSP1RXL_ENA	0	Enable DSP1 (Left) input path 0 = Disabled 1 = Enabled	
	8	DSP1RXR_ENA	0	Enable DSP1 (Right) input path 0 = Disabled 1 = Enabled	
	5	DMIC2L_ENA	0	Digital microphone DMICDAT2 Left channel enable 0 = Disabled 1 = Enabled	
	4	DMIC2R_ENA	0	Digital microphone DMICDAT2 Right channel enable 0 = Disabled 1 = Enabled	
	3	DMIC1L_ENA	0	Digital microphone DMICDAT1 Left channel enable 0 = Disabled 1 = Enabled	
	2	DMIC1R_ENA	0	Digital microphone DMICDAT1 Right channel enable 0 = Disabled 1 = Enabled	
	1	ADCL_ENA	0	Left ADC Enable 0 = ADC disabled 1 = ADC enabled	
	0	ADCR_ENA	0	Right ADC Enable 0 = ADC disabled 1 = ADC enabled	

Register 03h Power Management (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R4 (04h) Power Management (4)	9	AIF2RX_CHAN1_ENA	0	Enable AIF2 input channel 1 0 = Disabled 1 = Enabled	
	8	AIF2RX_CHAN0_ENA	0	Enable AIF2 input channel 0 0 = Disabled 1 = Enabled	
	5	AIF1RX_CHAN5	0	Enable AIF1 input channel 5	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
		_ENA		0 = Disabled 1 = Enabled	
	4	AIF1RX_CHAN4 _ENA	0	Enable AIF1 input channel 4 0 = Disabled 1 = Enabled	
	3	AIF1RX_CHAN3 _ENA	0	Enable AIF1 input channel 3 0 = Disabled 1 = Enabled	
	2	AIF1RX_CHAN2 _ENA	0	Enable AIF1 input channel 2 0 = Disabled 1 = Enabled	
	1	AIF1RX_CHAN1 _ENA	0	Enable AIF1 input channel 1 0 = Disabled 1 = Enabled	
	0	AIF1RX_CHAN0 _ENA	0	Enable AIF1 input channel 0 0 = Disabled 1 = Enabled	

Register 04h Power Management (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R5 (05h) Power Management (5)	11	DSP2TXL_ENA	0	Enable DSP2 (Left) output path 0 = Disabled 1 = Enabled	
	10	DSP2TXR_ENA	0	Enable DSP2 (Right) output path 0 = Disabled 1 = Enabled	
	9	DSP1TXL_ENA	0	Enable DSP1 (Left) output path 0 = Disabled 1 = Enabled	
	8	DSP1TXR_ENA	0	Enable DSP1 (Right) output path 0 = Disabled 1 = Enabled	
	3	DAC2L_ENA	0	Left DAC2 Enable 0 = Disabled 1 = Enabled	
	2	DAC2R_ENA	0	Right DAC2 Enable 0 = Disabled 1 = Enabled	
	1	DAC1L_ENA	0	Left DAC1 Enable 0 = Disabled 1 = Enabled	
	0	DAC1R_ENA	0	Right DAC1 Enable 0 = Disabled 1 = Enabled	

Register 05h Power Management (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R6 (06h) Power	9	AIF2TX_CHAN1 _ENA	0	Enable AIF2 output channel 1 0 = Disabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
Management (6)				1 = Enabled	
	8	AIF2TX_CHAN1_ENA	0	Enable AIF2 output channel 0 0 = Disabled 1 = Enabled	
	5	AIF1TX_CHAN5_ENA	0	Enable AIF1 output channel 5 0 = Disabled 1 = Enabled	
	4	AIF1TX_CHAN4_ENA	0	Enable AIF1 output channel 4 0 = Disabled 1 = Enabled	
	3	AIF1TX_CHAN3_ENA	0	Enable AIF1 output channel 3 0 = Disabled 1 = Enabled	
	2	AIF1TX_CHAN2_ENA	0	Enable AIF1 output channel 2 0 = Disabled 1 = Enabled	
	1	AIF1TX_CHAN1_ENA	0	Enable AIF1 output channel 1 0 = Disabled 1 = Enabled	
	0	AIF1TX_CHAN0_ENA	0	Enable AIF1 output channel 0 0 = Disabled 1 = Enabled	

Register 06h Power Management (6)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R7 (07h) Power Management (7)	9	DMIC2_FN	0	DMICCLK2 and DMICDAT2 function 0 = Disabled 1 = Digital microphone enabled on DMICLK2 / DMICDAT2. Note that IN2RN and IN2RP cannot support analogue input when DMIC2_FN is enabled.	
	8	DMIC1_FN	0	DMICCLK1 and DMICDAT1 function 0 = Disabled 1 = Digital microphone interface on DMICLK1 / DMICDAT1. Note that IN2LN and IN2LP cannot support analogue input when DMIC1_FN is enabled.	
	7	ADC_DMIC_DSP2R_ENA	0	Input path 2R enable 0 = Disabled 1 = Enabled	
	6	ADC_DMIC_DSP2L_ENA	0	Input path 2L enable 0 = Disabled 1 = Enabled	
	5:4	ADC_DMIC_SRC2 [1:0]	01	Input path 2L and 2R select 00 = ADC 01 = DMICDAT1 10 = DMICDAT2 11 = Reserved	
	3	ADC_DMIC_DSP1R_ENA	0	Input path 1R enable 0 = Disabled 1 = Enabled	
	2	ADC_DMIC_DSP1L_ENA	0	Input path 1L enable 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1:0	ADC_DMIC_SRC1 [1:0]	00	Input path 1L and 1R select 00 = ADC 01 = DMICDAT1 10 = DMICDAT2 11 = Reserved	

Register 07h Power Management (7)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R8 (08h) Power Management (8)	7:6	AIF2TX_SRC [1:0]	00	Selects source for AIF2 output 00 = DSP2 output 01 = DSP1 output 10 = AIF1 input (channels 4 and 5) 11 = Reserved	
	4	DSP2RX_SRC	0	Selects source for DSP2 input 0 = AIF2 input 1 = AIF1 input (channels 2 and 3)	
	0	DSP1RX_SRC	0	Selects source for DSP1 input 0 = AIF1 input (channels 0 and 1) 1 = AIF2 input	

Register 08h Power Management (8)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16 (10h) Left Line Input Volume	7	IN_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause INL and INR input PGA volumes to be updated simultaneously	
	5	INL_ZC	0	INL PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only	
	4:0	INL_VOL [4:0]	0_0000	INL Volume 0dB to +31dB in 1dB steps 00h = 0dB 01h = 1dB … (1dB steps) 1Fh = 31dB	

Register 10h Left Line Input Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R17 (11h) Right Line Input Volume	7	IN_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause INL and INR input PGA volumes to be updated simultaneously	
	5	INR_ZC	0	INR PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only	
	4:0	INR_VOL [4:0]	0_0000	INR Volume 0dB to +31dB in 1dB steps 00h = 0dB 01h = 1dB … (1dB steps) 1Fh = 31dB	

Register 11h Right Line Input Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R18 (12h) Line Input Control	3:2	INL_MODE [1:0]	00	Left Input PGA Mode 00 = Differential (IN1LP - IN1LN) 01 = Single-ended inverting (IN1LN) 10 = Single-ended non-inverting (IN1LP) 11 = Differential (IN2LP - IN2LN) Note that IN2LN and IN2LP cannot support analogue input when DMIC1_FN is enabled.	
	1:0	INR_MODE [1:0]	00	Right Input PGA Mode 00 = Differential (IN1RP - IN1RN) 01 = Single-ended inverting (IN1RN) 10 = Single-ended non-inverting (IN1RP) 11 = Differential (IN2RP - IN2RN) Note that IN2RN and IN2RP cannot support analogue input when DMIC2_FN is enabled.	

Register 12h Line Input Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R21 (15h) DAC1 HPOUT1 Volume	7:4	DAC2R_HPOUT 2R_VOL [3:0]	1000	HPOUT2R Digital Volume Control -12dB to 0dB in 1.5dB steps 0000 = -12.0dB 0001 = -10.5dB … (1.5dB steps) 1000 = 0dB 1001 to 1111 = Reserved	
	3:0	DAC2L_HPOUT 2L_VOL [3:0]	1000	HPOUT2L Digital Volume Control -12dB to 0dB in 1.5dB steps 0000 = -12.0dB 0001 = -10.5dB … (1.5dB steps) 1000 = 0dB 1001 to 1111 = Reserved	

Register 15h DAC1 HPOUT1 Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R22 (16h) DAC2 HPOUT2 Volume	7:4	DAC2R_HPOUT2R_VOL [3:0]	1000	HPOUT2R Digital Volume Control -12dB to 0dB in 1.5dB steps 0000 = -12.0dB 0001 = -10.5dB … (1.5dB steps) 1000 = 0dB 1001 to 1111 = Reserved	
	3:0	DAC2L_HPOUT2L_VOL [3:0]	1000	HPOUT2L Digital Volume Control -12dB to 0dB in 1.5dB steps 0000 = -12.0dB 0001 = -10.5dB … (1.5dB steps) 1000 = 0dB 1001 to 1111 = Reserved	

Register 16h DAC2 HPOUT2 Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R23 (17h) Output Volume Control 1	0	OUT_VOL_SHARED	0	When this bit is set to 1, the HPOUT volume and DAC volume are both controlled by the DAC volume registers and the HPOUT volume control fields are disabled. Note that the DAC volume register coding is different when OUT_VOL_SHARED is set.	

Register 17h Output Volume Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R24 (18h) DAC1 Left Volume	9	DAC1L_MUTE	1	DAC1L Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute	
	8	DAC1_VU	0	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously	
	7:0	DAC1L_VOL [7:0]	1100_0000	DAC1L Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) E0h = 12.000dB FFh = 12.000dB	

Register 18h DAC1 Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R25 (19h) DAC1 Right Volume	9	DAC1R_MUTE	1	DAC1R Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute	
	8	DAC1_VU	0	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously	
	7:0	DAC1R_VOL [7:0]	1100_0000	DAC1R Digital Volume 00h = MUTE	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				01h = -71.625dB … (0.375dB steps) E0h = 12.000dB FFh = 12.000dB	

Register 19h DAC1 Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R26 (1Ah) DAC2 Left Volume	9	DAC2L_MUTE	1	DAC2L Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute	
	8	DAC2_VU	0	DAC2L and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2L and DAC2R volume to be updated simultaneously	
	7:0	DAC2L_VOL [7:0]	1100_0000	DAC2L Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) E0h = 12.000dB FFh = 12.000dB	

Register 1Ah DAC2 Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R27 (1Bh) DAC2 Right Volume	9	DAC2R_MUTE	1	DAC2R Soft Mute Control 0 = DAC Un-mute 1 = DAC Mute	
	8	DAC2_VU	0	DAC2L and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2L and DAC2R volume to be updated simultaneously	
	7:0	DAC2R_VOL [7:0]	1100_0000	DAC2R Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) E0h = 12.000dB FFh = 12.000dB	

Register 1Bh DAC2 Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R28 (1Ch) Output1 Left Volume	8	DAC1_VU	N/A	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously	
	7	HPOUT1L_ZC	1	HPOUT1L PGA Zero Cross Enable 0 = Disabled 1 = Enabled	
	3:0	HPOUT1L_VOL [3:0]	0000	HPOUT1L PGA Volume Control -9dB to 0dB in 0.75dB steps 0000 = -9.00dB 0001 = -8.25dB … (0.75dB steps)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1100 = 0dB 1101 to 1111 = Reserved	

Register 1Ch Output1 Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R29 (1Dh) Output1 Right Volume	8	DAC1_VU	N/A	DAC1L and DAC1R Volume Update Writing a 1 to this bit will cause the DAC1L and DAC1R volume to be updated simultaneously	
	7	HPOUT1R_ZC	1	HPOUT1R PGA Zero Cross Enable 0 = Disabled 1 = Enabled	
	3:0	HPOUT1R_VOL [3:0]	0000	HPOUT1R PGA Volume Control -9dB to 0dB in 0.75dB steps 0000 = -9.00dB 0001 = -8.25dB … (0.75dB steps) 1100 = 0dB 1101 to 1111 = Reserved	

Register 1Dh Output1 Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30 (1Eh) Output2 Left Volume	8	DAC2_VU	N/A	DAC2L and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2L and DAC2R volume to be updated simultaneously	
	7	HPOUT2L_ZC	1	HPOUT2L PGA Zero Cross Enable 0 = Disabled 1 = Enabled	
	3:0	HPOUT2L_VOL [3:0]	0000	HPOUT2L PGA Volume Control -9dB to 0dB in 0.75dB steps 0000 = -9.00dB 0001 = -8.25dB … (0.75dB steps) 1100 = 0dB 1101 to 1111 = Reserved	

Register 1Eh Output2 Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R31 (1Fh) Output2 Right Volume	8	DAC2_VU	N/A	DAC2L and DAC2R Volume Update Writing a 1 to this bit will cause the DAC2L and DAC2R volume to be updated simultaneously	
	7	HPOUT2R_ZC	1	HPOUT2R PGA Zero Cross Enable 0 = Disabled 1 = Enabled	
	3:0	HPOUT2R_VOL [3:0]	0000	HPOUT2R PGA Volume Control -9dB to 0dB in 0.75dB steps 0000 = -9.00dB 0001 = -8.25dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				… (0.75dB steps) 1100 = 0dB 1101 to 1111 = Reserved	

Register 1Fh Output2 Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R32 (20h) MICBIAS (1)	5	MICB1_RATE	1	Microphone Bias 1 Rate 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down	
	4	MICB1_MODE	1	Microphone Bias 1 Mode 0 = Regulator mode 1 = Bypass mode	
	3:1	MICB1_LVL [2:0]	100	Microphone Bias 1 Voltage Control (when MICB1_MODE = 0) 000 = 1.5V 001 = 1.8V 010 = 1.9V 011 = 2.0V 100 = 2.2V 101 = 2.4V 110 = 2.5V 111 = 2.6V	
	0	MICB1_DISCH	1	Microphone Bias 1 Discharge 0 = MICBIAS1 floating when disabled 1 = MICBIAS1 discharged when disabled	

Register 20h MICBIAS (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R33 (21h) MICBIAS (2)	5	MICB2_RATE	1	Microphone Bias 2 Rate 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down	
	4	MICB2_MODE	1	Microphone Bias 2 Mode 0 = Regulator mode 1 = Bypass mode	
	3:1	MICB2_LVL [2:0]	100	Microphone Bias 2 Voltage Control (when MICB2_MODE = 0) 000 = 1.5V 001 = 1.8V 010 = 1.9V 011 = 2.0V 100 = 2.2V 101 = 2.4V 110 = 2.5V 111 = 2.6V	
	0	MICB2_DISCH	1	Microphone Bias 2 Discharge 0 = MICBIAS2 floating when disabled 1 = MICBIAS2 discharged when disabled	

Register 21h MICBIAS (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R40 (28h) LDO 1	5	LDO1_MODE	0	LDO1 Mode (read only) 0 = Regulator mode (DCVDD is controlled by LDO1_VSEL) 1 = Bypass mode (DCVDD is connected to DBVDD)	
	2:1	LDO1_VSEL [1:0]	01	LDO1 Output Voltage Select 0.9V to 1.2V in 100mV steps 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V	
	0	LDO1_DISCH	1	LDO1 Discharge Select 0 = LDO1 floating when disabled 1 = LDO1 discharged when disabled	

Register 28h LDO 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R41 (29h) LDO 2	5	LDO2_MODE	0	LDO2 Mode (read only) 0 = Regulator mode (MICVDD is controlled by LDO2_VSEL) 1 = Bypass mode (MICVDD is connected to AVDD1)	
	4:1	LDO2_VSEL [3:0]	1001	LDO2 Output Voltage Select 1.7V to in 100mV steps 0000 = 1.7V 0001 = 1.8V 0010 = 1.9V 0011 = 2.0V 0100 = 2.1V 0101 = 2.2V 0110 = 2.3V 0111 = 2.4V 1000 = 2.5V 1001 = 2.6V 1010 = 2.7V 1011 = 2.8V 1100 to 1111 = Reserved	
	0	LDO2_DISCH	1	LDO2 Discharge Select 0 = LDO2 floating when disabled 1 = LDO2 discharged when disabled	

Register 29h LDO 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R48 (30h) Accessory Detect Mode 1	1:0	JD_MODE [1:0]	00	Accessory Detect Mode Select 00 = MICDET measurement 01 = HPDETL measurement 10 = HPDETR measurement 11 = Reserved Note that the MICDET function is provided on the MICDET1 or MICDET2 pins, depending on the MICD_SRC register bit.	

Register 30h Accessory Detect Mode 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R49 (31h) Accessory Detect Mode 2	2	HPOUT1FB_SRC	0	HPOUT1 Ground feedback pin select 0 = HPOUT1FB1/MICDET2 1 = HPOUT1FB2/MICDET1	
	1	MICD_SRC	0	Accessory Detect (MICDET) pin select 0 = HPOUT1FB2/MICDET1 1 = HPOUT1FB1/MICDET2	
	0	MICD_BIAS_SRC	0	Accessory Detect (MICDET) reference select 0 = MICBIAS1 1 = MICBIAS2	

Register 31h Accessory Detect Mode 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R52 (34h) Headphone Detect 1	7:5	HP_HOLDTIME [2:0]	001	Headphone Detect Hold Time (Selects the hold time between ramp up and ramp down of the headphone detect current source. The clock cycle rate is set by HP_CLK_DIV) 000 = 1 clock cycle 001 = 4 clock cycles 010 = 16 clock cycles 011 = 64 clock cycles 100 = 256 clock cycles 101 = 512 clock cycles 110 = 768 clock cycles 111 =1024 clock cycles	
	4:3	HP_CLK_DIV [1:0]	00	Headphone Detect Clock Rate (Selects the clocking rate of the headphone detect adjustable current source.) 00 = 32kHz 01 = 16kHz 10 = 8kHz 11 = 4kHz	
	1	HP_STEP_SIZE	0	Headphone Detect Ramp Rate 0 = Normal rate 1 = Fast rate	
	0	HP_POLL	0	Headphone Detect Enable Write 1 to start HP Detect function	

Register 34h Headphone Detect 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R53 (35h) Headphone Detect 2	7	HP_DONE	0	Headphone Detect Status 0 = HP Detect not complete 1 = HP Detect done	
	6:0	HP_LVL [6:0]	000_0000	Headphone Detect Level LSB = 1 ohm Valid from 8..126 ohm 08h = 8 ohm or less 09h = 9 ohm 0Ah = 10 ohm ….	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				7Dh = 125 ohm 7Eh = 126 ohm or more	

Register 35h Headphone Detect 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R56 (38h) Mic Detect 1	15:12	MICD_BIAS_STARTTIME [3:0]	0111	Mic Detect Bias Startup Delay (If MICBIAS is not enabled already, this field selects the delay time allowed for MICBIAS to startup prior to performing the MICDET function.) 0000 = 0ms (continuous) 0001 = 0.25ms 0010 = 0.5ms 0011 = 1ms 0100 = 2ms 0101 = 4ms 0110 = 8ms 0111 = 16ms 1000 = 32ms 1001 = 64ms 1010 = 128ms 1011 = 256ms 1100 to 1111 = 512ms	
	11:8	MICD_RATE [3:0]	0110	Mic Detect Rate (Selects the delay between successive Mic Detect measurements.) 0000 = 0ms (continuous) 0001 = 0.25ms 0010 = 0.5ms 0011 = 1ms 0100 = 2ms 0101 = 4ms 0110 = 8ms 0111 = 16ms 1000 = 32ms 1001 = 64ms 1010 = 128ms 1011 = 256ms 1100 to 1111 = 512ms	
	1	MICD_DBTIME	0	Mic Detect De-bounce 0 = 2 measurements 1 = 4 measurements	
	0	MICD_ENA	0	Mic Detect Enable 0 = Disabled 1 = Enabled	

Register 38h Mic Detect 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R57 (39h) Mic Detect 2	7:0	MICD_LVL_SEL [7:0]	1011_1111	Mic Detect Level Select (enables Mic Detection in specific impedance ranges) [7] = Enable >475 ohm detection	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				[6] = Not used - must be set to 0 [5] = Enable 326 ohm detection [4] = Enable 152 ohm detection [3] = Enable 77 ohm detection [2] = Enable 47.6 ohm detection [1] = Enable 29.4 ohm detection [0] = Enable 14 ohm detection Note that the impedance values quoted assume that a microphone (475ohm-30kohm) is also present on the MICDET pin.	

Register 39h Mic Detect 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R58 (3Ah) Mic Detect 3	10:2	MICD_LVL [8:0]	0_0000_0000	Mic Detect Level (indicates the measured impedance) [8] = >475 ohm, <30k ohm [7] = Not used [6] = 326 ohm [5] = 152 ohm [4] = 77 ohm [3] = 47.6 ohm [2] = 29.4 ohm [1] = 14 ohm [0] = <2 ohm Note that the impedance values quoted assume that a microphone (475ohm-30kohm) is also present on the MICDET pin.	
	1	MICD_VALID	0	Mic Detect Data Valid 0 = Not Valid 1 = Valid	
	0	MICD_STS	0	Mic Detect Status 0 = No Mic Accessory present (impedance is >30k ohm) 1 = Mic Accessory is present (impedance is <30k ohm)	

Register 3Ah Mic Detect 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R64 (40h) Charge Pump (1)	15	CP_ENA	0	Charge Pump Enable 0 = Disabled 1 = Enabled	

Register 40h Charge Pump (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R65 (41h) Charge Pump (2)	15	CP_DISCH	1	Charge Pump Discharge Select 0 = Charge Pump outputs floating when disabled 1 = Charge Pump outputs discharged when disabled	

Register 41h Charge Pump (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R80 (50h) DC Servo (1)	3	DCS_ENA_CHAN_3	0	DC Servo enable for HPOUT2R 0 = Disabled 1 = Enabled	
	2	DCS_ENA_CHAN_2	0	DC Servo enable for HPOUT2L 0 = Disabled 1 = Enabled	
	1	DCS_ENA_CHAN_1	0	DC Servo enable for HPOUT1R 0 = Disabled 1 = Enabled	
	0	DCS_ENA_CHAN_0	0	DC Servo enable for HPOUT1L 0 = Disabled 1 = Enabled	

Register 50h DC Servo (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R81 (51h) DC Servo (2)	15	DCS_TRIG_SINGLE_3	0	Writing 1 to this bit selects a single DC offset correction for HPOUT2R. In readback, a value of 1 indicates that the DC Servo single correction is in progress.	
	14	DCS_TRIG_SINGLE_2	0	Writing 1 to this bit selects a single DC offset correction for HPOUT2L. In readback, a value of 1 indicates that the DC Servo single correction is in progress.	
	13	DCS_TRIG_SINGLE_1	0	Writing 1 to this bit selects a single DC offset correction for HPOUT1R. In readback, a value of 1 indicates that the DC Servo single correction is in progress.	
	12	DCS_TRIG_SINGLE_0	0	Writing 1 to this bit selects a single DC offset correction for HPOUT1L. In readback, a value of 1 indicates that the DC Servo single correction is in progress.	
	11	DCS_TRIG_SERIES_3	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT2R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	10	DCS_TRIG_SERIES_2	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT2L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	9	DCS_TRIG_SERIES_1	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT1R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	8	DCS_TRIG_SERIES_0	0	Writing 1 to this bit selects a series of DC offset corrections for HPOUT1L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	7	DCS_TRIG_STARTUP_3	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT2R. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.	
	6	DCS_TRIG_STARTUP_2	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT2L. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5	DCS_TRIG_STARTUP_1	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT1R. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.	
	4	DCS_TRIG_STARTUP_0	0	Writing 1 to this bit selects Start-Up DC Servo mode for HPOUT1L. In readback, a value of 1 indicates that the DC Servo Start-Up correction is in progress.	
	3	DCS_TRIG_DAC_WR_3	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT2R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	2	DCS_TRIG_DAC_WR_2	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT2L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	1	DCS_TRIG_DAC_WR_1	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT1R. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	
	0	DCS_TRIG_DAC_WR_0	0	Writing 1 to this bit selects DAC Write DC Servo mode for HPOUT1L. In readback, a value of 1 indicates that the DC Servo DAC Write correction is in progress.	

Register 51h DC Servo (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R82 (52h) DC Servo (3)	11:8	DCS_TIMER_PERIOD_23 [3:0]	0000	Time between periodic updates (HPOUT2L and HPOUT2R). Time is calculated as 0.251s x (2^PERIOD) 0000 = Off 0001 = 0.502s …. 1010 = 257s (4min 17s) 1111 = 8224s (2hr 17ms)	
	3:0	DCS_TIMER_PERIOD_01 [3:0]	0000	Time between periodic updates (HPOUT1L and HPOUT1R). Time is calculated as 0.251s x (2^PERIOD) 0000 = Off 0001 = 0.502s …. 1010 = 257s (4min 17s) 1111 = 8224s (2hr 17ms)	

Register 52h DC Servo (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R84 (54h) DC Servo (5)	14:8	DCS_SERIES_NO_23 [6:0]	010_1010	Number of DC Servo updates to perform in a series event (HPOUT2L and HPOUT2R). 0 = 1 update 1 = 2 updates ... 127 = 128 updates	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:0	DCS_SERIES_NO_01 [6:0]	010_1010	Number of DC Servo updates to perform in a series event (HPOUT1L and HPOUT1R). 0 = 1 update 1 = 2 updates ... 127 = 128 updates	

Register 54h DC Servo (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R85 (55h) DC Servo (6)	15:8	DCS_DAC_WR_VAL_3 [7:0]	0000_0000	Writing to this field sets the DC Offset value for HPOUT2R in DAC Write DC Servo mode. Reading this field gives the current DC Offset value for HPOUT2R. Two's complement format. LSB is 0.25mV. Range is -32mV to +31.75mV	
	7:0	DCS_DAC_WR_VAL_2 [7:0]	0000_0000	Writing to this field sets the DC Offset value for HPOUT2L in DAC Write DC Servo mode. Reading this field gives the current DC Offset value for HPOUT2L. Two's complement format. LSB is 0.25mV. Range is -32mV to +31.75mV	

Register 55h DC Servo (6)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R86 (56h) DC Servo (7)	15:8	DCS_DAC_WR_VAL_1 [7:0]	0000_0000	Writing to this field sets the DC Offset value for HPOUT1R in DAC Write DC Servo mode. Reading this field gives the current DC Offset value for HPOUT2R. Two's complement format. LSB is 0.25mV. Range is -32mV to +31.75mV	
	7:0	DCS_DAC_WR_VAL_0 [7:0]	0000_0000	Writing to this field sets the DC Offset value for HPOUT1L in DAC Write DC Servo mode. Reading this field gives the current DC Offset value for HPOUT2L. Two's complement format. LSB is 0.25mV. Range is -32mV to +31.75mV	

Register 56h DC Servo (7)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R87 (57h) DC Servo Readback 0	11:8	DCS_CAL_COMPLETE [3:0]	0000	DC Servo Complete status 0 = DAC Write or Start-Up DC Servo mode not completed. 1 = DAC Write or Start-Up DC Servo mode complete. Bit [3] = HPOUT2R Bit [2] = HPOUT2L Bit [1] = HPOUT1R	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Bit [0] = HPOUT1L	
	7:4	DCS_DAC_WR_COMPLETE [3:0]	0000	DC Servo DAC Write status 0 = DAC Write DC Servo mode not completed. 1 = DAC Write DC Servo mode complete. Bit [3] = HPOUT2R Bit [2] = HPOUT2L Bit [1] = HPOUT1R Bit [0] = HPOUT1L	
	3:0	DCS_STARTUP_COMPLETE [3:0]	0000	DC Servo Start-Up status 0 = Start-Up DC Servo mode not completed. 1 = Start-Up DC Servo mode complete. Bit [3] = HPOUT2R Bit [2] = HPOUT2L Bit [1] = HPOUT1R Bit [0] = HPOUT1L	

Register 57h DC Servo Readback 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R96 (60h) Analogue HP (1)	7	HPOUT1L_RMV_SHORT	0	Removes HPOUT1L short 0 = HPOUT1L short enabled 1 = HPOUT1L short removed For normal operation, this bit should be set as the final step of the HPOUT1L Enable sequence.	
	6	HPOUT1L_OUTP	0	Enables HPOUT1L output stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the DC offset cancellation has been scheduled.	
	5	HPOUT1L_DLY	0	Enables HPOUT1L intermediate stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the output signal path has been configured, and before DC offset cancellation is scheduled. This bit should be set with at least 20us delay after HPOUT1L_ENA.	
	3	HPOUT1R_RMV_SHORT	0	Removes HPOUT1R short 0 = HPOUT1R short enabled 1 = HPOUT1R short removed For normal operation, this bit should be set as the final step of the HPOUT1R Enable sequence.	
	2	HPOUT1R_OUTP	0	Enables HPOUT1R output stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the DC offset cancellation has been scheduled.	
	1	HPOUT1R_DLY	0	Enables HPOUT1R intermediate stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the output signal path has been configured, and before DC offset cancellation is scheduled. This bit should be set with at least 20us delay after HPOUT1R_ENA.	

Register 60h Analogue HP (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R97 (61h) Analogue HP (2)	7	HPOUT2L_RMV_SHORT	0	Removes HPOUT2L short 0 = HPOUT2L short enabled 1 = HPOUT2L short removed For normal operation, this bit should be set as the final step of the HPOUT2L Enable sequence.	
	6	HPOUT2L_OUTP	0	Enables HPOUT2L output stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the DC offset cancellation has been scheduled.	
	5	HPOUT2L_DLY	0	Enables HPOUT2L intermediate stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the output signal path has been configured, and before DC offset cancellation is scheduled. This bit should be set with at least 20us delay after HPOUT2L_ENA.	
	3	HPOUT2R_RMV_SHORT	0	Removes HPOUT2R short 0 = HPOUT2R short enabled 1 = HPOUT2R short removed For normal operation, this bit should be set as the final step of the HPOUT2R Enable sequence.	
	2	HPOUT2R_OUTP	0	Enables HPOUT2R output stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the DC offset cancellation has been scheduled.	
	1	HPOUT2R_DLY	0	Enables HPOUT2R intermediate stage 0 = Disabled 1 = Enabled For normal operation, this bit should be set to 1 after the output signal path has been configured, and before DC offset cancellation is scheduled. This bit should be set with at least 20us delay after HPOUT2R_ENA.	

Register 61h Analogue HP (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R256 (0100h) Chip Revision	3:0	CHIP_REV [3:0]	0000	Chip revision	

Register 0100h Chip Revision

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R257 (0101h) Control Interface (1)	15	REG_SYNC	1	Selects automatic control of the register access synchroniser. 0 = Synchroniser always disabled 1 = Synchroniser is enabled when SYSCLK is enabled. Note that, if SYSCLK is enabled (using SYSCLK_ENA) but the MCLK or FLL source is not present, then register access is not possible.	
	2	AUTO_INC	1	Enables address auto-increment	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0 = Disabled 1 = Enabled	

Register 0101h Control Interface (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R272 (0110h) Write Sequencer Ctrl (1)	15	WSEQ_ENA	0	Write Sequencer Enable 0 = Disabled 1 = Enabled	
	9	WSEQ_ABORT	0	Writing a 1 to this bit aborts the current sequence and returns control of the device back to the serial control interface.	
	8	WSEQ_START	0	Writing a 1 to this bit starts the write sequencer at the index location selected by WSEQ_START_INDEX. The sequence continues until it reaches an “End of sequence” flag. At the end of the sequence, this bit will be reset by the Write Sequencer.	
	6:0	WSEQ_START_INDEX [6:0]	000_0000	Sequence Start Index. This field determines the memory location of the first command in the selected sequence. There are 127 Write Sequencer RAM addresses: 00h = WSEQ_ADDR0 (R12288) 01h = WSEQ_ADDR1 (R12292) 02h = WSEQ_ADDR2 (R12296) …. 7Fh = WSEQ_ADDR127 (R12796)	

Register 0110h Write Sequencer Ctrl (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R273 (0111h) Write Sequencer Ctrl (2)	8	WSEQ_BUSY	0	Sequencer Busy flag (Read Only). 0 = Sequencer idle 1 = Sequencer busy Note: it is not possible to write to control registers via the control interface while the Sequencer is Busy.	
	6:0	WSEQ_CURRENT_INDEX [6:0]	000_0000	Sequence Current Index. This indicates the memory location of the most recently accessed command in the write sequencer memory. Coding is the same as WSEQ_START_INDEX.	

Register 0111h Write Sequencer Ctrl (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R512 (0200h) AIF Clocking (1)	4:3	SYSCLK_SRC [1:0]	00	SYSCLK Source Select 00 = MCLK1 01 = MCLK2 10 = FLL 11 = Reserved	
	2	SYSCLK_INV	0	SYSCLK Invert 0 = SYSCLK not inverted 1 = SYSCLK inverted	
	1	SYSCLK_DIV	0	SYSCLK Divider 0 = SYSCLK	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = SYSCLK / 2	
	0	SYSCLK_ENA	0	SYSCLK Enable 0 = Disabled 1 = Enabled	

Register 0200h AIF Clocking (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R513 (0201h) AIF Clocking (2)	4:3	DSP2_DIV [1:0]	00	Selects the sample rate for the AIF/DSP2 paths 00 = 48kHz (44.1kHz) 01 = 32kHz (29.4kHz) 10 = 16kHz (14.7kHz) 11 = 8kHz (7.35kHz) The 48kHz-related sample rates assume SYSCLK=12.288MHz. The figures in brackets apply for SYSCLK=11.2896MHz.	
	1:0	DSP1_DIV [1:0]	00	Selects the sample rate for the AIF/DSP1 paths 00 = 48kHz (44.1kHz) 01 = 32kHz (29.4kHz) 10 = 16kHz (14.7kHz) 11 = 8kHz (7.35kHz) The 48kHz-related sample rates assume SYSCLK=12.288MHz. The figures in brackets apply for SYSCLK=11.2896MHz.	

Register 0201h AIF Clocking (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R520 (0208h) Clocking (1)	5	LFCLK_ENA	0	Low Frequency Clocking Mode 0 = Disabled 1 = Enabled	
	4	TOCLK_ENA	1	Slow Clock (TOCLK) Enable 0 = Disabled 1 = Enabled This clock is required for zero-cross timeout.	
	2	AIFCLK_ENA	0	AIF Clock Enable 0 = Disabled 1 = Enabled	
	1	SYSDSPCLK_ENA	0	DSP Clock Enable 0 = Disabled 1 = Enabled	

Register 0208h Clocking (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R521 (0209h) Clocking (2)	10:8	TOCLK_DIV [2:0]	000	Slow Clock (TOCLK) Divider (Sets TOCLK rate relative to 256kHz.) 000 = Divide by 256 (1kHz) 001 = Divide by 512 (500Hz) 010 = Divide by 1024 (250Hz)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				011 = Divide by 2048 (125Hz) 100 = Divide by 4096 (62.5Hz) 101 = Divide by 8192 (31.2Hz) 110 = Divide by 16384 (15.6Hz) 111 = Divide by 32768 (7.8Hz)	
	7:4	DBCLK_DIV [3:0]	0000	De-bounce Clock (DBCLK) Divider (Sets DBCLK rate relative to 256kHz. The de-bounce time, quoted in brackets, corresponds to 2 cycles of DBCLK) 0000 = Divide by 16 (125us) 0001 = Divide by 32 (250us) 0010 = Divide by 64 (500us) 0011 = Divide by 128 (1ms) 0100 = Divide by 256 (2ms) 0101 = Divide by 512 (4ms) 0110 = Divide by 1024 (8ms) 0111 = Divide by 2048 (16ms) 1000 = Divide by 4096 (32ms) 1001 = Divide by 8192 (64ms) 1010 = Divide by 16384 (128ms) 1011 = Divide by 32768 (256ms) 1100 = Divide by 65536 (512ms) When LFCLK_ENA = 1, the DBCLK rate is set relative to SYSCLK. In this case, with 32kHz SYSCLK, the de-bounce times above are multiplied by 8.	
	2:0	OPCLK_DIV [2:0]	000	GPIO Output Clock (OPCLK) Divider 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16	

Register 0209h Clocking (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R528 (0210h) AIF Rate	0	SYSCLK_RATE	1	SYSCLK Rate 0 = 6.144MHz (or 5.6448MHz) 1 = 12.288MHz (or 11.2896MHz) Note that the device functionality is limited when SYSCLK_RATE=0. This is a power saving mode, which supports AIF1 playback to Headphone outputs, provided the DRC, EQ and 3D functions are all disabled.	

Register 0210h AIF Rate

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R544 (0220h) FLL Control (1)	1	FLL_OSC_ENA	0	FLL Oscillator enable 0 = Disabled 1 = Enabled (Note that this field is required for free-running FLL modes	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				only)	
	0	FLL_ENA	0	FLL Enable 0 = Disabled 1 = Enabled	

Register 0220h FLL Control (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R545 (0221h) FLL Control (2)	13:8	FLL_OUTDIV [5:0]	00_0000	FLL FOUT clock ratio 000000 = Reserved 000001 = 2 000010 = 3 000011 = 4 000100 = 5 000101 = 6 … 111110 = 63 111111 = 64 (FOUT = FVCO / FLL_OUTDIV)	
	6:4		000	Reserved - Do not change	
	2:0	FLL_FRATIO [2:0]	000	FLL FVCO clock ratio 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16	

Register 0221h FLL Control (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R546 (0222h) FLL Control (3)	15:0	FLL_THETA [15:0]	0000_0000_0000_0000	FLL Fractional multiply for FREF This field sets the numerator (multiply) part of the FLL_THETA / FLL_LAMBDA ratio. Coded as LSB = 1	

Register 0222h FLL Control (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R547 (0223h) FLL Control (4)	14:5	FLL_N [9:0]	10_1110_1110	FLL Integer multiply for FREF (LSB = 1)	
	3:0	FLL_LOOP_GAIN [3:0]	0000	Gain applied to error 0000 = x 1 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Recommended that this should be set to 0101 (x32) when the input reference frequency is 3MHz or higher. Recommended that this should be set to 0000 (x1) in all other cases.	

Register 0223h FLL Control (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R548 (0224h) FLL Control (5)	12:7	FLL_FRC_NCO_VAL [5:0]	01_1001	FLL Forced oscillator value Valid range is 000000 to 111111 0x19h (011001) = 12MHz approx (Note that this field is required for free-running FLL modes only)	
	6	FLL_FRC_NCO	0	FLL Forced control select 0 = Normal 1 = FLL oscillator controlled by FLL_FRC_NCO_VAL (Note that this field is required for free-running FLL modes only)	
	4:3	FLL_REFCLK_DIV [1:0]	00	FLL Clock Reference Divider 00 = MCLK / 1 01 = MCLK / 2 10 = MCLK / 4 11 = MCLK / 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.	
	2	FLL_REF_FREQ	1	Low frequency reference locking 0 = High frequency reference locking (recommended for reference clock > 48kHz) 1 = Lock frequency reference locking (recommended for reference clock <= 48kHz)	
	1:0	FLL_REFCLK_SRC [1:0]	00	FLL Clock source 00 = MCLK1 01 = MCLK2 10 = DACLRCLK1 11 = BCLK1	

Register 0224h FLL Control (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R549 (0225h) FLL Control (6)	3:2	FLL_REFCLK_SRC_STS [1:0]	00	FLL Clock Source (Read Only) 00 = MCLK1 01 = MCLK2 10 = DACLRCLK1 11 = BCLK1 Writing to FLL_REFCLK_SRC while the FLL is enabled will not change the FLL Clock source until a 1 is written to FLL_SWITCH_CLK. The read-only FLL_REFCLK_SRC_STS field indicates the active FLL Clock source.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	FLL_SWITCH_CLK	0	FLL Clock Switch Writing a 1 to this bit will cause the FLL configuration to be updated. (Updates to the FLL control registers while the FLL is enabled will not change the FLL output frequency until a 1 is written to FLL_SWITCH_CLK.)	

Register 0225h FLL Control (6)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R550 (0226h) FLL EFS 1	15:0	FLL_LAMBDA [15:0]	0000_0000_0000_0000	FLL Fractional multiply for FREF This field sets the denominator (dividing) part of the FLL_THETA / FLL_LAMBDA ratio. Coded as LSB = 1.	

Register 0226h FLL EFS 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R551 (0227h) FLL EFS 2	2:1	FLL_LFSR_SEL [1:0]	01	FLL EFS Dither Mode select 11 is recommended when FLL_EFS_ENA = 1.	
	0	FLL_EFS_ENA	0	FLL Fractional Mode EFS enable 0 = Integer Mode 1 = Fractional Mode This bit should be set to 1 when FLL_THETA > 0.	

Register 0227h FLL EFS 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R768 (0300h) AIF1 Control	2	AIF1_TRI	0	AIF1 Tri-State Control 0 = Disabled (normal operation) 1 = Enabled (all AIF1 outputs tri-stated)	
	1:0	AIF1_FMT [1:0]	00	AIF1 Digital Audio Interface Format 00 = DSP Mode A 01 = DSP Mode B 10 = I2S mode 11 = Left Justified mode	

Register 0300h AIF1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R769 (0301h) AIF1 BCLK	10	AIF1_BCLK_INV	0	BCLK1 Invert 0 = BCLK1 not inverted 1 = BCLK1 inverted	
	9	AIF1_BCLK_FRC	0	Force BCLK1 output in Master and Slave modes 0 = Normal 1 = BCLK1 enabled at all times (including when all AIF1 channels are disabled)	
	8	AIF1_BCLK_MSTR	0	Select BCLK1 Master mode 0 = Slave Mode 1 = Master Mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	AIF1_BCLK_DIV [3:0]	0000	BCLK1 Rate 0000 = AIFCLK 0001 = AIFCLK / 2 0010 = AIFCLK / 3 0011 = AIFCLK / 4 0100 = AIFCLK / 6 0101 = AIFCLK / 8 0110 = AIFCLK / 12 0111 = AIFCLK / 16 1000 = AIFCLK / 24 1001 = AIFCLK / 32 1010 = AIFCLK / 48 1011 = AIFCLK / 64 1100 = AIFCLK / 96 1101 = AIFCLK / 96 1110 = AIFCLK / 96 1111 = AIFCLK / 96 All other codes are Reserved	

Register 0301h AIF1 BCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R770 (0302h) AIF1 TX LRCLK(1)	10:0	AIF1TX_RATE [10:0]	000_1000_0000	ADCLRCLK1 Rate ADCLRCLK1 clock output = BCLK1 / AIF1TX_RATE Integer (LSB = 1) Valid from 8..2047	

Register 0302h AIF1 TX LRCLK(1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R771 (0303h) AIF1 TX LRCLK(2)	3	AIF1TX_LRCLK_MODE	1	AIF1 output path LRCLK select 0 = Use ADCLRCLK1 1 = Use DACLRCLK1	
	2	AIF1TX_LRCLK_INV	0	ADCLRCLK1 Invert 0 = ADCLRCLK1 not inverted 1 = ADCLRCLK1 inverted	
	1	AIF1TX_LRCLK_FRC	0	Force ADCLRCLK1 output in Master and Slave modes 0 = Normal 1 = ADCLRCLK1 enabled at all times (including when all AIF1 channels are disabled) Note that an internal or external BCLK1 signal must be present for ADCLRCLK1 output.	
	0	AIF1TX_LRCLK_MSTR	0	Select ADCLRCLK1 Master mode 0 = Slave Mode 1 = Master Mode	

Register 0303h AIF1 TX LRCLK(2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R772 (0304h) AIF1 RX LRCLK(1)	10:0	AIF1RX_RATE [10:0]	000_1000_0000	DACLRCLK1 Rate DACLRCLK1 clock output = BCLK1 / AIF1RX_RATE Integer (LSB = 1) Valid from 8..2047	

Register 0304h AIF1 RX LRCLK(1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R773 (0305h) AIF1 RX LRCLK(2)	2	AIF1RX_LRCLK_INV	0	DACLRCLK1 Invert 0 = DACLRCLK1 not inverted 1 = DACLRCLK1 inverted	
	1	AIF1RX_LRCLK_FRC	0	Force DACLRCLK1 output in Master and Slave modes 0 = Normal 1 = DACLRCLK1 enabled at all times (including when all AIF1 channels are disabled) Note that an internal or external BCLK1 signal must be present for DACLRCLK1 output.	
	0	AIF1RX_LRCLK_MSTR	0	Select DACLRCLK1 Master mode 0 = Slave Mode 1 = Master Mode	

Register 0305h AIF1 RX LRCLK(2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R774 (0306h) AIF1TX Data Configuration (1)	15:8	AIF1TX_WL [7:0]	0001_1000	AIF1 TX Word Length Coded as integer (LSB = 1) Default is 24 bits	
	7:0	AIF1TX_SLOT_LEN [7:0]	0001_1000	AIF1 TX Slot Length Coded as integer (LSB = 1) Default is 24 bits	

Register 0306h AIF1TX Data Configuration (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R775 (0307h) AIF1TX Data Configuration (2)	0	AIF1TX_DAT_TRI	0	ADCDAT1 Tri-State Control 0 = ADCDAT1 is logic 0 during disabled timeslots 1 = ADCDAT1 is tri-stated during disabled timeslots	

Register 0307h AIF1TX Data Configuration (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R776 (0308h) AIF1RX Data Configuration	15:8	AIF1RX_WL [7:0]	0001_1000	AIF1 RX Word Length Coded as integer (LSB = 1) Default is 24 bits	
	7:0	AIF1RX_SLOT_LEN [7:0]	0001_1000	AIF1 RX Slot Length Coded as integer (LSB = 1)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Default is 24 bits	

Register 0308h AIF1RX Data Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R777 (0309h) AIF1TX Channel 0 Configuration	15	AIF1TX_CHAN0_DAT_INV	0	AIF1 TX Channel 0 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1TX_CHAN0_SPACING [5:0]	00_0000	AIF1 TX Channel 0 Slot Spacing Defines the number of slots between successive samples of channel 0 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1TX_CHAN0_SLOTS [2:0]	000	AIF1 TX Channel 0 Number of Slots Defines the number of audio samples of channel 0 within the LRCLK frame 000 = TX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1TX_CHAN0_ENA = 1.	
	5:0	AIF1TX_CHAN0_START_SLOT [5:0]	00_0000	AIF1 TX Channel 0 Start Slot position Defines the timeslot position of the first audio sample of channel 0 Integer (LSB=1); Valid from 0 to 63	

Register 0309h AIF1TX Channel 0 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R778 (030Ah) AIF1TX Channel 1 Configuration	15	AIF1TX_CHAN1_DAT_INV	0	AIF1 TX Channel 1 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1TX_CHAN1_SPACING [5:0]	00_0000	AIF1 TX Channel 1 Slot Spacing Defines the number of slots between successive samples of channel 1 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1TX_CHAN1_SLOTS [2:0]	000	AIF1 TX Channel 1 Number of Slots Defines the number of audio samples of channel 1 within the LRCLK frame 000 = TX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1TX_CHAN1_ENA = 1.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5:0	AIF1TX_CHAN1_START_SLOT [5:0]	00_0000	AIF1 TX Channel 1 Start Slot position Defines the timeslot position of the first audio sample of channel 1 Integer (LSB=1); Valid from 0 to 63	

Register 030Ah AIF1TX Channel 1 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R779 (030Bh) AIF1TX Channel 2 Configuration	15	AIF1TX_CHAN2_DAT_INV	0	AIF1 TX Channel 2 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1TX_CHAN2_SPACING [5:0]	00_0000	AIF1 TX Channel 2 Slot Spacing Defines the number of slots between successive samples of channel 2 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1TX_CHAN2_SLOTS [2:0]	000	AIF1 TX Channel 2 Number of Slots Defines the number of audio samples of channel 2 within the LRCLK frame 000 = TX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1TX_CHAN2_ENA = 1.	
	5:0	AIF1TX_CHAN2_START_SLOT [5:0]	00_0000	AIF1 TX Channel 2 Start Slot position Defines the timeslot position of the first audio sample of channel 2 Integer (LSB=1); Valid from 0 to 63	

Register 030Bh AIF1TX Channel 2 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R780 (030Ch) AIF1TX Channel 3 Configuration	15	AIF1TX_CHAN3_DAT_INV	0	AIF1 TX Channel 3 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1TX_CHAN3_SPACING [5:0]	00_0000	AIF1 TX Channel 3 Slot Spacing Defines the number of slots between successive samples of channel 3 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1TX_CHAN3_SLOTS [2:0]	000	AIF1 TX Channel 3 Number of Slots Defines the number of audio samples of channel 3 within the LRCLK frame 000 = TX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1TX_CHAN3_ENA = 1.	
	5:0	AIF1TX_CHAN3_START_SLOT [5:0]	00_0000	AIF1 TX Channel 3 Start Slot position Defines the timeslot position of the first audio sample of channel 3 Integer (LSB=1); Valid from 0 to 63	

Register 030Ch AIF1TX Channel 3 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R781 (030Dh) AIF1TX Channel 4 Configuration	15	AIF1TX_CHAN4_DAT_INV	0	AIF1 TX Channel 4 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1TX_CHAN4_SPACING [5:0]	00_0000	AIF1 TX Channel 4 Slot Spacing Defines the number of slots between successive samples of channel 4 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1TX_CHAN4_SLOTS [2:0]	000	AIF1 TX Channel 4 Number of Slots Defines the number of audio samples of channel 4 within the LRCLK frame 000 = TX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1TX_CHAN4_ENA = 1.	
	5:0	AIF1TX_CHAN4_START_SLOT [5:0]	00_0000	AIF1 TX Channel 4 Start Slot position Defines the timeslot position of the first audio sample of channel 4 Integer (LSB=1); Valid from 0 to 63	

Register 030Dh AIF1TX Channel 4 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R782 (030Eh) AIF1TX Channel 5 Configuration	15	AIF1TX_CHAN5_DAT_INV	0	AIF1 TX Channel 5 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1TX_CHAN5_SPACING [5:0]	00_0000	AIF1 TX Channel 5 Slot Spacing Defines the number of slots between successive samples of channel 5 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1TX_CHAN5_SLOTS [2:0]	000	AIF1 TX Channel 5 Number of Slots Defines the number of audio samples of channel 5 within the LRCLK frame 000 = TX channel is unused 001 = 1 sample 010 = 2 samples	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1TX_CHAN5_ENA = 1.	
	5:0	AIF1TX_CHAN5_START_SLOT [5:0]	00_0000	AIF1 TX Channel 5 Start Slot position Defines the timeslot position of the first audio sample of channel 5 Integer (LSB=1); Valid from 0 to 63	

Register 030Eh AIF1TX Channel 5 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R783 (030Fh) AIF1RX Channel 0 Configuration	15	AIF1RX_CHAN0_DAT_INV	0	AIF1 RX Channel 0 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1RX_CHAN0_SPACING [5:0]	00_0000	AIF1 RX Channel 0 Slot Spacing Defines the number of slots between successive samples of channel 0 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1RX_CHAN0_SLOTS [2:0]	000	AIF1 RX Channel 0 Number of Slots Defines the number of audio samples of channel 0 within the LRCLK frame 000 = RX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1RX_CHAN0_ENA = 1.	
	5:0	AIF1RX_CHAN0_START_SLOT [5:0]	00_0000	AIF1 RX Channel 0 Start Slot position Defines the timeslot position of the first audio sample of channel 0 Integer (LSB=1); Valid from 0 to 63	

Register 030Fh AIF1RX Channel 0 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R784 (0310h) AIF1RX Channel 1 Configuration	15	AIF1RX_CHAN1_DAT_INV	0	AIF1 RX Channel 1 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1RX_CHAN1_SPACING [5:0]	00_0000	AIF1 RX Channel 1 Slot Spacing Defines the number of slots between successive samples of channel 1 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1RX_CHAN1_SLOTS [2:0]	000	AIF1 RX Channel 1 Number of Slots Defines the number of audio samples of channel 1 within the LRCLK frame	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				000 = RX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1RX_CHAN1_ENA = 1.	
	5:0	AIF1RX_CHAN1_START_SLOT [5:0]	00_0000	AIF1 RX Channel 1 Start Slot position Defines the timeslot position of the first audio sample of channel 1 Integer (LSB=1); Valid from 0 to 63	

Register 0310h AIF1RX Channel 1 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R785 (0311h) AIF1RX Channel 2 Configuration	15	AIF1RX_CHAN2_DAT_INV	0	AIF1 RX Channel 2 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1RX_CHAN2_SPACING [5:0]	00_0000	AIF1 RX Channel 2 Slot Spacing Defines the number of slots between successive samples of channel 2 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1RX_CHAN2_SLOTS [2:0]	000	AIF1 RX Channel 2 Number of Slots Defines the number of audio samples of channel 2 within the LRCLK frame 000 = RX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1RX_CHAN2_ENA = 1.	
	5:0	AIF1RX_CHAN2_START_SLOT [5:0]	00_0000	AIF1 RX Channel 2 Start Slot position Defines the timeslot position of the first audio sample of channel 2 Integer (LSB=1); Valid from 0 to 63	

Register 0311h AIF1RX Channel 2 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R786 (0312h) AIF1RX Channel 3 Configuration	15	AIF1RX_CHAN3_DAT_INV	0	AIF1 RX Channel 3 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1RX_CHAN3_SPACING [5:0]	00_0000	AIF1 RX Channel 3 Slot Spacing Defines the number of slots between successive samples of channel 3 Integer (LSB=1); Valid from 0 to 63	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	8:6	AIF1RX_CHAN3_SLOTS [2:0]	000	AIF1 RX Channel 3 Number of Slots Defines the number of audio samples of channel 3 within the LRCLK frame 000 = RX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1RX_CHAN3_ENA = 1.	
	5:0	AIF1RX_CHAN3_START_SLOT [5:0]	00_0000	AIF1 RX Channel 3 Start Slot position Defines the timeslot position of the first audio sample of channel 3 Integer (LSB=1); Valid from 0 to 63	

Register 0312h AIF1RX Channel 3 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R787 (0313h) AIF1RX Channel 4 Configuration	15	AIF1RX_CHAN4_DAT_INV	0	AIF1 RX Channel 4 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1RX_CHAN4_SPACING [5:0]	00_0000	AIF1 RX Channel 4 Slot Spacing Defines the number of slots between successive samples of channel 4 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1RX_CHAN4_SLOTS [2:0]	000	AIF1 RX Channel 4 Number of Slots Defines the number of audio samples of channel 4 within the LRCLK frame 000 = RX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1RX_CHAN4_ENA = 1.	
	5:0	AIF1RX_CHAN4_START_SLOT [5:0]	00_0000	AIF1 RX Channel 4 Start Slot position Defines the timeslot position of the first audio sample of channel 4 Integer (LSB=1); Valid from 0 to 63	

Register 0313h AIF1RX Channel 4 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R788 (0314h) AIF1RX Channel 5 Configuration	15	AIF1RX_CHAN5_DAT_INV	0	AIF1 RX Channel 5 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF1RX_CHAN5	00_0000	AIF1 RX Channel 5 Slot Spacing	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
		_SPACING [5:0]		Defines the number of slots between successive samples of channel 5 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF1RX_CHAN5 _SLOTS [2:0]	000	AIF1 RX Channel 5 Number of Slots Defines the number of audio samples of channel 5 within the LRCLK frame 000 = RX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF1RX_CHAN5_ENA = 1.	
	5:0	AIF1RX_CHAN5 _START_SLOT [5:0]	00_0000	AIF1 RX Channel 5 Start Slot position Defines the timeslot position of the first audio sample of channel 5 Integer (LSB=1); Valid from 0 to 63	

Register 0314h AIF1RX Channel 5 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R789 (0315h) AIF1RX Mono Configuration	2	AIF1RX_CHAN4 _MONO_MODE	0	AIF1 RX Channels 4-5 Mono Mode 0 = Disabled 1 = Enabled When enabled, then RX channel 4 is copied onto RX channel 5. Note that channel 5 must be disabled (AIF1RX_CHAN5_ENA = 0).	
	1	AIF1RX_CHAN2 _MONO_MODE	0	AIF1 RX Channels 2-3 Mono Mode 0 = Disabled 1 = Enabled When enabled, then RX channel 2 is copied onto RX channel 3. Note that channel 3 must be disabled (AIF1RX_CHAN3_ENA = 0).	
	0	AIF1RX_CHAN0 _MONO_MODE	0	AIF1 RX Channels 0-1 Mono Mode 0 = Disabled 1 = Enabled When enabled, then RX channel 0 is copied onto RX channel 1. Note that channel 1 must be disabled (AIF1RX_CHAN1_ENA = 0).	

Register 0315h AIF1RX Mono Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R794 (031Ah) AIF1TX Test	2	AIF1TX45_DITH ER_ENA	1	AIF1 TX Channels 4-5 Dither 0 = Disabled 1 = Enabled in 16-bit mode	
	1	AIF1TX23_DITH ER_ENA	1	AIF1 TX Channels 2-3 Dither 0 = Disabled 1 = Enabled in 16-bit mode	
	0	AIF1TX01_DITH	1	AIF1 TX Channels 0-1 Dither	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
		ER_ENA		0 = Disabled 1 = Enabled in 16-bit mode	

Register 031Ah AIF1TX Test

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R800 (0320h) AIF2 Control	2	AIF2_TRI	0	AIF2 Tri-State Control 0 = Disabled (normal operation) 1 = Enabled (all AIF2 outputs tri-stated)	
	1:0	AIF2_FMT [1:0]	00	AIF2 Digital Audio Interface Format 00 = DSP Mode A 01 = DSP Mode B 10 = I2S mode 11 = Left Justified mode	

Register 0320h AIF2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R801 (0321h) AIF2 BCLK	10	AIF2_BCLK_INV	0	BCLK2 Invert 0 = BCLK2 not inverted 1 = BCLK2 inverted	
	9	AIF2_BCLK_FRC	0	Force BCLK2 output in Master and Slave modes 0 = Normal 1 = BCLK2 enabled at all times (including when both AIF2 channels are disabled)	
	8	AIF2_BCLK_MSTR	0	Select BCLK2 Master mode 0 = Slave Mode 1 = Master Mode	
	3:0	AIF2_BCLK_DIV [3:0]	0000	BCLK2 Rate 0000 = AIFCLK 0001 = AIFCLK / 2 0010 = AIFCLK / 3 0011 = AIFCLK / 4 0100 = AIFCLK / 6 0101 = AIFCLK / 8 0110 = AIFCLK / 12 0111 = AIFCLK / 16 1000 = AIFCLK / 24 1001 = AIFCLK / 32 1010 = AIFCLK / 48 1011 = AIFCLK / 64 1100 = AIFCLK / 96 1101 = AIFCLK / 96 1110 = AIFCLK / 96 1111 = AIFCLK / 96 All other codes are Reserved	

Register 0321h AIF2 BCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R802 (0322h) AIF2 TX LRCLK(1)	10:0	AIF2TX_RATE [10:0]	000_1000_0000	ADCLRCLK2 Rate ADCLRCLK2 clock output = BCLK2 / AIF2TX_RATE Integer (LSB = 1) Valid from 8..2047	

Register 0322h AIF2 TX LRCLK(1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R803 (0323h) AIF2 TX LRCLK(2)	3	AIF2TX_LRCLK_MODE	1	AIF2 output path LRCLK select 0 = Use ADCLRCLK2 1 = Use DACLRCLK2	
	2	AIF2TX_LRCLK_INV	0	ADCLRCLK2 Invert 0 = ADCLRCLK2 not inverted 1 = ADCLRCLK2 inverted	
	1	AIF2TX_LRCLK_FRC	0	Force ADCLRCLK2 output in Master and Slave modes 0 = Normal 1 = ADCLRCLK2 enabled at all times (including when both AIF2 channels are disabled) Note that an internal or external BCLK2 signal must be present for ADCLRCLK2 output.	
	0	AIF2TX_LRCLK_MSTR	0	Select ADCLRCLK2 Master mode 0 = Slave Mode 1 = Master Mode	

Register 0323h AIF2 TX LRCLK(2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R804 (0324h) AIF2 RX LRCLK(1)	10:0	AIF2RX_RATE [10:0]	000_1000_0000	DACLRCLK2 Rate DACLRCLK2 clock output = BCLK2 / AIF2RX_RATE Integer (LSB = 1) Valid from 8..2047	

Register 0324h AIF2 RX LRCLK(1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R805 (0325h) AIF2 RX LRCLK(2)	2	AIF2RX_LRCLK_INV	0	DACLRCLK2 Invert 0 = DACLRCLK2 not inverted 1 = DACLRCLK2 inverted	
	1	AIF2RX_LRCLK_FRC	0	Force DACLRCLK2 output in Master and Slave modes 0 = Normal 1 = DACLRCLK2 enabled at all times (including when both AIF2 channels are disabled) Note that an internal or external BCLK2 signal must be present for DACLRCLK2 output.	
	0	AIF2RX_LRCLK_MSTR	0	Select DACLRCLK2 Master mode 0 = Slave Mode 1 = Master Mode	

Register 0325h AIF2 RX LRCLK(2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R806 (0326h) AIF2TX Data Configuration (1)	15:8	AIF2TX_WL [7:0]	0001_1000	AIF2 TX Word Length Coded as integer (LSB = 1) Default is 24 bits	
	7:0	AIF2TX_SLOT_LEN [7:0]	0001_1000	AIF2 TX Slot Length Coded as integer (LSB = 1) Default is 24 bits	

Register 0326h AIF2TX Data Configuration (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R807 (0327h) AIF2TX Data Configuration (2)	0	AIF2TX_DAT_TRI	0	ADCDAT2 Tri-State Control 0 = ADCDAT2 is logic 0 during disabled timeslots 1 = ADCDAT2 is tri-stated during disabled timeslots	

Register 0327h AIF2TX Data Configuration (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R808 (0328h) AIF2RX Data Configuration	15:8	AIF2RX_WL [7:0]	0001_1000	AIF2 RX Word Length Coded as integer (LSB = 1) Default is 24 bits	
	7:0	AIF2RX_SLOT_LEN [7:0]	0001_1000	AIF2 RX Slot Length Coded as integer (LSB = 1) Default is 24 bits	

Register 0328h AIF2RX Data Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R809 (0329h) AIF2TX Channel 0 Configuration	15	AIF2TX_CHAN0_DAT_INV	0	AIF2 TX Channel 0 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF2TX_CHAN0_SPACING [5:0]	00_0000	AIF2 TX Channel 0 Slot Spacing Defines the number of slots between successive samples of channel 0 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF2TX_CHAN0_SLOTS [2:0]	000	AIF2 TX Channel 0 Number of Slots Defines the number of audio samples of channel 0 within the LRCLK frame 000 = TX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF2TX_CHAN0_ENA = 1.	
	5:0	AIF2TX_CHAN0_START_SLOT	00_0000	AIF2 TX Channel 0 Start Slot position Defines the timeslot position of the first audio sample of	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
		[5:0]		channel 0 Integer (LSB=1); Valid from 0 to 63	

Register 0329h AIF2TX Channel 0 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R810 (032Ah) AIF2TX Channel 1 Configuration	15	AIF2TX_CHAN1_DAT_INV	0	AIF2 TX Channel 1 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF2TX_CHAN1_SPACING [5:0]	00_0000	AIF2 TX Channel 1 Slot Spacing Defines the number of slots between successive samples of channel 1 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF2TX_CHAN1_SLOTS [2:0]	000	AIF2 TX Channel 1 Number of Slots Defines the number of audio samples of channel 1 within the LRCLK frame 000 = TX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF2TX_CHAN1_ENA = 1.	
	5:0	AIF2TX_CHAN1_START_SLOT [5:0]	00_0000	AIF2 TX Channel 1 Start Slot position Defines the timeslot position of the first audio sample of channel 1 Integer (LSB=1); Valid from 0 to 63	

Register 032Ah AIF2TX Channel 1 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R811 (032Bh) AIF2RX Channel 0 Configuration	15	AIF2RX_CHAN0_DAT_INV	0	AIF2 RX Channel 0 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF2RX_CHAN0_SPACING [5:0]	00_0000	AIF2 RX Channel 0 Slot Spacing Defines the number of slots between successive samples of channel 0 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF2RX_CHAN0_SLOTS [2:0]	000	AIF2 RX Channel 0 Number of Slots Defines the number of audio samples of channel 0 within the LRCLK frame 000 = RX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF2RX_CHAN0_ENA	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				= 1.	
	5:0	AIF2RX_CHAN0_START_SLOT [5:0]	00_0000	AIF2 RX Channel 0 Start Slot position Defines the timeslot position of the first audio sample of channel 0 Integer (LSB=1); Valid from 0 to 63	

Register 032Bh AIF2RX Channel 0 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R812 (032Ch) AIF2RX Channel 1 Configuration	15	AIF2RX_CHAN1_DAT_INV	0	AIF2 RX Channel 1 Invert 0 = Not inverted 1 = Inverted	
	14:9	AIF2RX_CHAN1_SPACING [5:0]	00_0000	AIF2 RX Channel 1 Slot Spacing Defines the number of slots between successive samples of channel 1 Integer (LSB=1); Valid from 0 to 63	
	8:6	AIF2RX_CHAN1_SLOTS [2:0]	000	AIF2 RX Channel 1 Number of Slots Defines the number of audio samples of channel 1 within the LRCLK frame 000 = RX channel is unused 001 = 1 sample 010 = 2 samples 011 = 3 samples 100 = 4 samples 101 = 5 samples 110 = 6 samples 111 = Reserved Note that 000 is not a valid setting if AIF2RX_CHAN1_ENA = 1.	
	5:0	AIF2RX_CHAN1_START_SLOT [5:0]	00_0000	AIF2 RX Channel 1 Start Slot position Defines the timeslot position of the first audio sample of channel 1 Integer (LSB=1); Valid from 0 to 63	

Register 032Ch AIF2RX Channel 1 Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R813 (032Dh) AIF2RX Mono Configuration	0	AIF2RX_CHAN0_MONO_MODE	0	AIF2 RX Mono Mode 0 = Disabled 1 = Enabled When enabled, then RX channel 1 is copied onto RX channel 0. Note that channel 1 must be disabled (AIF2RX_CHAN1_ENA = 0).	

Register 032Dh AIF2RX Mono Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R815 (032Fh) AIF2TX Test	0	AIF2TX_DITHER_ENA	1	AIF2 TX Dither 0 = Disabled 1 = Enabled in 16-bit mode	

Register 032Fh AIF2TX Test

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1024 (0400h) DSP1 TX Left Volume	8	DSP1TX_VU	0	DSP1 TX output path Volume Update Writing a 1 to this bit will cause the DSP1TXL and DSP1TXR volume to be updated simultaneously	
	7:0	DSP1TXL_VOL [7:0]	1100_0000	DSP1 TX (Left) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB	

Register 0400h DSP1 TX Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1025 (0401h) DSP1 TX Right Volume	8	DSP1TX_VU	0	DSP1 TX output path Volume Update Writing a 1 to this bit will cause the DSP1TXL and DSP1TXR volume to be updated simultaneously	
	7:0	DSP1TXR_VOL [7:0]	1100_0000	DSP1 TX (Right) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB	

Register 0401h DSP1 TX Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1026 (0402h) DSP1 RX Left Volume	8	DSP1RX_VU	0	DSP1 RX input path Volume Update Writing a 1 to this bit will cause the DSP1RXL and DSP1RXR volume to be updated simultaneously	
	7:0	DSP1RXL_VOL [7:0]	1100_0000	DSP1 RX (Left) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0402h DSP1 RX Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1027 (0403h) DSP1 RX Right Volume	8	DSP1RX_VU	0	DSP1 RX input path Volume Update Writing a 1 to this bit will cause the DSP1RXL and DSP1RXR volume to be updated simultaneously	
	7:0	DSP1RXR_VOL [7:0]	1100_0000	DSP1 RX (Right) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0403h DSP1 RX Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1040 (0410h) DSP1 TX Filters	13	DSP1TX_NF	1	DSP1 TX output path Digital Notch Filter Enable 0 = Disabled at all times 1 = Enabled in 8kHz and 16kHz modes	
	12	DSP1TXL_HPF	0	DSP1 TX (Left) output path Digital HPF Enable 0 = Disabled 1 = Enabled	
	11	DSP1TXR_HPF	0	DSP1 TX (Right) output path Digital HPF Enable 0 = Disabled 1 = Enabled	
	4:3	DSP1TX_HPF_MODE [1:0]	00	DSP1 TX output path Digital HPF Mode 00 = Hi-Fi mode (cut-off is 3.7Hz) 01 = Application mode (cut-off is set by DSP1TX_HPF_CUT) 10 = Voice mode (cut-off is 260Hz)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				11 = Reserved Note that Voice mode is only supported for 8kHz and 16kHz sample rates	
	2:0	DSP1TX_HPF_CUT [2:0]	000	DSP1 TX output path Digital HPF cut-off frequency 000 = 50Hz 001 = 75Hz 010 = 100Hz 011 = 150Hz 100 = 200Hz 101 = 300Hz 110 = 400Hz 111 = Reserved Frequencies are correct for 12.288MHz SYSCLK. The cut-off frequencies scale proportionately for other SYSCLK frequencies (eg. 11.2896MHz).	

Register 0410h DSP1 TX Filters

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1056 (0420h) DSP1 RX Filters (1)	9	DSP1RX_MUTE	1	DSP1 RX input path Soft Mute Control 0 = Un-mute 1 = Mute	
	7	DSP1RX_MONO	0	DSP1 RX input path Mono Mix Control 0 = Disabled 1 = Enabled	
	5	DSP1RX_MUTERATE	0	DSP1 RX input path Soft Mute Ramp Rate 0 = Fast ramp (maximum ramp time is 8ms) 1 = Slow ramp (maximum ramp time is 128ms)	
	4	DSP1RX_UNMUTE_RAMP	0	DSP1 RX input path Unmute Ramp select 0 = Disabling soft-mute (DSP1RX_MUTE=0) will cause the volume to change immediately to DSP1RXL_VOL and DSP1RXR_VOL settings 1 = Disabling soft-mute (DSP1RX_MUTE=0) will cause the DAC volume to ramp up gradually to the DSP1RXL_VOL and DSP1RXR_VOL settings	

Register 0420h DSP1 RX Filters (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1057 (0421h) DSP1 RX Filters (2)	13:9	DSP1RX_3D_GAIN [4:0]	0_0000	DSP1 3D Stereo depth 00000 = Off 00001 = Minimum (-16dB) …(0.915dB steps) 11111 = Maximum (+11.5dB)	
	8	DSP1RX_3D_ENA	0	Enable 3D Stereo in DSP1 RX input path 0 = Disabled 1 = Enabled	

Register 0421h DSP1 RX Filters (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1088	15:11	DSP1DRC_SIG	0_0000	DSP1 DRC Signal Detect RMS Threshold.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
(0440h) DSP1 DRC (1)		_DET_RMS [4:0]		This is the RMS signal level for signal detect to be indicated when DSP1DRC_SIG_DET_MODE=1. 00000 = -30dB 00001 = -31.5dB …. (1.5dB steps) 11110 = -75dB 11111 = -76.5dB	
	10:9	DSP1DRC_SIG_DET_PK [1:0]	00	DSP1 DRC Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when DSP1DRC_SIG_DET_MODE=0. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	8	DSP1DRC_NG_ENA	0	DSP1 DRC Noise Gate Enable 0 = Disabled 1 = Enabled	
	7	DSP1DRC_SIG_DET_MODE	1	DSP1 DRC Signal Detect Mode 0 = Peak threshold mode 1 = RMS threshold mode	
	6	DSP1DRC_SIG_DET	0	DSP1 DRC Signal Detect Enable 0 = Disabled 1 = Enabled	
	5	DSP1DRC_KNEE2_OP_ENA	0	DSP1 DRC KNEE2_OP Enable 0 = Disabled 1 = Enabled	
	4	DSP1DRC_QR	1	DSP1 DRC Quick-release Enable 0 = Disabled 1 = Enabled	
	3	DSP1DRC_ANTICLIP	1	DSP1 DRC Anti-clip Enable 0 = Disabled 1 = Enabled	
	2	DSP1RX_DRC_ENA	0	Enable DRC in DSP1 RX input path 0 = Disabled 1 = Enabled	
	1	DSP1TXL_DRC_ENA	0	Enable DRC in DSP1 TX (Left) output path 0 = Disabled 1 = Enabled	
	0	DSP1TXR_DRC_ENA	0	Enable DRC in DSP1 TX (Right) output path 0 = Disabled 1 = Enabled	

Register 0440h DSP1 DRC (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1089 (0441h) DSP1 DRC (2)	12:9	DSP1DRC_ATK [3:0]	0100	DSP1 DRC Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved	
	8:5	DSP1DRC_DCY [3:0]	0010	DSP1 DRC Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved	
	4:2	DSP1DRC_MIN GAIN [2:0]	001	DSP1 DRC Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved	
	1:0	DSP1DRC_MAX GAIN [1:0]	01	DSP1 DRC Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB	

Register 0441h DSP1 DRC (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1090 (0442h) DSP1 DRC (3)	15:12	DSP1DRC_NG_ MINGAIN [3:0]	0000	DSP1 DRC Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved	
	11:10	DSP1DRC_NG_ EXP [1:0]	00	DSP1 DRC Noise Gate slope 00 = 1 (no expansion) 01 = 2	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				10 = 4 11 = 8	
	9:8	DSP1DRC_QR_THR [1:0]	00	DSP1 DRC Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	7:6	DSP1DRC_QR_DCY [1:0]	00	DSP1 DRC Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = Reserved	
	5:3	DSP1DRC_HI_COMP [2:0]	000	DSP1 DRC Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved	
	2:0	DSP1DRC_LO_COMP [2:0]	000	DSP1 DRC Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved	

Register 0442h DSP1 DRC (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1091 (0443h) DSP1 DRC (4)	10:5	DSP1DRC_KNEE_IP [5:0]	00_0000	DSP1 DRC Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved	
	4:0	DSP1DRC_KNEE_OP [4:0]	0_0000	DSP1 DRC Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved	

Register 0443h DSP1 DRC (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1092 (0444h) DSP1 DRC (5)	9:5	DSP1DRC_KNEE2_IP [4:0]	0_0000	DSP1 DRC Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DSP1DRC_NG_ENA = 1.	
	4:0	DSP1DRC_KNEE2_OP [4:0]	0_0000	DSP1 DRC Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DSP1DRC_KNEE2_OP_ENA = 1.	

Register 0444h DSP1 DRC (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1152 (0480h) DSP1 RX EQ Gains (1)	15:11	DSP1RX_EQ_B1_GAIN [4:0]	0_1100	DSP1 EQ Band 1 Gain -12dB to +12dB in 1dB steps	
	10:6	DSP1RX_EQ_B2_GAIN [4:0]	0_1100	DSP1 EQ Band 2 Gain -12dB to +12dB in 1dB steps	
	5:1	DSP1RX_EQ_B3_GAIN [4:0]	0_1100	DSP1 EQ Band 3 Gain -12dB to +12dB in 1dB steps	
	0	DSP1RX_EQ_ENA	0	Enable EQ in DSP1 RX input path 0 = Disabled 1 = Enabled	

Register 0480h DSP1 RX EQ Gains (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1153 (0481h) DSP1 RX EQ Gains (2)	15:11	DSP1RX_EQ_B4_GAIN [4:0]	0_1100	DSP1 EQ Band 4 Gain -12dB to +12dB in 1dB steps	
	10:6	DSP1RX_EQ_B5_GAIN [4:0]	0_1100	DSP1 EQ Band 5 Gain -12dB to +12dB in 1dB steps	

Register 0481h DSP1 RX EQ Gains (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1154 (0482h) DSP1 RX EQ Band 1 A	15:0	DSP1RX_EQ_B1_A [15:0]	0000_1111_1100_1010	EQ Band 1 Coefficient A	

Register 0482h DSP1 RX EQ Band 1 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1155 (0483h) DSP1 RX EQ Band 1 B	15:0	DSP1RX_EQ_B1_B [15:0]	0000_0100_0000_0000	EQ Band 1 Coefficient B	

Register 0483h DSP1 RX EQ Band 1 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1156 (0484h) DSP1 RX EQ Band 1 PG	15:0	DSP1RX_EQ_B1_PG [15:0]	0000_0000_1101_1000	EQ Band 1 Coefficient PG	

Register 0484h DSP1 RX EQ Band 1 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1157 (0485h) DSP1 RX EQ Band 2 A	15:0	DSP1RX_EQ_B2_A [15:0]	0001_1110_1011_0101	EQ Band 2 Coefficient A	

Register 0485h DSP1 RX EQ Band 2 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1158 (0486h) DSP1 RX EQ Band 2 B	15:0	DSP1RX_EQ_B2_B [15:0]	1111_0001_0100_0101	EQ Band 2 Coefficient B	

Register 0486h DSP1 RX EQ Band 2 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1159 (0487h) DSP1 RX EQ Band 2 C	15:0	DSP1RX_EQ_B2_C [15:0]	0000_1011_0111_0101	EQ Band 2 Coefficient C	

Register 0487h DSP1 RX EQ Band 2 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1160 (0488h) DSP1 RX EQ Band 2 PG	15:0	DSP1RX_EQ_B2_PG [15:0]	0000_0001_1100_0101	EQ Band 2 Coefficient PG	

Register 0488h DSP1 RX EQ Band 2 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1161 (0489h) DSP1 RX EQ Band 3 A	15:0	DSP1RX_EQ_B3_A [15:0]	0001_1100_0101_1000	EQ Band 3 Coefficient A	

Register 0489h DSP1 RX EQ Band 3 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1162 (048Ah) DSP1 RX EQ Band 3 B	15:0	DSP1RX_EQ_B3_B [15:0]	1111_0011_0111_0011	EQ Band 3 Coefficient B	

Register 048Ah DSP1 RX EQ Band 3 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1163 (048Bh) DSP1 RX EQ Band 3 C	15:0	DSP1RX_EQ_B3_C [15:0]	0000_1010_0101_0100	EQ Band 3 Coefficient C	

Register 048Bh DSP1 RX EQ Band 3 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1164 (048Ch) DSP1 RX EQ Band 3 PG	15:0	DSP1RX_EQ_B3_PG [15:0]	0000_0101_0101_1000	EQ Band 3 Coefficient PG	

Register 048Ch DSP1 RX EQ Band 3 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1165 (048Dh) DSP1 RX EQ Band 4 A	15:0	DSP1RX_EQ_B4_A [15:0]	0001_0110_1000_1110	EQ Band 4 Coefficient A	

Register 048Dh DSP1 RX EQ Band 4 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1166 (048Eh) DSP1 RX EQ Band 4 B	15:0	DSP1RX_EQ_B4_B [15:0]	1111_1000_0010_1001	EQ Band 4 Coefficient B	

Register 048Eh DSP1 RX EQ Band 4 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1167	15:0	DSP1RX_EQ_B	0000_0111_1010_110	EQ Band 4 Coefficient C	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
(048Fh) DSP1 RX EQ Band 4 C		4_C [15:0]	1		

Register 048Fh DSP1 RX EQ Band 4 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1168 (0490h) DSP1 RX EQ Band 4 PG	15:0	DSP1RX_EQ_B4_PG [15:0]	0001_0001_0000_0011	EQ Band 4 Coefficient PG	

Register 0490h DSP1 RX EQ Band 4 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1169 (0491h) DSP1 RX EQ Band 5 A	15:0	DSP1RX_EQ_B5_A [15:0]	0000_0101_0110_0100	EQ Band 5 Coefficient A	

Register 0491h DSP1 RX EQ Band 5 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1170 (0492h) DSP1 RX EQ Band 5 B	15:0	DSP1RX_EQ_B5_B [15:0]	0000_0101_0101_1001	EQ Band 5 Coefficient B	

Register 0492h DSP1 RX EQ Band 5 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1171 (0493h) DSP1 RX EQ Band 5 PG	15:0	DSP1RX_EQ_B5_PG [15:0]	0100_0000_0000_0000	EQ Band 5 Coefficient PG	

Register 0493h DSP1 RX EQ Band 5 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1280 (0500h) DSP2 TX Left Volume	8	DSP2TX_VU	0	DSP2 TX output path Volume Update Writing a 1 to this bit will cause the DSP2TXL and DSP2TXR volume to be updated simultaneously	
	7:0	DSP2TXL_VOL [7:0]	1100_0000	DSP2 TX (Left) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB	

Register 0500h DSP2 TX Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1281 (0501h) DSP2 TX Right Volume	8	DSP2TX_VU	0	DSP2 TX output path Volume Update Writing a 1 to this bit will cause the DSP2TXL and DSP2TXR volume to be updated simultaneously	
	7:0	DSP2TXR_VOL [7:0]	1100_0000	DSP2 TX (Right) output path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) EFh = +17.625dB	

Register 0501h DSP2 TX Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1282 (0502h) DSP2 RX Left Volume	8	DSP2RX_VU	0	DSP2 RX input path Volume Update Writing a 1 to this bit will cause the DSP2RXL and DSP2RXR volume to be updated simultaneously	
	7:0	DSP2RXL_VOL [7:0]	1100_0000	DSP2 RX (Left) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0502h DSP2 RX Left Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1283 (0503h) DSP2 RX Right Volume	8	DSP2RX_VU	0	DSP2 RX input path Volume Update Writing a 1 to this bit will cause the DSP2RXL and DSP2RXR volume to be updated simultaneously	
	7:0	DSP2RXR_VOL [7:0]	1100_0000	DSP2 RX (Right) input path Digital Volume 00h = MUTE 01h = -71.625dB … (0.375dB steps) C0h = 0dB FFh = 0dB	

Register 0503h DSP2 RX Right Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1296 (0510h) DSP2 TX Filters	13	DSP2TX_NF	1	DSP2 TX output path Digital Notch Filter Enable 0 = Disabled at all times 1 = Enabled in 8kHz and 16kHz modes	
	12	DSP2TXL_HPF	0	DSP2 TX (Left) output path Digital HPF Enable 0 = Disabled 1 = Enabled	
	11	DSP2TXR_HPF	0	DSP2 TX (Right) output path Digital HPF Enable 0 = Disabled 1 = Enabled	
	4:3	DSP2TX_HPF_MODE [1:0]	00	DSP2 TX output path Digital HPF Mode 00 = Hi-Fi mode (cut-off is 3.7Hz) 01 = Application mode (cut-off is set by	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				DSP2TX_HPF_CUT) 10 = Voice mode (cut-off is 260Hz) 11 = Reserved Note that Voice mode is only supported for 8kHz and 16kHz sample rates	
	2:0	DSP2TX_HPF_CUT [2:0]	000	DSP2 TX output path Digital HPF cut-off frequency 000 = 50Hz 001 = 75Hz 010 = 100Hz 011 = 150Hz 100 = 200Hz 101 = 300Hz 110 = 400Hz 111 = Reserved Frequencies are correct for 12.288MHz SYSCLK. The cut-off frequencies scale proportionately for other SYSCLK frequencies (eg. 11.2896MHz).	

Register 0510h DSP2 TX Filters

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1312 (0520h) DSP2 RX Filters (1)	9	DSP2RX_MUTE	1	DSP2 RX input path Soft Mute Control 0 = Un-mute 1 = Mute	
	7	DSP2RX_MONO	0	DSP2 RX input path Mono Mix Control 0 = Disabled 1 = Enabled	
	5	DSP2RX_MUTERATE	0	DSP2 RX input path Soft Mute Ramp Rate 0 = Fast ramp (maximum ramp time is 8ms) 1 = Slow ramp (maximum ramp time is 128ms)	
	4	DSP2RX_UNMUTE_RAMP	0	DSP2 RX input path Unmute Ramp select 0 = Disabling soft-mute (DSP2RX_MUTE=0) will cause the volume to change immediately to DSP2RXL_VOL and DSP2RXR_VOL settings 1 = Disabling soft-mute (DSP2RX_MUTE=0) will cause the DAC volume to ramp up gradually to the DSP2RXL_VOL and DSP2RXR_VOL settings	

Register 0520h DSP2 RX Filters (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1313 (0521h) DSP2 RX Filters (2)	13:9	DSP2RX_3D_GAIN [4:0]	0_0000	DSP2 3D Stereo depth 00000 = Off 00001 = Minimum (-16dB) …(0.915dB steps) 11111 = Maximum (+11.5dB)	
	8	DSP2RX_3D_ENA	0	Enable 3D Stereo in DSP2 RX input path 0 = Disabled 1 = Enabled	

Register 0521h DSP2 RX Filters (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1344 (0540h) DSP2 DRC (1)	15:11	DSP2DRC_SIG_DET_RMS [4:0]	0_0000	DSP2 DRC Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when DSP2DRC_SIG_DET_MODE=1. 00000 = -30dB 00001 = -31.5dB …. (1.5dB steps) 11110 = -75dB 11111 = -76.5dB	
	10:9	DSP2DRC_SIG_DET_PK [1:0]	00	DSP2 DRC Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when DSP2DRC_SIG_DET_MODE=0. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	8	DSP2DRC_NG_ENA	0	DSP2 DRC Noise Gate Enable 0 = Disabled 1 = Enabled	
	7	DSP2DRC_SIG_DET_MODE	1	DSP2 DRC Signal Detect Mode 0 = Peak threshold mode 1 = RMS threshold mode	
	6	DSP2DRC_SIG_DET	0	DSP2 DRC Signal Detect Enable 0 = Disabled 1 = Enabled	
	5	DSP2DRC_KNEE2_OP_ENA	0	DSP2 DRC KNEE2_OP Enable 0 = Disabled 1 = Enabled	
	4	DSP2DRC_QR	1	DSP2 DRC Quick-release Enable 0 = Disabled 1 = Enabled	
	3	DSP2DRC_ANTICLIP	1	DSP2 DRC Anti-clip Enable 0 = Disabled 1 = Enabled	
	2	DSP2RX_DRC_ENA	0	Enable DRC in DSP2 RX input path 0 = Disabled 1 = Enabled	
	1	DSP2TXL_DRC_ENA	0	Enable DRC in DSP2 TX (Left) output path 0 = Disabled 1 = Enabled	
	0	DSP2TXR_DRC_ENA	0	Enable DRC in DSP2 TX (Right) output path 0 = Disabled 1 = Enabled	

Register 0540h DSP2 DRC (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1345 (0541h) DSP2 DRC (2)	12:9	DSP2DRC_ATK [3:0]	0100	DSP2 DRC Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved	
	8:5	DSP2DRC_DCY [3:0]	0010	DSP2 DRC Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved	
	4:2	DSP2DRC_MIN GAIN [2:0]	001	DSP2 DRC Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved	
	1:0	DSP2DRC_MAX GAIN [1:0]	01	DSP2 DRC Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB	

Register 0541h DSP2 DRC (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1346 (0542h) DSP2 DRC (3)	15:12	DSP2DRC_NG_ MINGAIN [3:0]	0000	DSP2 DRC Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved	
	11:10	DSP2DRC_NG_	00	DSP2 DRC Noise Gate slope	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
		EXP [1:0]		00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8	
	9:8	DSP2DRC_QR_THR [1:0]	00	DSP2 DRC Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	7:6	DSP2DRC_QR_DCY [1:0]	00	DSP2 DRC Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = Reserved	
	5:3	DSP2DRC_HI_COMP [2:0]	000	DSP2 DRC Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved	
	2:0	DSP2DRC_LO_COMP [2:0]	000	DSP2 DRC Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved	

Register 0542h DSP2 DRC (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1347 (0543h) DSP2 DRC (4)	10:5	DSP2DRC_KNEE_IP [5:0]	00_0000	DSP2 DRC Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved	
	4:0	DSP2DRC_KNEE_OP [4:0]	0_0000	DSP2 DRC Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved	

Register 0543h DSP2 DRC (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1348 (0544h) DSP2 DRC (5)	9:5	DSP2DRC_KNEE2_IP [4:0]	0_0000	DSP2 DRC Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DSP2DRC_NG_ENA = 1.	
	4:0	DSP2DRC_KNEE2_OP [4:0]	0_0000	DSP2 DRC Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DSP2DRC_KNEE2_OP_ENA = 1.	

Register 0544h DSP2 DRC (5)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1408 (0580h) DSP2 RX EQ Gains (1)	15:11	DSP2RX_EQ_B1_GAIN [4:0]	0_1100	DSP2 EQ Band 1 Gain -12dB to +12dB in 1dB steps	
	10:6	DSP2RX_EQ_B2_GAIN [4:0]	0_1100	DSP2 EQ Band 2 Gain -12dB to +12dB in 1dB steps	
	5:1	DSP2RX_EQ_B3_GAIN [4:0]	0_1100	DSP2 EQ Band 3 Gain -12dB to +12dB in 1dB steps	
	0	DSP2RX_EQ_ENA	0	Enable EQ in DSP2 RX input path 0 = Disabled 1 = Enabled	

Register 0580h DSP2 RX EQ Gains (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1409 (0581h) DSP2 RX EQ Gains (2)	15:11	DSP2RX_EQ_B4_GAIN [4:0]	0_1100	DSP2 EQ Band 4 Gain -12dB to +12dB in 1dB steps	
	10:6	DSP2RX_EQ_B5_GAIN [4:0]	0_1100	DSP2 EQ Band 5 Gain -12dB to +12dB in 1dB steps	

Register 0581h DSP2 RX EQ Gains (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1410 (0582h) DSP2 RX EQ Band 1 A	15:0	DSP2RX_EQ_B1_A [15:0]	0000_1111_1100_1010	EQ Band 1 Coefficient A	

Register 0582h DSP2 RX EQ Band 1 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1411 (0583h) DSP2 RX EQ Band 1 B	15:0	DSP2RX_EQ_B1_B [15:0]	0000_0100_0000_0000	EQ Band 1 Coefficient B	

Register 0583h DSP2 RX EQ Band 1 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1412 (0584h) DSP2 RX EQ Band 1 PG	15:0	DSP2RX_EQ_B1_PG [15:0]	0000_0000_1101_1000	EQ Band 1 Coefficient PG	

Register 0584h DSP2 RX EQ Band 1 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1413 (0585h) DSP2 RX EQ Band 2 A	15:0	DSP2RX_EQ_B2_A [15:0]	0001_1110_1011_0101	EQ Band 2 Coefficient A	

Register 0585h DSP2 RX EQ Band 2 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1414 (0586h) DSP2 RX EQ Band 2 B	15:0	DSP2RX_EQ_B2_B [15:0]	1111_0001_0100_0101	EQ Band 2 Coefficient B	

Register 0586h DSP2 RX EQ Band 2 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1415 (0587h) DSP2 RX EQ Band 2 C	15:0	DSP2RX_EQ_B2_C [15:0]	0000_1011_0111_0101	EQ Band 2 Coefficient C	

Register 0587h DSP2 RX EQ Band 2 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1416 (0588h) DSP2 RX EQ Band 2 PG	15:0	DSP2RX_EQ_B2_PG [15:0]	0000_0001_1100_0101	EQ Band 2 Coefficient PG	

Register 0588h DSP2 RX EQ Band 2 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1417	15:0	DSP2RX_EQ_B	0001_1100_0101_100	EQ Band 3 Coefficient A	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
(0589h) DSP2 RX EQ Band 3 A		3_A [15:0]	0		

Register 0589h DSP2 RX EQ Band 3 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1418 (058Ah) DSP2 RX EQ Band 3 B	15:0	DSP2RX_EQ_B3_B [15:0]	1111_0011_0111_0011	EQ Band 3 Coefficient B	

Register 058Ah DSP2 RX EQ Band 3 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1419 (058Bh) DSP2 RX EQ Band 3 C	15:0	DSP2RX_EQ_B3_C [15:0]	0000_1010_0101_0100	EQ Band 3 Coefficient C	

Register 058Bh DSP2 RX EQ Band 3 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1420 (058Ch) DSP2 RX EQ Band 3 PG	15:0	DSP2RX_EQ_B3_PG [15:0]	0000_0101_0101_1000	EQ Band 3 Coefficient PG	

Register 058Ch DSP2 RX EQ Band 3 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1421 (058Dh) DSP2 RX EQ Band 4 A	15:0	DSP2RX_EQ_B4_A [15:0]	0001_0110_1000_1110	EQ Band 4 Coefficient A	

Register 058Dh DSP2 RX EQ Band 4 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1422 (058Eh) DSP2 RX EQ Band 4 B	15:0	DSP2RX_EQ_B4_B [15:0]	1111_1000_0010_1001	EQ Band 4 Coefficient B	

Register 058Eh DSP2 RX EQ Band 4 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1423 (058Fh) DSP2 RX EQ Band 4 C	15:0	DSP2RX_EQ_B4_C [15:0]	0000_0111_1010_1101	EQ Band 4 Coefficient C	

Register 058Fh DSP2 RX EQ Band 4 C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1424 (0590h) DSP2 RX EQ Band 4 PG	15:0	DSP2RX_EQ_B4_PG [15:0]	0001_0001_0000_0011	EQ Band 4 Coefficient PG	

Register 0590h DSP2 RX EQ Band 4 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1425 (0591h) DSP2 RX EQ Band 5 A	15:0	DSP2RX_EQ_B5_A [15:0]	0000_0101_0110_0100	EQ Band 5 Coefficient A	

Register 0591h DSP2 RX EQ Band 5 A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1426 (0592h) DSP2 RX EQ Band 5 B	15:0	DSP2RX_EQ_B5_B [15:0]	0000_0101_0101_1001	EQ Band 5 Coefficient B	

Register 0592h DSP2 RX EQ Band 5 B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1427 (0593h) DSP2 RX EQ Band 5 PG	15:0	DSP2RX_EQ_B5_PG [15:0]	0100_0000_0000_0000	EQ Band 5 Coefficient PG	

Register 0593h DSP2 RX EQ Band 5 PG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1536 (0600h) DAC1 Mixer Volumes	9:5	ADCR_DAC1_VOL [4:0]	0_0000	Sidetone STR to DAC1L and DAC1R Volume 00000 = -36dB 00001 = -34.5dB 00010 = -33dB …. (1.5dB steps) 10111 = -1.5dB 11000 = 0dB	
	4:0	ADCL_DAC1_VOL [4:0]	0_0000	Sidetone STL to DAC1L and DAC1R Volume 00000 = -36dB 00001 = -34.5dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				00010 = -33dB …. (1.5dB steps) 10111 = -1.5dB 11000 = 0dB	

Register 0600h DAC1 Mixer Volumes

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1537 (0601h) DAC1 Left Mixer Routing	5	ADCR_TO_DAC 1L	0	Enable Sidetone STR to DAC1L 0 = Disabled 1 = Enabled	
	4	ADCL_TO_DAC 1L	0	Enable Sidetone STL to DAC1L 0 = Disabled 1 = Enabled	
	1	DSP2RXL_TO_ DAC1L	0	Enable DSP2 RX (Left) input to DAC1L 0 = Disabled 1 = Enabled	
	0	DSP1RXL_TO_ DAC1L	0	Enable DSP1 RX (Left) input to DAC1L 0 = Disabled 1 = Enabled	

Register 0601h DAC1 Left Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1538 (0602h) DAC1 Right Mixer Routing	5	ADCR_TO_DAC 1R	0	Enable Sidetone STR to DAC1R 0 = Disabled 1 = Enabled	
	4	ADCL_TO_DAC 1R	0	Enable Sidetone STL to DAC1R 0 = Disabled 1 = Enabled	
	1	DSP2RXR_TO_ DAC1R	0	Enable DSP2 RX (Right) input to DAC1R 0 = Disabled 1 = Enabled	
	0	DSP1RXR_TO_ DAC1R	0	Enable DSP1 RX (Right) input to DAC1R 0 = Disabled 1 = Enabled	

Register 0602h DAC1 Right Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1539 (0603h) DAC2 Mixer Volumes	9:5	ADCR_DAC2_V OL [4:0]	0_0000	Sidetone STR to DAC2L and DAC2R Volume 00000 = -36dB 00001 = -34.5dB 00010 = -33dB …. (1.5dB steps) 10111 = -1.5dB 11000 = 0dB	
	4:0	ADCL_DAC2_V OL [4:0]	0_0000	Sidetone STL to DAC2L and DAC2R Volume 00000 = -36dB 00001 = -34.5dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				00010 = -33dB …. (1.5dB steps) 10111 = -1.5dB 11000 = 0dB	

Register 0603h DAC2 Mixer Volumes

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1540 (0604h) DAC2 Left Mixer Routing	5	ADCR_TO_DAC 2L	0	Enable Sidetone STR to DAC2L 0 = Disabled 1 = Enabled	
	4	ADCL_TO_DAC 2L	0	Enable Sidetone STL to DAC2L 0 = Disabled 1 = Enabled	
	1	DSP2RXL_TO_ DAC2L	0	Enable DSP2 RX (Left) input to DAC2L 0 = Disabled 1 = Enabled	
	0	DSP1RXL_TO_ DAC2L	0	Enable DSP1 RX (Left) input to DAC2L 0 = Disabled 1 = Enabled	

Register 0604h DAC2 Left Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1541 (0605h) DAC2 Right Mixer Routing	5	ADCR_TO_DAC 2R	0	Enable Sidetone STR to DAC2R 0 = Disabled 1 = Enabled	
	4	ADCL_TO_DAC 2R	0	Enable Sidetone STL to DAC2R 0 = Disabled 1 = Enabled	
	1	DSP2RXR_TO_ DAC2R	0	Enable DSP2 RX (Right) input to DAC2R 0 = Disabled 1 = Enabled	
	0	DSP1RXR_TO_ DAC2R	0	Enable DSP1 RX (Right) input to DAC2R 0 = Disabled 1 = Enabled	

Register 0605h DAC2 Right Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1542 (0606h) DSP1 TX Left Mixer Routing	1	ADC1L_TO_DSP1TXL	0	Enable Input path 1L to DSP1 TX (Left) output 0 = Disabled 1 = Enabled Note that the ADC / DMIC input source is set by ADC_DMIC_SRC1.	
	0	DACL_TO_DSP1TXL	0	Enable DAC path (Left) to DSP1 TX (Left) output 0 = Disabled 1 = Enabled Note that the DAC input source is set by DAC_TO_DSPTX_SRC.	

Register 0606h DSP1 TX Left Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1543 (0607h) DSP1 TX Right Mixer Routing	1	ADC1R_TO_DSP1TXR	0	Enable Input path 1R to DSP1 TX (Right) output 0 = Disabled 1 = Enabled Note that the ADC / DMIC input source is set by ADC_DMIC_SRC1.	
	0	DACR_TO_DSP1TXR	0	Enable DAC path (Right) to DSP1 TX (Right) output 0 = Disabled 1 = Enabled Note that the DAC input source is set by DAC_TO_DSPTX_SRC.	

Register 0607h DSP1 TX Right Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1544 (0608h) DSP2 TX Left Mixer Routing	1	ADC2L_TO_DSP2TXL	0	Enable Input path 2L to DSP2 TX (Left) output 0 = Disabled 1 = Enabled Note that the ADC / DMIC input source is set by ADC_DMIC_SRC2.	
	0	DACL_TO_DSP2TXL	0	Enable DAC path (Left) to DSP2 TX (Left) output 0 = Disabled 1 = Enabled Note that the DAC input source is set by DAC_TO_DSPTX_SRC.	

Register 0608h DSP2 TX Left Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1545 (0609h) DSP2 TX Right Mixer Routing	1	ADC2R_TO_DSP2TXR	0	Enable Input path 2R to DSP2 TX (Right) output 0 = Disabled 1 = Enabled Note that the ADC / DMIC input source is set by ADC_DMIC_SRC2.	
	0	DACR_TO_DSP2TXR	0	Enable DAC path (Right) to DSP2 TX (Right) output 0 = Disabled 1 = Enabled Note that the DAC input source is set by DAC_TO_DSPTX_SRC.	

Register 0609h DSP2 TX Right Mixer Routing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1546 (060Ah) DSP TX Mixer Select	0	DAC_TO_DSPTX_SRC	0	DAC path select for DSP TX output 0 = DACL1 and DACR1 1 = DACL2 and DACR2	

Register 060Ah DSP TX Mixer Select

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1552 (0610h) DAC Softmute	1	DAC_SOFTMUTEMODE	0	DAC Unmute Ramp select 0 = Disabling soft-mute (DAC [1/2][L/R]_MUTE=0) will cause the DAC volume to change immediately to DAC [1/2][L/R]_VOL settings 1 = Disabling soft-mute (DAC [1/2][L/R]_MUTE=0) will cause the DAC volume to ramp up gradually to the DAC [1/2][L/R]_VOL settings	
	0	DAC_MUTERATE	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (maximum ramp time is 10.7ms) 1 = Slow ramp (maximum ramp time is 171ms)	

Register 0610h DAC Softmute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1568 (0620h) Oversampling	3	SPK_OSR128	1	Digital Speaker (SPDM) Oversample Rate Select 0 = 64fs 1 = 128fs	
	2	DMIC_OSR64	1	Digital Microphone (DMIC) Oversample Rate Select 0 = 32fs 1 = 64fs	
	1	ADC_OSR128	0	ADC Oversample Rate Select 0 = 64fs 1 = 128fs	
	0	DAC_OSR128	1	DAC Oversample Rate Select 0 = 64fs 1 = 128fs	

Register 0620h Oversampling

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1569 (0621h) Sidetone	12	ST_LPF	1	Digital Sidetone LPF Select (Cut-off frequency is 3.3kHz) 0 = Disabled 1 = Enabled	
	9:7	ST_HPF_CUT [2:0]	000	Sidetone HPF cut-off frequency 000 = 2.9kHz 001 = 1.5kHz 010 = 735Hz 011 = 403Hz 100 = 196Hz 101 = 98Hz 110 = 49Hz 111 = Reserved	
	6	ST_HPF	0	Digital Sidetone HPF Select 0 = Disabled 1 = Enabled	
	1	STR_SEL	0	Select source for sidetone STR path 0 = Input path 1R (set by ADC_DMIC_SRC1) 1 = Input path 2R (set by ADC_DMIC_SRC2)	
	0	STL_SEL	0	Select source for sidetone STL path 0 = Input path 1L (set by ADC_DMIC_SRC1) 1 = Input path 2L (set by ADC_DMIC_SRC2)	

Register 0621h Sidetone

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1792 (0700h) GPIO 1	15	GP1_DIR	1	GPIO1 Pin Direction 0 = Output 1 = Input	
	14	GP1_PU	0	GPIO1 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP1_PD	1	GPIO1 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP1_POL	0	GPIO1 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP1_OP_CFG	0	GPIO1 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP1_DB	1	GPIO1 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP1_LVL	0	GPIO1 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. For output functions only, when GP1_POL is set, the register contains the opposite logic level to the external pin.	
	3:0	GP1_FN [3:0]	0001	GPIO1 Pin Function 00h = ADCLRCLK1 01h = GPIO 02h = IRQ 03h = Microphone Detect	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				04h = Headphone Detect Complete 05h = DSP1 DRC Signal Detect 06h = DSP2 DRC Signal Detect 07h = FIFO Error 08h = Write Sequencer Status 09h = DCS_01 Done 0Ah = DCS_23 Done 0Bh = FLL Clock Switch 0Ch = FLL Lock 0Dh = OPCLK Clock output 0Eh = FLL Clock output 0Fh to 1Fh = Reserved	

Register 0700h GPIO 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1793 (0701h) GPIO 2	15	GP2_DIR	1	GPIO2 Pin Direction 0 = Output 1 = Input	
	14	GP2_PU	0	GPIO2 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP2_PD	1	GPIO2 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP2_POL	0	GPIO2 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP2_OP_CFG	0	GPIO2 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP2_DB	1	GPIO2 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP2_LVL	0	GPIO2 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. For output functions only, when GP2_POL is set, the register contains the opposite logic level to the external pin.	
	3:0	GP2_FN [3:0]	0001	GPIO2 Pin Function 00h = ADCLRCLK2 01h = GPIO 02h = IRQ 03h = Microphone Detect 04h = Headphone Detect Complete 05h = DSP1 DRC Signal Detect 06h = DSP2 DRC Signal Detect 07h = FIFO Error 08h = Write Sequencer Status 09h = DCS_01 Done 0Ah = DCS_23 Done 0Bh = FLL Clock Switch 0Ch = FLL Lock 0Dh = OPCLK Clock output	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0Eh = FLL Clock output 0Fh to 1Fh = Reserved	

Register 0701h GPIO 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1794 (0702h) GPIO 3	15	GP3_DIR	1	GPIO3 Pin Direction 0 = Output 1 = Input	
	14	GP3_PU	0	GPIO3 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP3_PD	1	GPIO3 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP3_POL	0	GPIO3 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP3_OP_CFG	0	GPIO3 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP3_DB	1	GPIO3 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP3_LVL	0	GPIO3 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. For output functions only, when GP3_POL is set, the register contains the opposite logic level to the external pin.	
	3:0	GP3_FN [3:0]	0001	GPIO3 Pin Function 00h = n/a 01h = GPIO 02h = IRQ 03h = Microphone Detect 04h = Headphone Detect Complete 05h = DSP1 DRC Signal Detect 06h = DSP2 DRC Signal Detect 07h = FIFO Error 08h = Write Sequencer Status 09h = DCS_01 Done 0Ah = DCS_23 Done 0Bh = FLL Clock Switch 0Ch = FLL Lock 0Dh = OPCLK Clock output 0Eh = FLL Clock output 0Fh to 1Fh = Reserved	

Register 0702h GPIO 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1795 (0703h)	15	GP4_DIR	1	GPIO4 Pin Direction 0 = Output	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
GPIO 4				1 = Input	
	14	GP4_PU	0	GPIO4 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP4_PD	1	GPIO4 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP4_POL	0	GPIO4 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	
	9	GP4_OP_CFG	0	GPIO4 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP4_DB	1	GPIO4 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP4_LVL	0	GPIO4 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. For output functions only, when GP4_POL is set, the register contains the opposite logic level to the external pin.	
	3:0	GP4_FN [3:0]	0001	GPIO4 Pin Function 00h = n/a 01h = GPIO 02h = IRQ 03h = Microphone Detect 04h = Headphone Detect Complete 05h = DSP1 DRC Signal Detect 06h = DSP2 DRC Signal Detect 07h = FIFO Error 08h = Write Sequencer Status 09h = DCS_01 Done 0Ah = DCS_23 Done 0Bh = FLL Clock Switch 0Ch = FLL Lock 0Dh = OPCLK Clock output 0Eh = FLL Clock output 0Fh to 1Fh = Reserved	

Register 0703h GPIO 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1796 (0704h) GPIO 5	15	GP5_DIR	1	GPIO5 Pin Direction 0 = Output 1 = Input	
	14	GP5_PU	0	GPIO5 Pull-Up Enable 0 = Disabled 1 = Enabled	
	13	GP5_PD	1	GPIO5 Pull-Down Enable 0 = Disabled 1 = Enabled	
	10	GP5_POL	0	GPIO5 Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	9	GP5_OP_CFG	0	GPIO5 Output Configuration 0 = CMOS 1 = Open Drain	
	8	GP5_DB	1	GPIO5 Input De-bounce 0 = Disabled 1 = Enabled	
	6	GP5_LVL	0	GPIO5 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. For output functions only, when GP5_POL is set, the register contains the opposite logic level to the external pin.	
	3:0	GP5_FN [3:0]	0001	GPIO5 Pin Function 00h = n/a 01h = GPIO 02h = IRQ 03h = Microphone Detect 04h = Headphone Detect Complete 05h = DSP1 DRC Signal Detect 06h = DSP2 DRC Signal Detect 07h = FIFO Error 08h = Write Sequencer Status 09h = DCS_01 Done 0Ah = DCS_23 Done 0Bh = FLL Clock Switch 0Ch = FLL Lock 0Dh = OPCLK Clock output 0Eh = FLL Clock output 0Fh to 1Fh = Reserved	

Register 0704h GPIO 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1824 (0720h) Pull Control (1)	12	DMICDAT2_PD	0	DMICDAT2 Pull-Down enable 0 = Disabled 1 = Enabled	
	10	DMICDAT1_PD	0	DMICDAT1 Pull-Down enable 0 = Disabled 1 = Enabled	
	9	MCLK2_PU	0	MCLK2 Pull-up enable 0 = Disabled 1 = Enabled	
	8	MCLK2_PD	0	MCLK2 Pull-down enable 0 = Disabled 1 = Enabled	
	7	MCLK1_PU	0	MCLK1 Pull-up enable 0 = Disabled 1 = Enabled	
	6	MCLK1_PD	0	MCLK1 Pull-down resstor enable 0 = Disabled 1 = Enabled	
	5	DACDAT1_PU	0	DACDAT1 Pull-up enable 0 = Disabled 1 = Enabled	
	4	DACDAT1_PD	0	DACDAT1 Pull-down enable	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0 = Disabled 1 = Enabled	
	3	DACLRCLK1_PU	0	DACLRCLK1 Pull-up enable 0 = Disabled 1 = Enabled	
	2	DACLRCLK1_PD	0	DACLRCLK1 Pull-down enable 0 = Disabled 1 = Enabled	
	1	BCLK1_PU	0	BCLK1 Pull-up enable 0 = Disabled 1 = Enabled	
	0	BCLK1_PD	0	BCLK1 Pull-down enable 0 = Disabled 1 = Enabled	

Register 0720h Pull Control (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1825 (0721h) Pull Control (2)	8	LDO1ENA_PD	1	LDO1ENA Pull-down enable 0 = Disabled 1 = Enabled	
	6	ADDR_PD	1	ADDR Pull-down enable 0 = Disabled 1 = Enabled	
	5	DACDAT2_PU	0	DACDAT2 Pull-up enable 0 = Disabled 1 = Enabled	
	4	DACDAT2_PD	0	DACDAT2 Pull-down enable 0 = Disabled 1 = Enabled	
	3	DACLRCLK2_PU	0	DACLRCLK2 Pull-up enable 0 = Disabled 1 = Enabled	
	2	DACLRCLK2_PD	0	DACLRCLK2 Pull-down enable 0 = Disabled 1 = Enabled	
	1	BCLK2_PU	0	BCLK2 Pull-up enable 0 = Disabled 1 = Enabled	
	0	BCLK2_PD	0	BCLK2 Pull-down enable 0 = Disabled 1 = Enabled	

Register 0721h Pull Control (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1840 (0730h) Interrupt Status 1	4	GP5_EINT	0	GPIO5 Interrupt status (Rising and falling edge triggered) Note: Cleared when a '1' is written.	
	3	GP4_EINT	0	GPIO4 Interrupt status (Rising and falling edge triggered)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Note: Cleared when a ‘1’ is written.	
	2	GP3_EINT	0	GPIO3 Interrupt status (Rising and falling edge triggered) Note: Cleared when a ‘1’ is written.	
	1	GP2_EINT	0	GPIO2 Interrupt status (Rising and falling edge triggered) Note: Cleared when a ‘1’ is written.	
	0	GP1_EINT	0	GPIO1 Interrupt status (Rising and falling edge triggered) Note: Cleared when a ‘1’ is written.	

Register 0730h Interrupt Status 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1841 (0731h) Interrupt Status 2	12	DCS_DONE_23_EINT	0	DC Servo Channels 2,3 IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.	
	11	DCS_DONE_01_EINT	0	DC Servo Channels 0,1 IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.	
	10	WSEQ_DONE_EINT	0	Write Sequencer IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.	
	9	FIFOS_ERR_EINT	0	Digital Core FIFO Error IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.	
	7	DSP2DRC_SIG_DET_EINT	0	DSP2 DRC Signal Detect IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.	
	6	DSP1DRC_SIG_DET_EINT	0	DSP1 DRC Signal Detect IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.	
	3	FLL_SW_CLK_DONE_EINT	0	FLL Clock Switch IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.	
	2	FLL_LOCK_EINT	0	FLL Lock IRQ status (Rising and falling edge triggered) Note: Cleared when a ‘1’ is written.	
	1	HP_DONE_EINT	0	Headphone Detection IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.	
	0	MICD_EINT	0	Microphone Detection IRQ status (Rising edge triggered) Note: Cleared when a ‘1’ is written.	

Register 0731h Interrupt Status 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1842 (0732h) Interrupt Raw	12	DCS_DONE_23_STS	0	DC Servo Channels 2,3 (HPOUT2L and HPOUT2R) status 0 = DC Servo not complete 1 = DC Servo complete	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
Status 2	11	DCS_DONE_01_STS	0	DC Servo Channels 0,1 (HPOUT1L and HPOUT1R) status 0 = DC Servo not complete 1 = DC Servo complete	
	10	WSEQ_DONE_STS	0	Write Sequencer status 0 = Sequencer Busy (sequence in progress) 1 = Sequencer Idle	
	9	FIFOS_ERR_STS	0	Digital Core FIFO Error status 0 = Normal 1 = FIFO Error	
	7	DSP2DRC_SIG_DET_STS	0	DSP2 DRC Signal Detect status 0 = Normal 1 = Activity Detected	
	6	DSP1DRC_SIG_DET_STS	0	DSP1 DRC Signal Detect status 0 = Normal 1 = Activity Detected	
	2	FLL_LOCK_STS	0	FLL Lock status 0 = Not locked 1 = Locked	

Register 0732h Interrupt Raw Status 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1848 (0738h) Interrupt Status 1 Mask	4	IM_GP5_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_GP4_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_GP3_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_GP2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_GP1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 0738h Interrupt Status 1 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1849 (0739h) Interrupt Status 2 Mask	12	IM_DCS_DONE_23_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	11	IM_DCS_DONE	1	Interrupt mask.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
		_01_EINT		0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	10	IM_WSEQ_DONE_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	9	IM_FIFOS_ERR_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	7	IM_DSP2DRC_SIG_DET_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	6	IM_DSP1DRC_SIG_DET_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_FLL_SW_CLK_DONE_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_FLL_LOCK_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_HP_DONE_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_MICD_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 0739h Interrupt Status 2 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1856 (0740h) Interrupt Control	0	IM_IRQ	0	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 0740h Interrupt Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2048 (0800h) Left PDM Speaker	4	SPKL_ENA	0	PDM Speaker Output (Left) Enable 0 = Disabled 1 = Enabled	
	3	SPKL_MUTE	0	PDM Speaker Output (Left) Mute	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0 = Audio output 1 = Mute Sequence output	
	2	SPKL_MUTE_ZC	0	PDM Speaker Output (Left) Zero Cross 0 = Disabled 1 = Enabled	
	1:0	SPKL_SRC [1:0]	00	PDM Speaker Output (Left) Source 00 = DAC1L 01 = DAC1R 10 = DAC2L 11 = DAC2R	

Register 0800h Left PDM Speaker

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2049 (0801h) Right PDM Speaker	4	SPKR_ENA	0	PDM Speaker Output (Right) Enable 0 = Disabled 1 = Enabled	
	3	SPKR_MUTE	0	PDM Speaker Output (Right) Mute 0 = Audio output 1 = Mute Sequence output	
	2	SPKR_MUTE_ZC	0	PDM Speaker Output (Right) Zero Cross 0 = Disabled 1 = Enabled	
	1:0	SPKR_SRC [1:0]	01	PDM Speaker Output (Right) Source 00 = DAC1L 01 = DAC1R 10 = DAC2L 11 = DAC2R	

Register 0801h Right PDM Speaker

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2050 (0802h) PDM Speaker Mute Sequence	8	SPK_MUTE_ENDIAN	0	PDM Speaker Output Mute Sequence Control 0 = Mute sequence is LSB first 1 = Mute sequence output is MSB first	
	7:0	SPK_MUTE_SEQ1 [7:0]	0110_1001	PDM Speaker Output Mute Sequence Defines the 8 bit code that is output on SPKDAT (left) or SPKDAT (right) when muted.	

Register 0802h PDM Speaker Mute Sequence

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2051 (0803h) PDM Speaker Volume	15	SPK_FMT	0	PDM Speakout Output timing format 0 = Mode A (PDM data is valid at the rising/falling edges of SPKCLK) 1 = Mode B (PDM data is valid during the high/low phase of SPKCLK)	
	7:4	SPKR_VOL [3:0]	0110	PDM Speaker Output (Right) Digital Volume Control -9dB to +3dB in 1.5dB steps	
	3:0	SPKL_VOL [3:0]	0110	PDM Speaker Output (Left) Digital Volume Control	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				-9dB to +3dB in 1.5dB steps	

Register 0803h PDM Speaker Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R12288 (3000h) Write Sequencer 0	13:0	WSEQ_ADDR0 [13:0]	00_0000_0000_0001	Control Register Address to be written to in this sequence step.	

Register 3000h Write Sequencer 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R12289 (3001h) Write Sequencer 1	7:0	WSEQ_DATA0 [7:0]	0000_0001	Data to be written in this sequence step. When the data width is less than 8 bits, then one or more of the MSBs of WSEQ_DATA0 are ignored. It is recommended that unused bits be set to 0.	

Register 3001h Write Sequencer 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R12290 (3002h) Write Sequencer 2	10:8	WSEQ_DATA_WIDTH0 [2:0]	000	Width of the data block written in this sequence step. 000 = 1 bit 001 = 2 bits 010 = 3 bits 011 = 4 bits 100 = 5 bits 101 = 6 bits 110 = 7 bits 111 = 8 bits	
	3:0	WSEQ_DATA_START0 [3:0]	0000	Bit position of the LSB of the data block written in this sequence step. 0000 = Bit 0 … 1111 = Bit 15	

Register 3002h Write Sequencer 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R12291 (3003h) Write Sequencer 3	8	WSEQ_EOS0	0	End of Sequence flag. This bit indicates whether the Control Write Sequencer should stop after executing this step. 0 = Not end of sequence 1 = End of sequence (Stop the sequencer after this step).	
	3:0	WSEQ_DELAY0 [3:0]	0110	Time delay after executing this step. Total time per step (including execution) = 62.5µs × (2^{WSEQ_DELAY} + 8)	

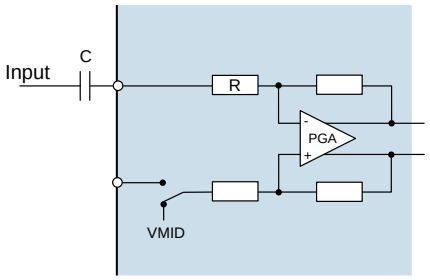
Register 3003h Write Sequencer 3

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

ANALOGUE INPUT PATHS

The WM8915 provides 2 analogue audio input paths. Each of the analogue input pins is referenced to the internal DC reference, VREF. A DC blocking capacitor is required for each analogue input pin used in the target application. The choice of capacitor is determined by the filter that is formed between that capacitor and the impedance of the input pin. The circuit is illustrated in Figure 56.



$$Fc = \frac{1}{2\pi RC}$$

Fc = high pass 3dB cut-off frequency

Figure 56 Audio Input Path DC Blocking Capacitor

Note that the WM8915 input impedance is not fixed in all applications, but varies according to the input configuration and gain settings, as described in “Electrical Characteristics”. A 1µF capacitance for all input connections will give good results in most cases. Tantalum electrolytic capacitors are particularly suitable as they offer high stability in a small package size.

Ceramic equivalents are a cost effective alternative to the superior tantalum packages, but care must be taken to ensure the desired capacitance is maintained at the AVDD operating voltage. Also, ceramic capacitors may show microphonic effects, where vibrations and mechanical conditions give rise to electrical signals. This is particularly problematic for microphone input paths where a large signal gain is required.

A single capacitor is required for a single-ended line or microphone input connection. For a differential input connection, a DC blocking capacitor is required on both input pins.

The external connections for single-ended and differential microphones, incorporating the WM8915 microphone bias circuit, are shown later in the “Microphone Bias Circuit” section - see Figure 57.

DIGITAL MICROPHONE INPUT PATHS

The WM8915 provides up to 4 digital microphone input paths; two channels of audio data can be multiplexed on each of the DMICDATn pins. Each of these stereo pairs is clocked using the respective DMICCLKn pin.

The external connections for digital microphones, incorporating the WM8915 microphone bias circuit, are shown later in the “Microphone Bias Circuit” section - see Figure 58.

Ceramic decoupling capacitors for the digital microphones may be required - refer to the specific recommendations for the application microphone(s).

When two microphones are connected to a single DMICDAT pin, the microphones must be configured to ensure that the Left mic transmits a data bit when DMICCLK is high, and the Right mic transmits a data bit when DMICCLK is low. The WM8915 samples the digital microphone data at the end of each DMICCLK phase. Each microphone must tri-state its data output when the other microphone is transmitting. Integrated pull-down resistors can be enabled on the DMICDAT pins if required.

The digital microphone interface is referenced to the MICBIAS1 voltage domain; the MICBIAS1 output must be enabled (MICB1_ENA = 1) when using the digital microphone interface.

MICROPHONE BIAS CIRCUIT

The WM8915 is designed to interface easily with up to four analogue microphones. These may be connected in single-ended or differential configurations, as illustrated in Figure 57. The single-ended method allows greater capability for the connection of multiple audio sources simultaneously, whilst the differential method provides better performance due to its rejection of common-mode noise.

In either configuration, the analogue microphone requires a bias current (electret condenser microphones) or voltage supply (silicon microphones), which can be provided by MICBIAS1 or MICBIAS2.

A current-limiting resistor is required when using an electret condenser microphone (ECM). The resistance should be chosen according to the minimum operating impedance of the microphone and MICBIAS voltage so that the maximum bias current of the WM8915 is not exceeded. Cirrus recommends a 2.2kΩ current limiting resistor as it provides compatibility with a wide range of microphone models.

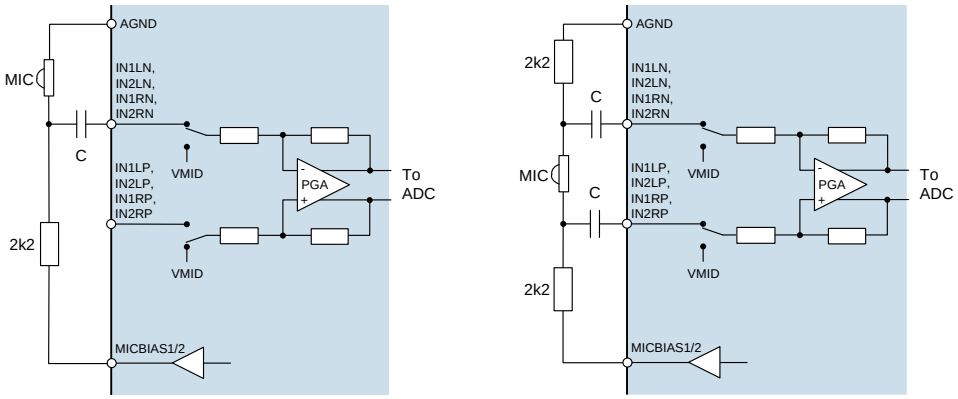


Figure 57 Single-Ended and Differential Analogue Microphone Connections

The WM8915 also supports up to four digital microphone inputs. The MICBIAS1 generator is suitable for use as a low noise supply for digital microphones, as shown in Figure 58.

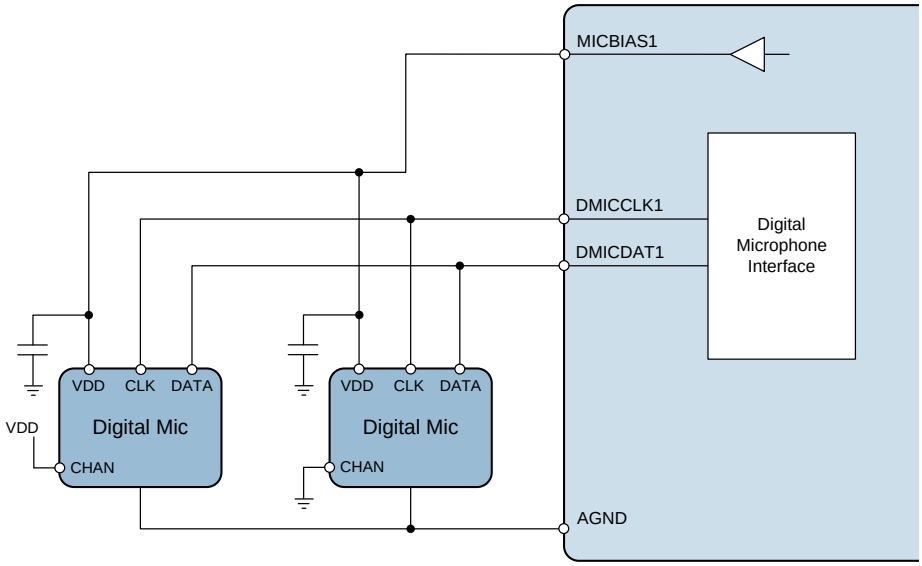


Figure 58 Digital Microphone Connection

The MICBIAS generators can each operate as a voltage regulator or in bypass mode. See “Analogue Input Signal Path” for details of the MICBIAS generators.

In Regulator mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. It is important that parasitic capacitances on the MICBIAS1 or MICBIAS2 pins do not exceed 50pF in Regulator mode.

If the capacitive load on MICBIAS1 or MICBIAS2 exceeds 50pF (eg. due to a decoupling capacitor or long PCB trace), then the respective generator must be configured in Bypass mode.

The maximum output current is noted in the “Electrical Characteristics”. This limit must be observed on each MICBIAS output, especially if more than one microphone is connected to a single MICBIAS pin. Note that the maximum output current differs between Regulator mode and Bypass mode. The MICBIAS output voltage can be adjusted using register control in Regulator mode.

HEADPHONE DRIVER OUTPUT PATH

The WM8915 provides 2 stereo headphone output drivers. These outputs are all ground-referenced, allowing direct connection to the external load(s). There is no requirement for DC blocking capacitors.

For best audio performance, it is recommended to connect a zobel network to the headphone output pins. The zobel network should comprise of a 20Ω resistor and 100nF capacitor in series with each other, as illustrated in Figure 59.

The zobel network components have the effect of dampening high frequency oscillations or instabilities that can arise outside the audio band under certain conditions. Possible sources of these instabilities include the inductive load of a headphone coil or an active load in the form of an external line amplifier.

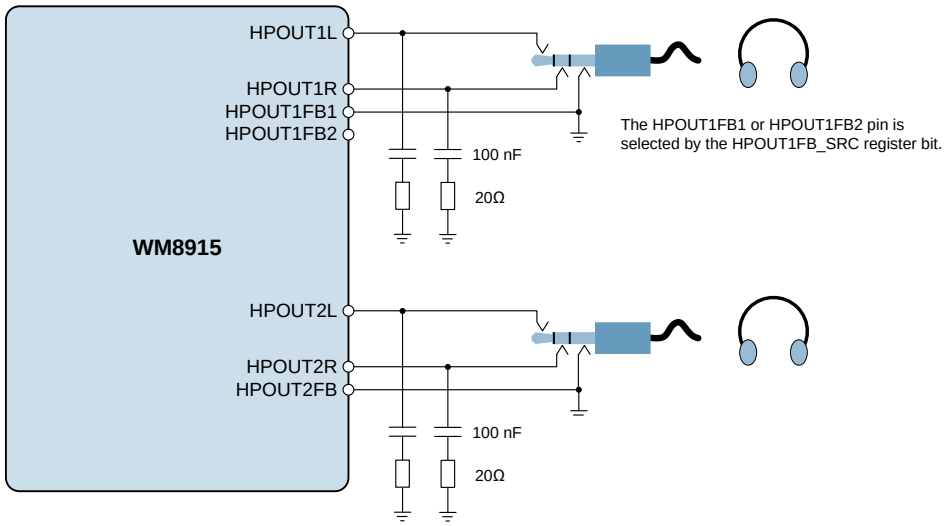


Figure 59 Headphone Connection

POWER SUPPLY / REFERENCE DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations (or 'spikes') in the power supply voltage can cause malfunctions and unintentional behavior in other components. A decoupling (or 'bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the WM8915, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling (or 'bypass') capacitor can be used to filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

The recommended power supply and voltage reference decoupling capacitors for WM8915 are listed below in Table 94.

POWER SUPPLY	DECOUPLING CAPACITOR
DBVDD, AVDD1, AVDD2	0.1µF ceramic (see Note)
DCVDD	Required capacitance is 0.5µF. Suitable component typically 1.0µF.
CPVDD	Required capacitance is 2.0µF. Suitable component typically 4.7µF.
MICVDD	Required capacitance is 1.1µF. Suitable component typically 4.7µF.
VREFC	Required capacitance is 0.5µF. Suitable component typically 1.0µF.

Table 94 Power Supply Decoupling Capacitors

Note: 0.1µF is required close to each pin, with 4.7µF a guide to the total required power rail capacitance, including that at the regulator output.

All decoupling capacitors should be placed as close as possible to the WM8915 device. The connection between AGND, the AVDD1 decoupling capacitor and the main system ground should be made at a single point as close as possible to the AGND ball of the WM8915.

The VREFC capacitor is not, technically, a decoupling capacitor. However, it does serve a similar purpose in filtering noise on the bandgap reference. The connection between AGND, the VREFC decoupling capacitor and the main system ground should be made at a single point as close as possible to the AGND ball of the WM8915.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most applications, the use of ceramic capacitors with capacitor dielectric X5R is recommended.

CHARGE PUMP COMPONENTS

The WM8915 incorporates a Charge Pump circuit, which generates the CPVOUTP and CPVOUTN supply rails for the ground-referenced headphone drivers.

Decoupling capacitors are required on each of the Charge Pump outputs. A fly-back capacitor is also required. The recommended Charge Pump capacitors for WM8915 are detailed below in Table 95.

DESCRIPTION	CAPACITOR
CPVOUTP decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CPVOUTN decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CP fly-back (connect between CPCA and CPCB)	Required capacitance is 1.0µF at 2V. Suitable component typically 2.2µF.

Table 95 Charge Pump External Capacitors

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most applications, the use of ceramic capacitors with capacitor dielectric X5R is recommended.

The positioning of the Charge Pump capacitors is important, particularly the fly-back capacitor. These capacitors should be placed as close as possible to the WM8915.

EXTERNAL ACCESSORY DETECTION COMPONENTS

The accessory detection circuit measures the impedance of an external load connected to one of the MICDET pins.

Under default conditions, this function uses the MICBIAS2 output as a reference, as shown in Figure 60. Note that the WM8915 will automatically enable MICBIAS2 when required in order to perform the detection function. It is also possible to select MICBIAS1 as the reference, using the MICD_BIAS_SRC register.

The WM8915 can detect the presence of a typical microphone and up to 7 push-buttons, using the components shown. When the microphone detection circuit is enabled, then each of the push-buttons shown will cause a different bit within the MICD_LVL register to be set.

The microphone detect function is specifically designed to detect a video accessory (typical 75Ω) load if required. A measured external impedance of 75Ω will cause the MICD_LVL [4] bit to be set.

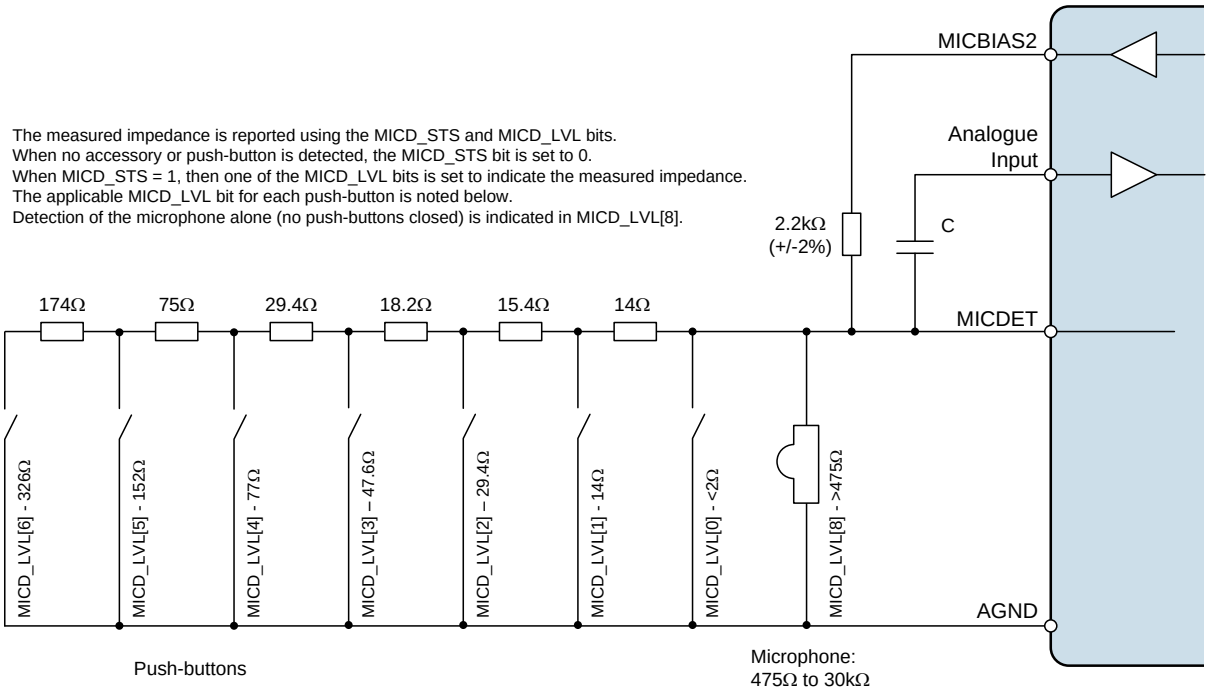


Figure 60 External Accessory Detect Connection

RECOMMENDED EXTERNAL COMPONENTS DIAGRAM

Figure 61 below provide a summary of recommended external components for WM8915. Note that these diagrams do not include any components that are specific to the end application e.g. they do not include RF decoupling, or RF filtering for external connections.

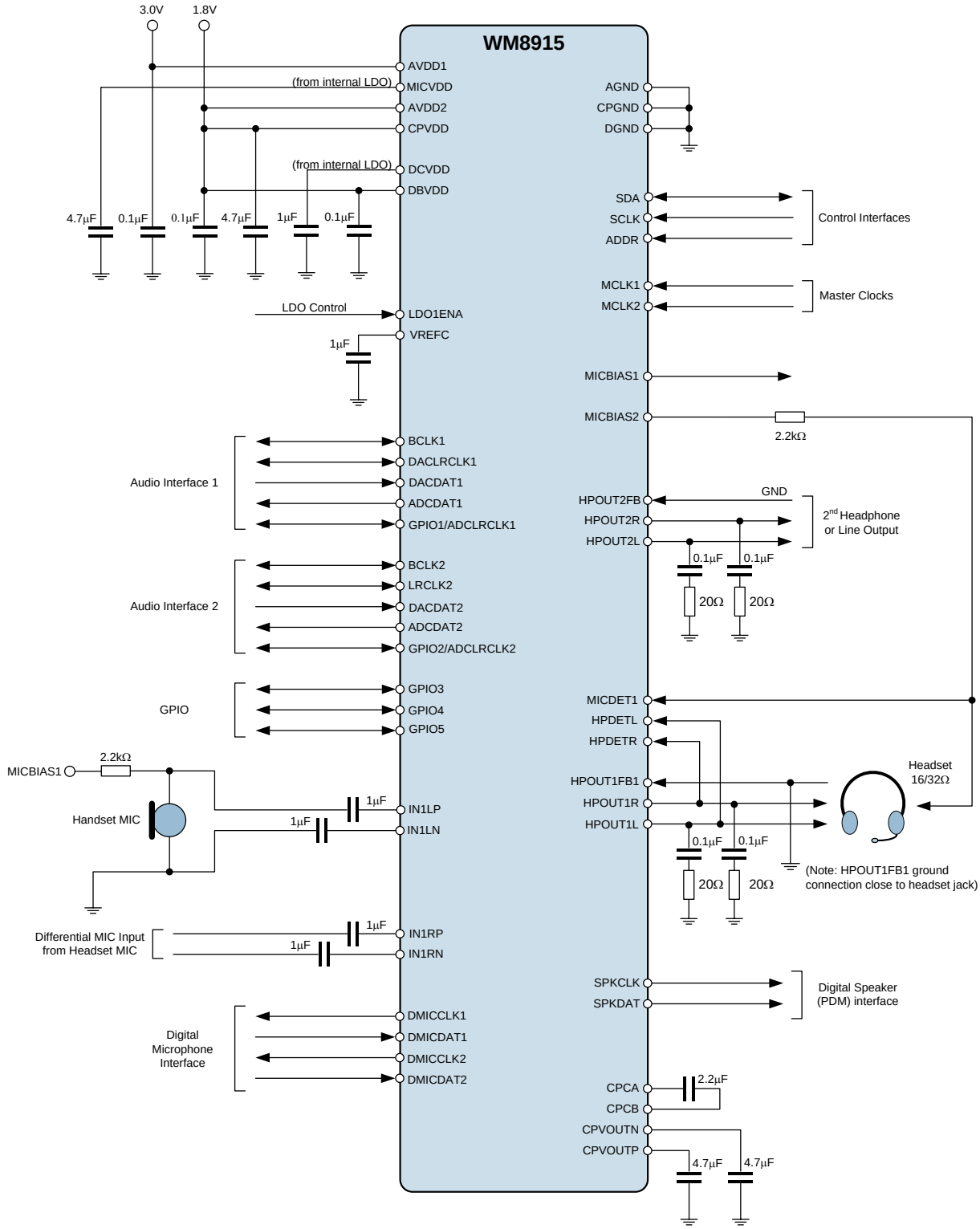


Figure 61 Recommended External Components Diagram

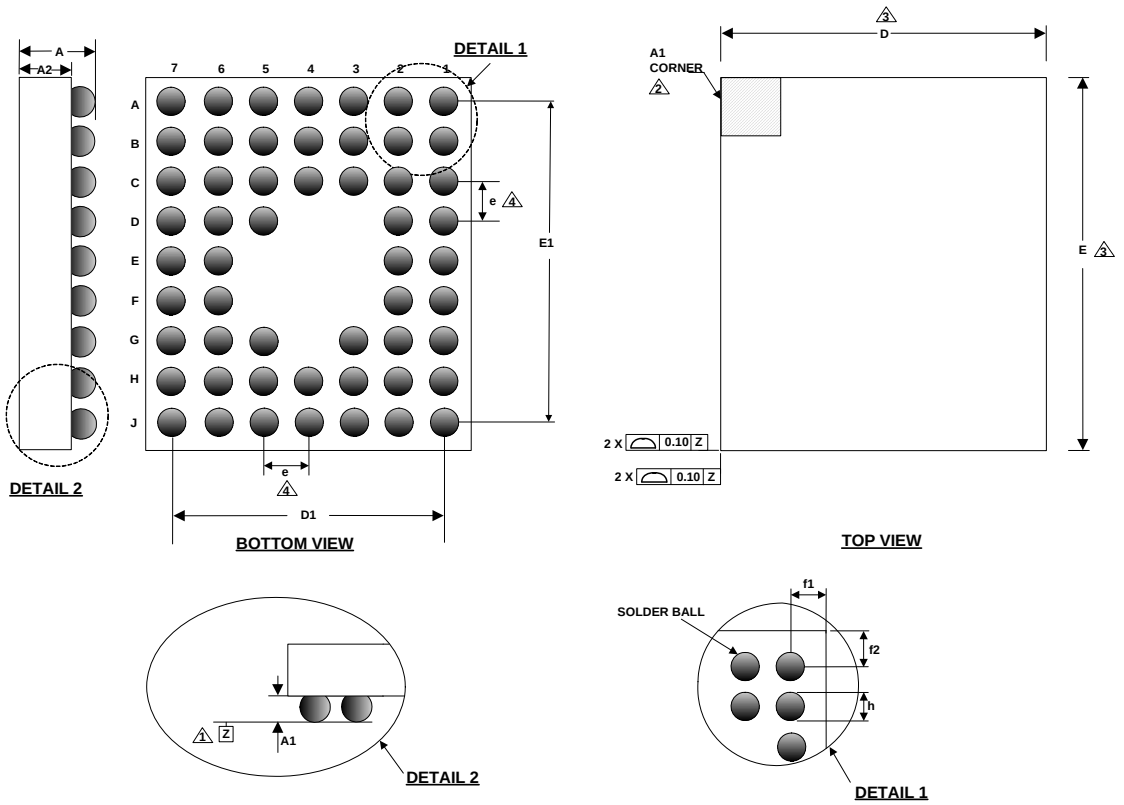
PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the WM8915 device as possible, with current loop areas kept as small as possible.

PACKAGE DIMENSIONS

PACKAGE DIAGRAM FOR DEVICES MARKED SJR

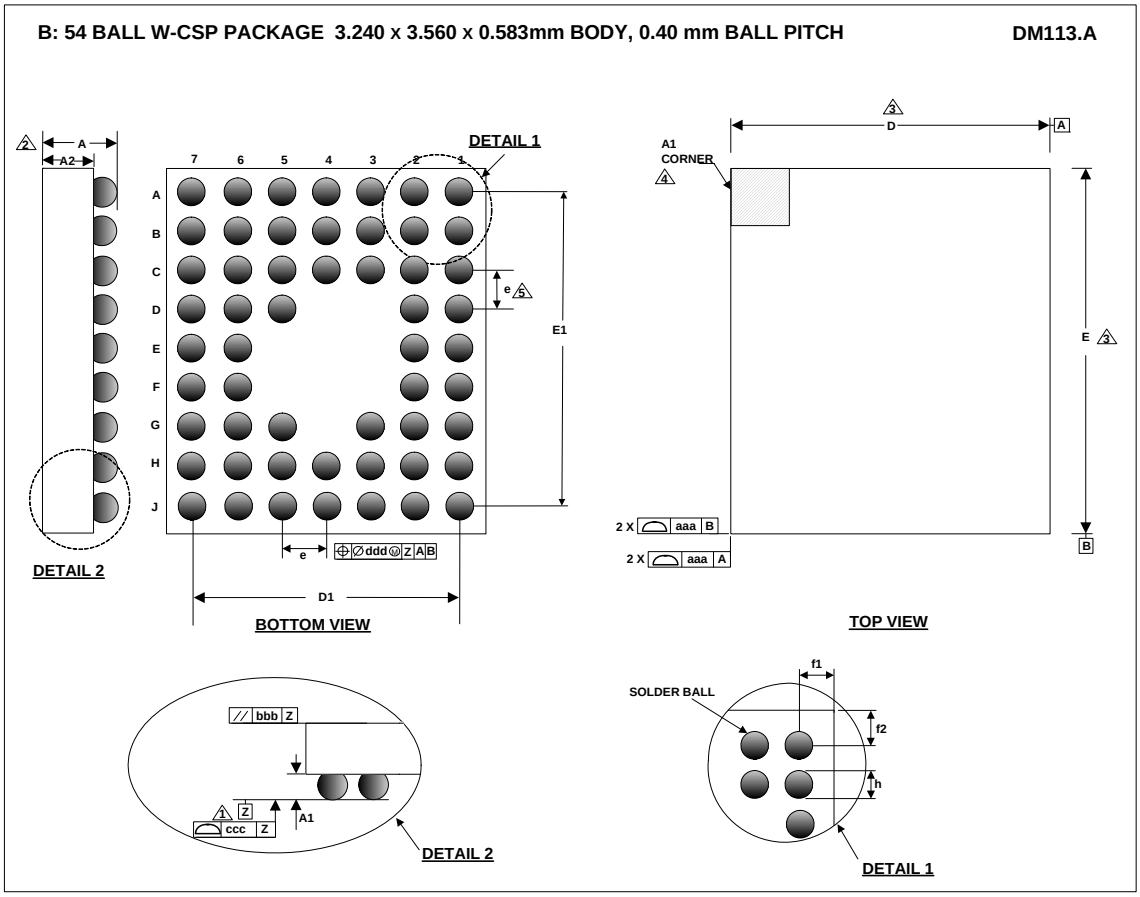
B: 54 BALL W-CSP PACKAGE 3.240 x 3.560 x 0.581mm BODY, 0.40 mm BALL PITCH **DM093.B**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.531	0.581	0.634	
A1	0.175	0.200	0.228	
A2	0.356	0.381	0.406	
D	3.210	3.240	3.270	
D1		2.400 BSC		
E	3.530	3.560	3.590	
E1		3.200 BSC		
e		0.400 BSC		4
f1	0.405			Bump centre to die edge
f2	0.165			Bump centre to die edge
h	0.221	0.260	0.299	

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
3. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
4. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
5. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
6. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

PACKAGE DIAGRAM FOR DEVICES MARKED 2RN



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.543	0.583	0.623	
A1	0.163	0.202	0.241	
A2	0.365	0.381	0.397	
D	3.215	3.240	3.265	
D1		2.400 BSC		
E	3.535	3.560	3.585	
E1		3.200 BSC		
e		0.400 BSC		4
f1	0.408			Bump centre to die edge
f2	0.168			Bump centre to die edge
h	0.222	0.262	0.302	
aaa		0.025		
bbb		0.060		
ccc		0.030		
ddd		0.015		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

IMPORTANT NOTICE

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.

REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
16/12/10	3.0	Noted that DRC Anti-Clip and Quick Release features should not be used at the same time. Added power domain information in 'Pin Description' section.		PH
09/02/11	3.0	Restriction on MICBIAS capacitance clarified - 50pF limit is only applicable in Normal (regulator) mode.		PH
16/02/11	3.0	Corrected package height reference on front page		JMacD
19/05/11	4.0	LDO & MICBIAS modes clarified as "Regulator" mode and "Bypass" mode. Input PGA & HPOUT1 volume detail added. Updates to clarify the position of the DRC, HPF, AIF Volumes in the respective signal paths. Clarification to clocking schematic and SYSDSPCLK_ENA register.		PH
19/05/11	4.0	Package Drawing updated - increased A and A1 to accommodate FCI drawing. External Accessory Detect description & characteristics updated; Recommended External Components added in Applications Information section.		PH
28/06/11	4.0	Min/max limits added in Electrical Characteristics. Timing requirement added for Bandgap enable.		PH
02/08/11	4.1	Update to LDO Block Diagram, confirming that DBVDD and AVDD1 are input pins only. Clarification to the HPOUTnFB functions, noting these are ground feedback connections, not the primary return path connections. Separate MICDETn pins shown on Accessory detect circuit.		PH
05/03/12	4.1	R1025 (0403h) corrected to R1025 (0401h)	58	PH
18/06/12	4.2	Package Diagram changed to DM113.A	256	JMacD
18/06/12	4.2	Reel quantity changed to 5,000	7	JMacD
27/08/12	4.3	Both Package Diagrams DM093A and DM113.A shown on datasheet.	257	JMacD
17/11/14	4.4	Updates noting support for 44.1kHz-related audio sample rates. Noted AIF format is 2's complement. Noted LJ / DSP-B modes are supported in Master mode only. Full scale ADC input level descriptions amended.	Various 107 107-125 11	PH