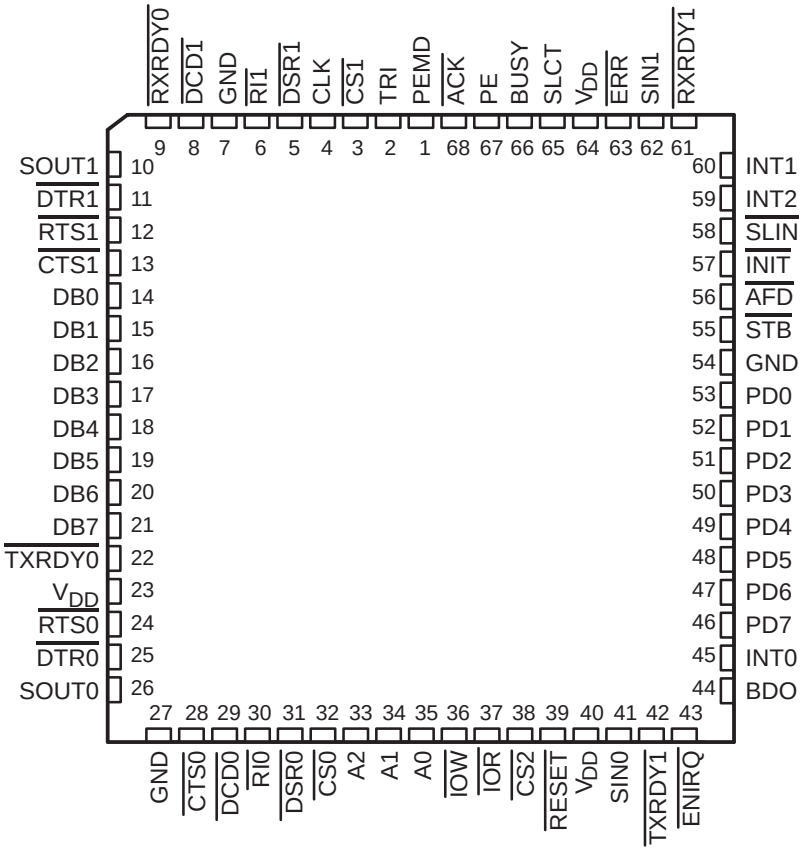
- **IBM PC/AT™ Compatible**
- **Two TL16C550 ACEs**
- **Enhanced Bidirectional Printer Port**
- **16-Byte FIFOs Reduce CPU Interrupts**
- **Up to 16-MHz Clock Rate for up to 1-Mbaud Operation**
- **Transmit, Receive, Line Status, and Data Set Interrupts on Each Channel Independently Controlled**
- **Individual Modem Control Signals for Each Channel**
- **Programmable Serial Interface Characteristics for Each Channel:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even, Odd, or No Parity Bit Generation and Detection**
  - **1-, 1-1/2-, or 2-Stop Bit Generation**
- **3-State Outputs Provide TTL Drive for the Data and Control Bus on Each Channel**
- **Hardware and Software Compatible With TL16C452**

HV or FN PACKAGE
(TOP VIEW)



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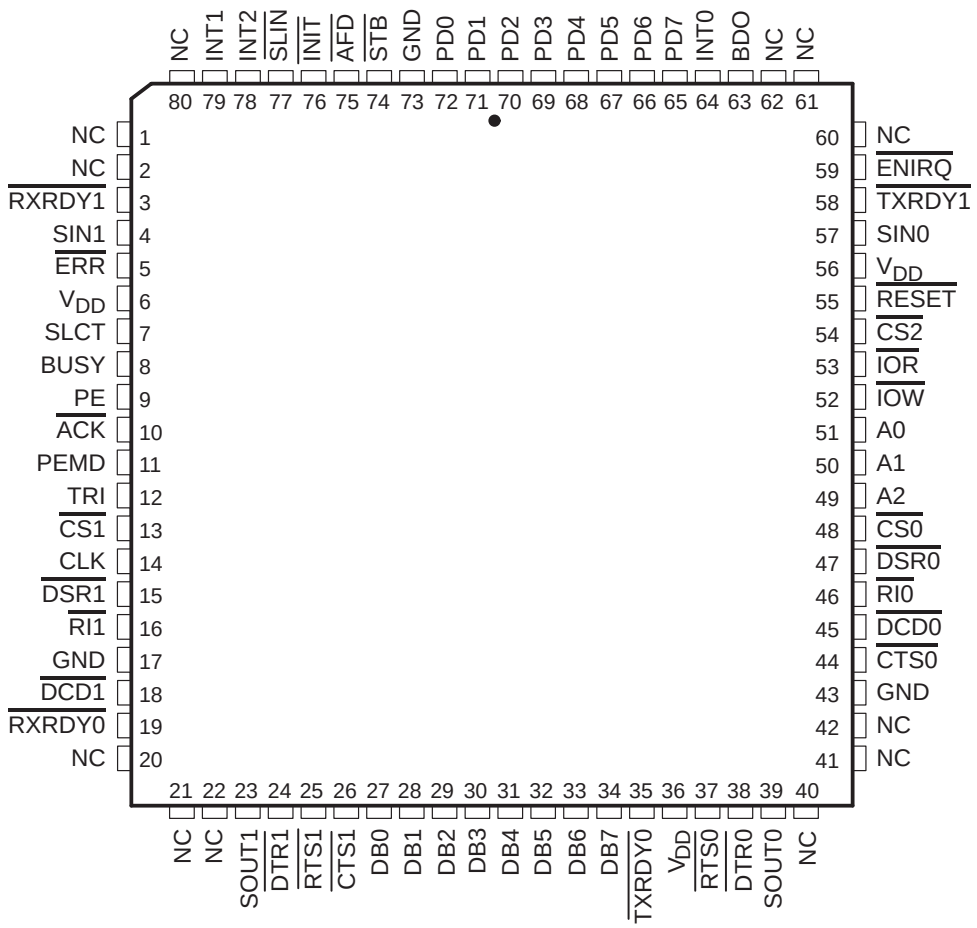
PN PACKAGE
(TOP VIEW)



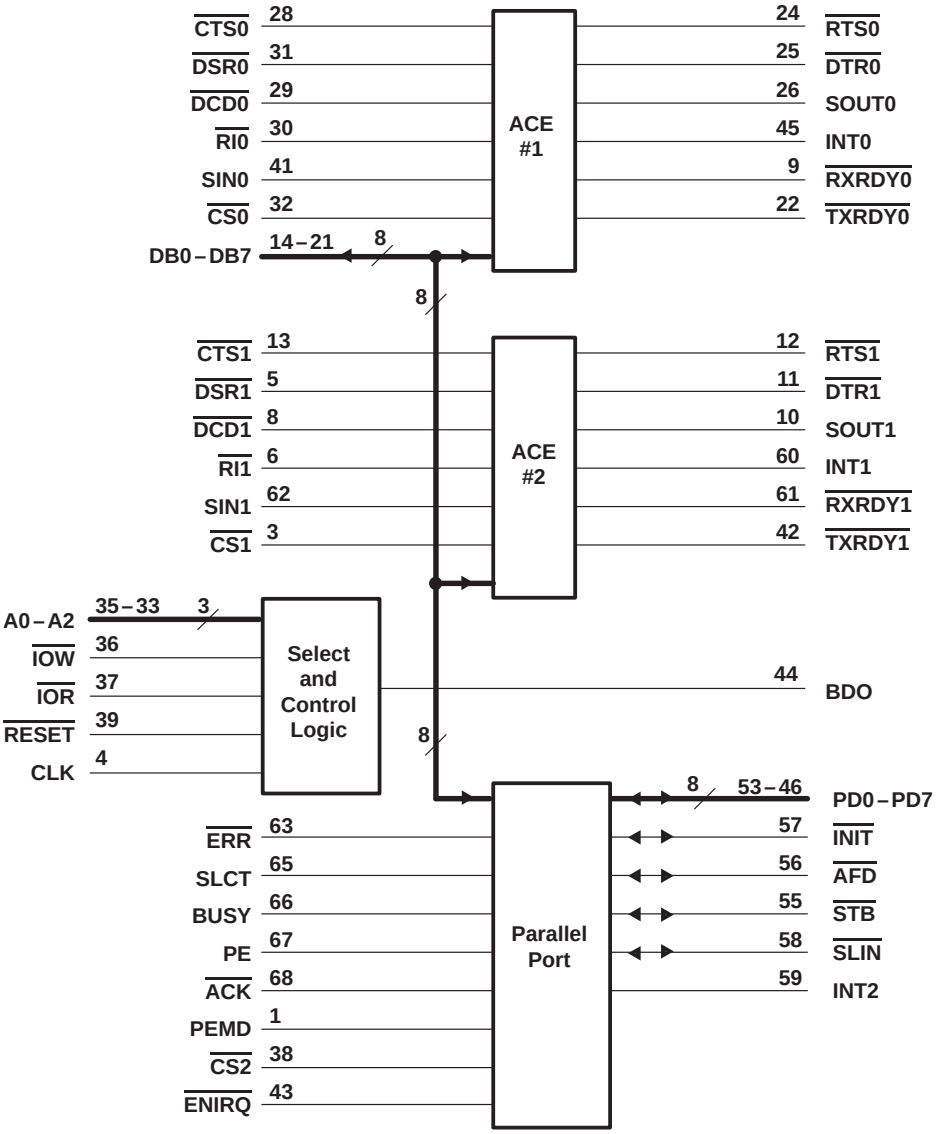
description

The TL16C552A is an enhanced dual-channel version of the popular TL16C550B asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed and the error conditions encountered.

In addition to its dual communications interface capabilities, the TL16C552A provides the user with a bidirectional parallel data port that fully supports the parallel Centronics-type printer interface. The parallel port and the two serial ports provide IBM PC/AT-compatible computers with a single device to serve the three system ports. A programmable baud rate generator that can divide the timing reference clock input by a divisor between 1 and (2^{16} – 1) is included.

The TL16C552A is available in a 68-pin plastic-leaded chip-carrier (FN) package and a 80-pin TQFP (PN) package. The TL16C552AM is available in a 68-pin ceramic quad flat (HV) package.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO. FN	TERMINAL NO. PN	I/O	DESCRIPTION
$\overline{\text{ACK}}$	68	10	I	Line printer acknowledge. $\overline{\text{ACK}}$ goes low to indicate a successful data transfer has taken place. $\overline{\text{ACK}}$ generates a printer port interrupt during its positive transition.
$\overline{\text{AFD}}$	56	75	I/O	Line printer autofeed. $\overline{\text{AFD}}$ is an open-drain line that provides the printer with an active-low signal when continuous form paper is to be autofed to the printer. $\overline{\text{AFD}}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
A0, A1, A2	35, 34, 33	51, 50, 49	I	Address. The address lines A0 – A2 select the internal registers during CPU bus operations. See Table 2 for the decode of the serial channels and Table 13 for the decode of the parallel printer port.
BDO	44	63	O	Bus buffer. BDO is the active-high output and is asserted when either the serial channel or the parallel port is read. BDO controls the system bus driver (74LS245 or 54LS245).
BUSY	66	8	I	Line printer busy. BUSY is an input line from the printer that goes high when the printer is not ready to accept data.
CLK	4	14	I	Clock. CLK is the external clock input to the baud rate divisor of each ACE.
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$, CS2	32, 3, 38	48, 13, 54	I	Chip select. Each $\overline{\text{CS}}$x input acts as an enable for the write and read signals for serial channels 1 ($\overline{\text{CS0}}$) and 2 ($\overline{\text{CS1}}$). CS2 enables the signals to the printer port.
$\overline{\text{CTS0}}$, $\overline{\text{CTS1}}$	28, 13	44, 26	I	Clear to send. The logical state of each $\overline{\text{CTS}}$x terminal is reflected in the CTS bit of the modem status register ($\overline{\text{CTS}}$ is bit 4 of the modem status register, written as MSR4) of each ACE. A change of state in either $\overline{\text{CTS}}$ terminal since the previous reading of the associated MSR causes the setting of ΔCTS (MSR0) of each modem status register.
DB0 – DB7	14 – 21	27 – 34	I/O	Data bits DB0 – DB7. The data bus provides eight I/O lines with 3-state outputs for the transfer of data, control, and status information between the TL16C552A and the CPU. These lines are normally in the high-impedance state except during read operations. DB0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
$\overline{\text{DCD0}}$, $\overline{\text{DCD1}}$	29, 8	45, 18	I	Data carrier detect. $\overline{\text{DCD}}$ is a modem input. Its condition can be tested by the CPU by reading MSR7 ($\overline{\text{DCD}}$) of the modem status registers. MSR3 (ΔDCD) of the modem status register indicates whether $\overline{\text{DCD}}$ has changed states since the previous reading of the MSR. $\overline{\text{DCD}}$ has no effect on the receiver.
$\overline{\text{DSR0}}$, $\overline{\text{DSR1}}$	31, 5	47, 15	I	Data set ready. The logical state of the $\overline{\text{DSR}}$x terminals is reflected in MSR5 of its associated modem status register. ΔDSR (MSR1) indicates whether the associated $\overline{\text{DSR}}$x terminal has changed states since the previous reading of the MSR.
$\overline{\text{DTR0}}$, $\overline{\text{DTR1}}$	25, 11	38, 24	O	Data terminal ready. Each $\overline{\text{DTR}}$x can be set low by setting MCR0, modem control register bit 0 of its associated ACE. $\overline{\text{DTR}}$x is cleared (high) by clearing the DTR bit (MCR0) or whenever a reset occurs. When active (low), $\overline{\text{DTR}}$x indicates that its ACE is ready to receive data.
$\overline{\text{ENIRQ}}$	43	59	I	Parallel port interrupt source mode selection. When $\overline{\text{ENIRQ}}$ is low, the AT mode of interrupts is enabled. In AT mode, INT2 is internally connected to $\overline{\text{ACK}}$. When $\overline{\text{ENIRQ}}$ is tied high, the PS-2 mode of interrupt is enabled and INT2 is internally tied to the inverse of the $\overline{\text{PRINT}}$ bit in the line printer status register. INT2 is latched high on the rising edge of $\overline{\text{ACK}}$. INT2 is held until the status register is read, which then clears the $\overline{\text{PRINT}}$ status bit and INT2.
$\overline{\text{ERR}}$	63	5	I	Line printer error. $\overline{\text{ERR}}$ is an input line from the printer. The printer reports an error by holding $\overline{\text{ERR}}$ low during the error condition.
GND	7, 27, 54	17, 43, 73		Ground (0 V). All terminals must be tied to GND for proper operation.
$\overline{\text{INIT}}$	57	76	I/O	Line printer initialize. $\overline{\text{INIT}}$ is an open-drain line that provides the printer with an active-low signal that allows the printer initialization routine to be started. $\overline{\text{INIT}}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
INT0, INT1	45, 60	64, 79	O	External serial channel interrupt. Each serial channel interrupt 3-state output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the interrupt enable register of its associated channel: receiver error flag, received data available, transmitter holding register empty, and modem status. The interrupt is cleared on appropriate service. Upon reset, the interrupt output is in the high-impedance state.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO. FN	TERMINAL NO. PN	I/O	DESCRIPTION
INT2	59	78	O	Printer port interrupt. INT2 is an active-high, 3-state output generated by the positive transition of $\overline{ACK}$. INT2 is enabled by bit 4 of the write control register. Upon reset, INT2 is in the high-impedance state. Its mode is also controlled by $\overline{ENIRQ}$.
$\overline{IOR}$	37	53	I	Input/output read strobe. $\overline{IOR}$ is an active-low input that enables the selected channel to output data to the data bus (DB0–DB7). The data output depends on the register selected by the address inputs A0, A1, A2, and chip select. Chip select 0 ($\overline{CS0}$) selects ACE #1, chip select 1 ($\overline{CS1}$) selects ACE #2, and chip select 2 ($\overline{CS2}$) selects the printer port.
$\overline{IOW}$	36	52	I	Input/output write strobe. $\overline{IOW}$ is an active-low input causing data from the data bus to be input to either ACE or to the parallel port. The destination depends on the register selected by the address inputs A0, A1, A2, and chip selects $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$.
PD0–PD7	53–46	72–65	I/O	Parallel data bits (0–7). PD0–PD7 provide a byte wide input or output port to the system.
PE	67	9	I	Line printer paper empty. PE is an input line from the printer that goes high when the printer runs out of paper.
PEMD	1	11	I	Printer enhancement mode. When low, PEMD enables the write data register to the PD0–PD7 lines. A high on PEMD allows direction control of the PD0–PD7 port by the DIR bit in the control register. PEMD is usually tied low for the printer operation.
$\overline{RESET}$	39	55	I	Reset. When low, $\overline{RESET}$ forces the TL16C552A into an idle mode in which all serial data activities are suspended. The modem control register and its associated outputs are cleared. The line status register is cleared except for the transmitter holding register empty (THRE) and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities. $\overline{RESET}$ has a hysteresis level of typically 400 mV.
$\overline{RTS0}$, $\overline{RTS1}$	24, 12	37, 25	O	Request to send. The $\overline{RTS}$ outputs are set low by setting MCR1 of its UARTs modem control register. Both $\overline{RTS}$ terminals are reset high by $\overline{RESET}$. A low on $\overline{RTS}$ indicates that its ACE has data ready to transmit. In half-duplex operations, $\overline{RTS}$ controls the direction of the line.
RXRDY0, $\overline{RXRDY1}$	9, 61	19, 3	O	Receiver ready. Receiver direct memory access (DMA) signaling is also available through this output. One of two types of DMA signaling can be selected using FCR3 when in FIFO mode. Only DMA mode 0 is allowed when in TL16C450 mode. For signal transfer DMA (a transfer is made between CPU bus cycles), mode 0 is used. Multiple transfers that are made continuously until the receiver FIFO has been emptied are supported by mode 1. Mode 0. $\overline{RXRDY}$ is active (low) in FIFO mode (FCR0 = 1, FCR3 = 0) or in TL16C450 mode (FCR0 = 0) and the receiver FIFO or receiver holding register contains at least one character. When there are no more characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). Mode 1. $\overline{RXRDY}$ goes active (low) in the FIFO mode (FCR0 = 1) when FCR3 = 1 and the time-out or trigger levels have been reached. $\overline{RXRDY}$ goes inactive (high) when the FIFO or holding register is empty.
$\overline{RI0}$, $\overline{RI1}$	30, 6	46, 16	I	Ring indicator. The $\overline{RI}$ signal is a modem control input. Its condition is tested by reading MSR6 (RI) of each ACE. The modem status register output TERI (MSR2) indicates whether $\overline{RI}$ has changed from high to low since the previous reading of the modem status register.
SIN0, SIN1	41, 62	57, 4	I	Serial data. SIN0 and SIN1 move information from the communication line or modem to the TL16C552A receiver circuits. Mark is a high state and space is a low state. Data on serial data inputs is disabled in loop mode.
SLCT	65	7	I	Line printer select. SLCT is an input line from the printer that goes high when the printer is selected.
$\overline{SLIN}$	58	77	I/O	Line printer select. $\overline{SLIN}$ is an open-drain I/O that selects the printer when active (low). $\overline{SLIN}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO. FN	TERMINAL NO. PN	I/O	DESCRIPTION
SOUT0, SOUT1	26, 10	39, 23	O	Serial data outputs. SOUT0 and SOUT1 are the serial data outputs from the ACE transmitter circuitry. A mark is a high state and a space is a low state. Each SOUT is held in the mark condition when the transmitter is disabled ($\overline{\text{RESET}}$ is asserted low), the transmitter register is empty, or when in the loop mode.
$\overline{\text{STB}}$	55	74	I/O	Line printer strobe. STB provides communication between the TL16C552A and the printer. When $\overline{\text{STB}}$ is active (low), it provides the printer with a signal to latch the data currently on the parallel port. STB has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
TRI	2	12	I	3-state output control input. TRI controls the 3-state control of all I/O and output terminals. When TRI is asserted, all I/Os and outputs are in the high-impedance state, allowing board level testers to drive the outputs without overdriving internal buffers. TRI is level sensitive and is pulled down with an internal resistor that is approximately 5 kΩ.
$\overline{\text{TXRDY0}}$ $\overline{\text{TXRDY1}}$	22, 42	35, 58	O	Transmitter ready. Two types of DMA signaling are available. Either can be selected using FCR3 when operating in FIFO mode. Only DMA mode 0 is allowed when in TL16C450 mode. Single-transfer DMA (a transfer is made between CPU bus cycles) is supported by mode 0. Multiple transfers that are made continuously until the transmitter FIFO has been filled are supported by mode 1. Mode 0. In FIFO mode (FCR0 = 1, FCR3 = 0) or in TL16C450 mode (FCR0 = 0) when there are no characters in the transmitter holding register or transmitter FIFO, $\overline{\text{TXRDYx}}$ is active (low). Once $\overline{\text{TXRDYx}}$ is activated (low), it goes inactive after the first character is loaded into the holding register of the transmitter FIFO. Mode 1. $\overline{\text{TXRDY}}$ goes active (low) in FIFO mode (FCR0 = 1) when FCR3 = 1 and there are no characters in the transmitter FIFO. When the transmitter FIFO is completely full, $\overline{\text{TXRDY}}$ goes inactive (high).
V_{DD}	23, 40, 64	6, 36, 56		Power supply. The V_{DD} requirement is 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.5 V to V_{DD} + 0.3 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Output voltage range, V_O . . . . . –0.5 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: I suffix . . . . . –40°C to 85°C
M suffix . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

DISSIPATION RATING TABLE‡

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR§ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FN	1730 mW	19.2 mW/°C	865 mW	–
HV	1689 mW	13.5 mW/°C	1081 mW	337 mW

‡ Power ratings assume a maximum junction temperature (T_J) of 115°C for ’I’ and 150°C for ’M’ suffix devices.
§ Derating factor is the inverse of the junction-to-ambient thermal resistance, $R_{\theta JA}$.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75	5	5.25	V
Clock high-level input voltage, $V_{IH(CLK)}$		2		V_{DD}	V
Clock low-level input voltage, $V_{IL(CLK)}$		0		0.8	V
High-level input voltage, V_{IH}		2		V_{DD}	V
Low-level input voltage, V_{IL}		0		0.8	V
Clock frequency, f_{clock}				16	MHz
Operating free-air temperature, T_A	I suffix	–40		85	°C
	M suffix	–55		125	°C

package thermal characteristics

PARAMETER		TEST CONDITIONS	FN Package			HV Package			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$R_{\theta JA}$	Junction-to-ambient thermal impedance	Board mounted, no air flow		52			74		°C/W
$R_{\theta JC}$	Junction-to-case thermal impedance			14			3		°C/W
T_J	Junction temperature				115			150	°C/W

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –12 mA for PD0–PD7, I_{OH} = –4 mA for all other outputs (see Note 2),	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 12 mA for PD0–PD7, I_{OL} = 12 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$, I_{OL} = 4 mA for all other outputs		0.4	V
I_I	Input current	V_{DD} = 5.25 V (see Note 3), All other terminals are floating		±10	µA
$I_{I(CLK)}$	Clock input current	V_I = 0 to 5.25 V		±10	µA
I_{OZ}	High-impedance output current	V_{DD} = 5.25 V, V_O = 0 with chip deselected or V_O = 5.25 V with chip and write mode selected (see Note 2)		±20	µA
I_{DD}	Supply current	V_{DD} = 5.25 V, No loads on outputs, Inputs at 0.8 V or 2 V, f_{clock} = 8 MHz		50	mA

NOTES: 2. Excluding $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$. They are open-drain terminals with an internal pullup resistor to V_{DD} of approximately 10 KΩ.
3. Excluding the TRI input terminal. It contains an internal pulldown resistor of approximately 5 kΩ.

clock timing requirements over recommended ranges of operating free-air temperature and supply voltage

		MIN	MAX	UNIT
t_{w1}	Pulse duration, CLK ↑ (external clock) (see Figure 1)	31		ns
t_{w2}	Pulse duration, CLK ↓ (external clock) (see Figure 1)	31		ns
t_{w3}	Pulse duration, $\overline{RESET}$	1000		ns

read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Note 4 and Figure 4)

		MIN	MAX	UNIT
t_{w4}	Pulse duration, $\overline{IOR}$ ↓	80		ns
t_{su1}	Setup time, $\overline{CSx}$ valid before $\overline{IOR}$ ↓ (see Note 5)	15		ns
t_{su2}	Setup time, A2–A0 valid before $\overline{IOR}$ ↓ (see Note 5)	15		ns
t_{h1}	Hold time, A2–A0 valid after $\overline{IOR}$ ↑ (see Note 5)	20		ns
t_{h2}	Hold time, $\overline{CSx}$ valid after $\overline{IOR}$ ↑ (see Note 5)	20		ns
t_{d1}	Delay time, $t_{su2} + t_{w4} + t_{d2}$ (see Note 6)	175		ns
t_{d2}	Delay time, $\overline{IOR}$ ↑ to $\overline{IOR}$ or $\overline{IOW}$ ↓	80		ns

NOTES: 4. These parameters are not production tested.
5. The internal address strobe is always active.
6. In FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (interrupt identification register and line status register).

write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Note 7 and Figure 5)

		MIN	MAX	UNIT
t_{w5}	Pulse duration, $\overline{IOW}$ ↓	80		ns
t_{su4}	Setup time, $\overline{CSx}$ valid before $\overline{IOW}$ ↓ (see Note 8)	15		ns
t_{su5}	Setup time, A2–A0 valid before $\overline{IOW}$ ↓ (see Note 8)	15		ns
t_{su6}	Setup time, DB0–DB7 valid before $\overline{IOW}$ ↑	15		ns
t_{h3}	Hold time, A2–A0 valid after $\overline{IOW}$ ↑ (see Note 8)	20		ns
t_{h4}	Hold time, $\overline{CSx}$ valid after $\overline{IOW}$ ↑ (see Note 8)	20		ns
t_{h5}	Hold time, DB0–DB7 valid after $\overline{IOW}$ ↑	15		ns
t_{d3}	Delay time, $t_{su5} + t_{w5} + t_{d4}$	175		ns
t_{d4}	Delay time, $\overline{IOW}$ ↑ to $\overline{IOW}$ or $\overline{IOR}$ ↓	80		ns

NOTES: 7. These parameters are not production tested.
8. The internal address strobe is always active.

read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Note 9 and Figure 4)

	PARAMETER	MIN	MAX	UNIT
t_{pd1}	Propagation delay time from $\overline{IOR}$ ↓ to BDO ↑ or from $\overline{IOR}$ ↑ to BDO ↓		60	ns
t_{en}	Enable time from $\overline{IOR}$ ↓ to DB0–DB7 valid (see Note 10)		60	ns
t_{dis}	Disable time from $\overline{IOR}$ ↑ to DB0–DB7 released (see Note 10)		60	ns

NOTES: 9. These parameters are not production tested.
10. V_{OL} and V_{OH} (and the external loading) determine the charge and discharge time.

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Note 11 and Figures 6, 7, and 8)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, interrupt THRE ↓ to SOUT ↓ at start	See Figure 6	8	24	RCLK cycles
t_{d6}	Delay time, SOUT ↓ at start to interrupt THRE ↑	See Note 12 and Figure 6	8	9	RCLK cycles
t_{d7}	Delay time, $\overline{IOW}$ (WR THR) ↑ to interrupt THRE ↑	See Note 12 and Figure 6	16	32	RCLK cycles
t_{d8}	Delay time, SOUT ↓ at start to $\overline{TXRDY}$ ↓	C_L = 100 pF, See Figures 7 and 8		8	RCLK cycles
t_{pd2}	Propagation delay time from $\overline{IOW}$ (WR THR) ↓ to interrupt THRE ↓	C_L = 100 pF, See Figure 6		140	ns
t_{pd4}	Propagation delay time from $\overline{IOR}$ (RD IIR) ↑ to interrupt THRE ↓	C_L = 100 pF, See Figure 6		140	ns
t_{pd5}	Propagation delay time from $\overline{IOW}$ (WR THR) ↑ to $\overline{TXRDY}$ ↑	C_L = 100 pF, See Figures 7 and 8		195	ns

NOTES: 11. These parameters are not production tested.
12. When the transmitter interrupt delay is active, this delay is lengthened by one character time minus the last stop bit time.

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Note 13 and Figures 9 through 13)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time from stop to INT ↑	See Note 14		1	RCLK cycle
t_{pd6}	Propagation delay time from RCLK ↑ to sample CLK ↑			100	ns
t_{pd7}	Propagation delay time from $\overline{IOR}$ (RD RBR/RD LSR) ↓ to reset interrupt ↓	C_L = 100 pF		150	ns
t_{pd8}	Propagation delay time from $\overline{IOR}$ (RD RBR) ↓ to $\overline{RXRDY}$ ↑			150	ns

NOTES: 13. These parameters are not production tested.
14. The receiver data available indicator, the overrun error indicator, the trigger level interrupts, and the active $\overline{RXRDY}$ indicator are delayed three RCLK cycles in FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) are delayed three RCLK cycles. These indicators are updated immediately for any further bytes received after RDRBR goes active. There are eight RCLK cycle delays for trigger change level interrupts.

modem control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Note 15 and Figure 14)

PARAMETER		MIN	MAX	UNIT
t_{pd9}	Propagation delay time from $\overline{IOW}$ (WR MCR) ↑ to $\overline{RTS}$ ($\overline{DTR}$) ↓↑		100	ns
t_{pd10}	Propagation delay time from modem input ($\overline{CTS}$, $\overline{DSR}$) ↓↑ to interrupt ↑		170	ns
t_{pd11}	Propagation delay time from $\overline{IOR}$ (RD MSR) ↑ to interrupt ↓		140	ns
t_{pd12}	Propagation delay time from $\overline{RI}$ ↑ to interrupt ↑		170	ns

NOTE 15: These parameters are not production tested.

parallel port timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 16 and Figures 15, 16, and 17)

		MIN	MAX	UNIT
t_{su7}	Setup time, data valid before $\overline{STB}$ ↓	1		µs
t_{h6}	Hold time, data valid after $\overline{STB}$ ↑	1		µs
t_{w6}	Pulse duration, $\overline{STB}$ ↓	1		µs
t_{d10}	Delay time, BUSY ↑ to $\overline{ACK}$ ↓	Defined by printer		
t_{d11}	Delay time, BUSY ↓ to $\overline{ACK}$ ↓	Defined by printer		
t_{w7}	Pulse duration, BUSY ↑	Defined by printer		
t_{w8}	Pulse duration, $\overline{ACK}$ ↓	Defined by printer		
t_{d12}	Delay time, BUSY ↑ after $\overline{STB}$ ↑	Defined by printer		
t_{d13}	Delay time, INT2 ↓ after $\overline{ACK}$ ↓ (see Note 17)		22	ns
t_{d14}	Delay time, INT2 ↑ after $\overline{ACK}$ ↑ (see Note 17)		20	ns
t_{d15}	Delay time, INT2 ↑ after $\overline{ACK}$ ↑ (see Note 17)		24	ns
t_{d16}	Delay time, INT2 ↓ after $\overline{IOR}$ ↑ (see Note 17)		25	ns

NOTES: 16. These parameters are not production tested.
17. t_{d13}–t_{d16} are all measured with a 15-pF load.

PARAMETER MEASUREMENT INFORMATION

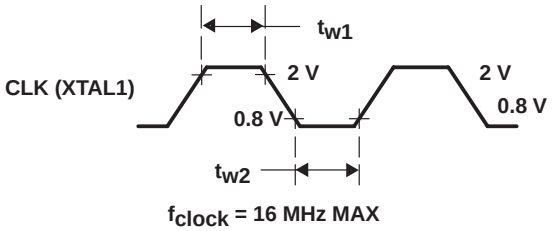
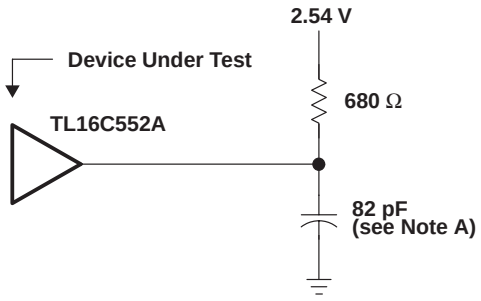


Figure 1. CLK Voltage Waveform



NOTE A: This includes scope and jig capacitance.

Figure 2. Output Load Circuit

PARAMETER MEASUREMENT INFORMATION

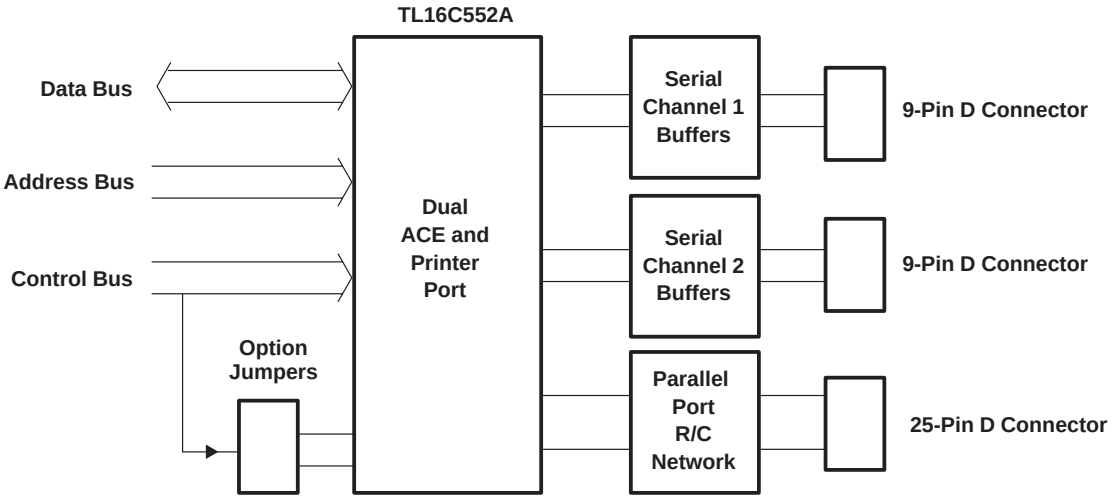


Figure 3. Basic Test Configuration

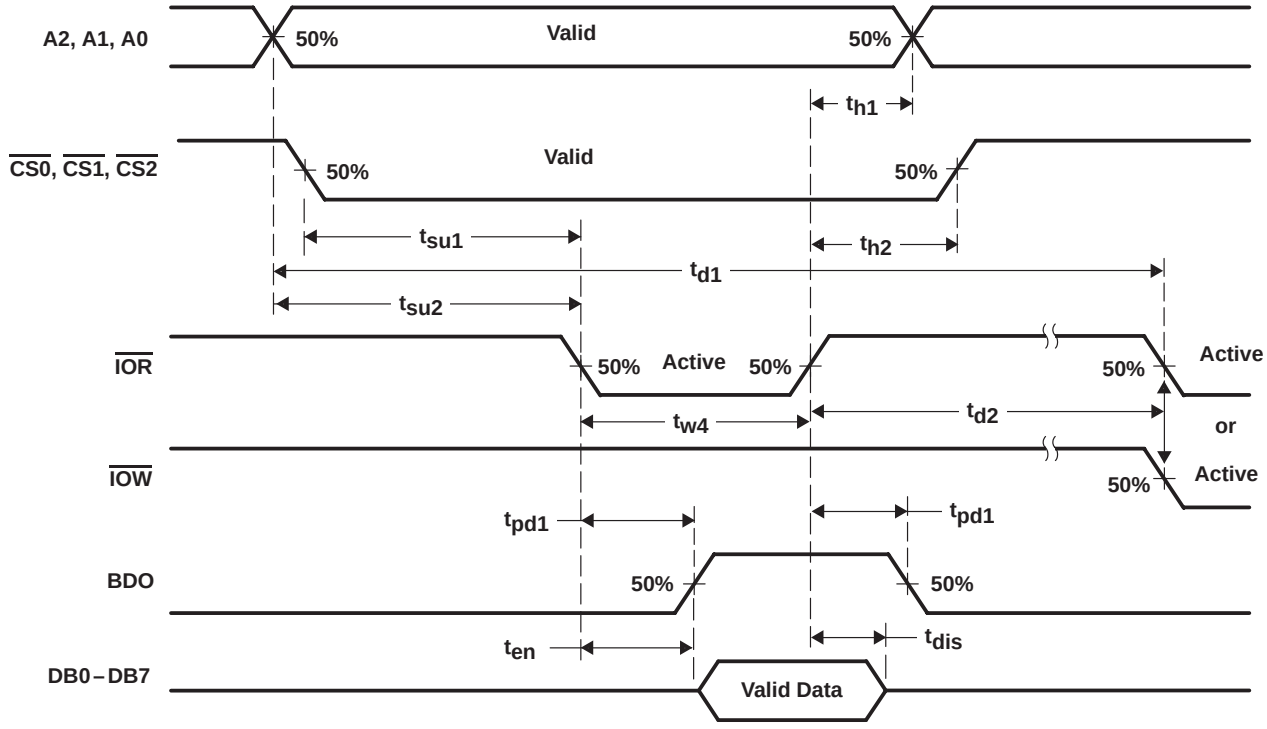


Figure 4. Read Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

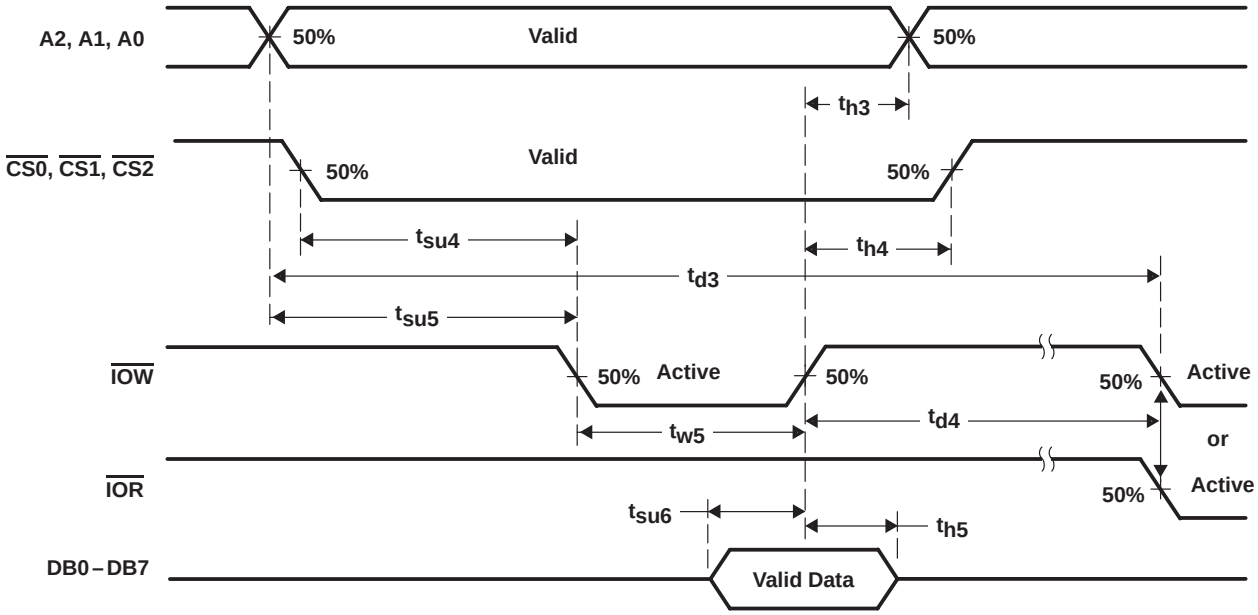


Figure 5. Write Cycle Timing Waveforms

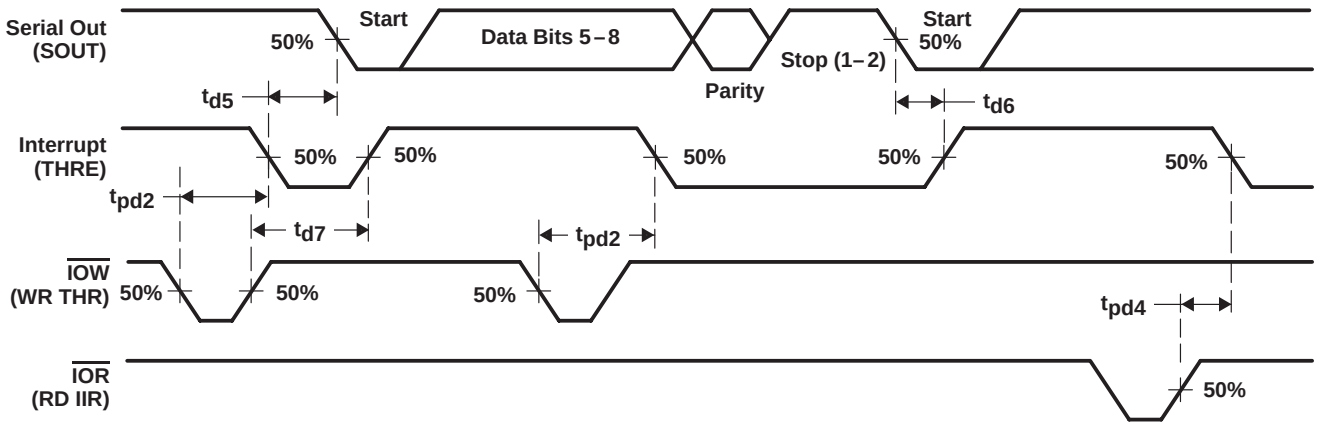


Figure 6. Transmitter Timing Waveforms

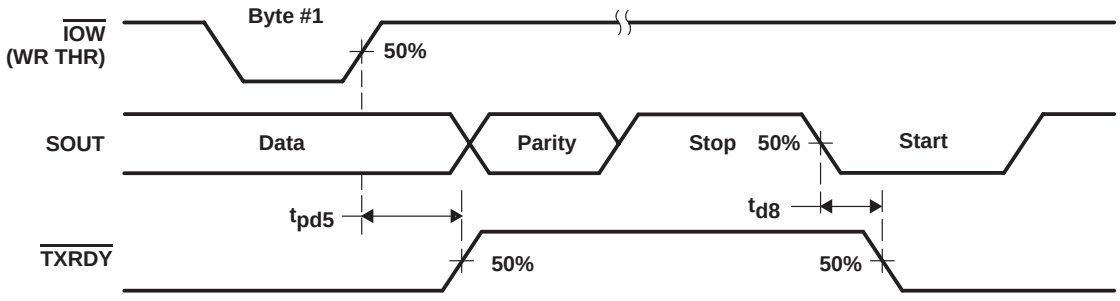


Figure 7. Transmitter Ready Mode 0 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

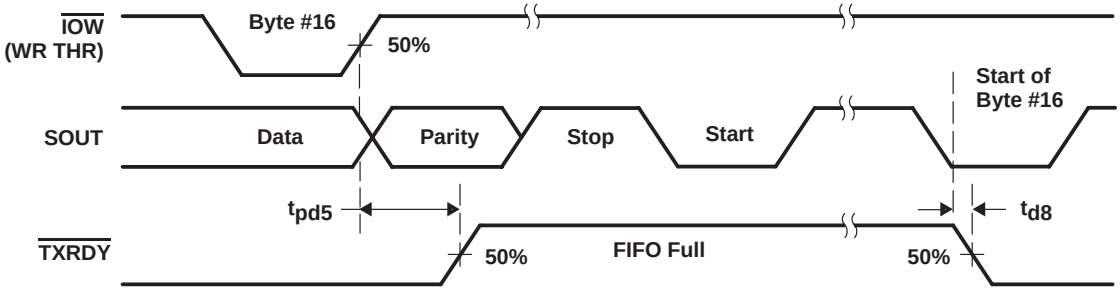


Figure 8. Transmitter Ready Mode 1 Timing Waveforms

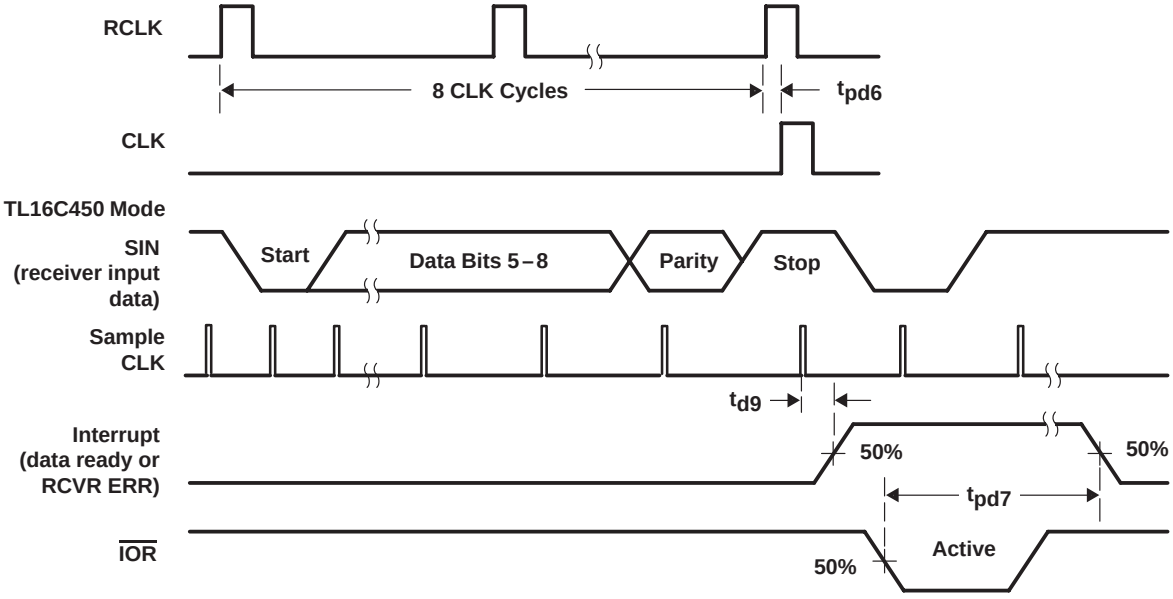


Figure 9. Receiver Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

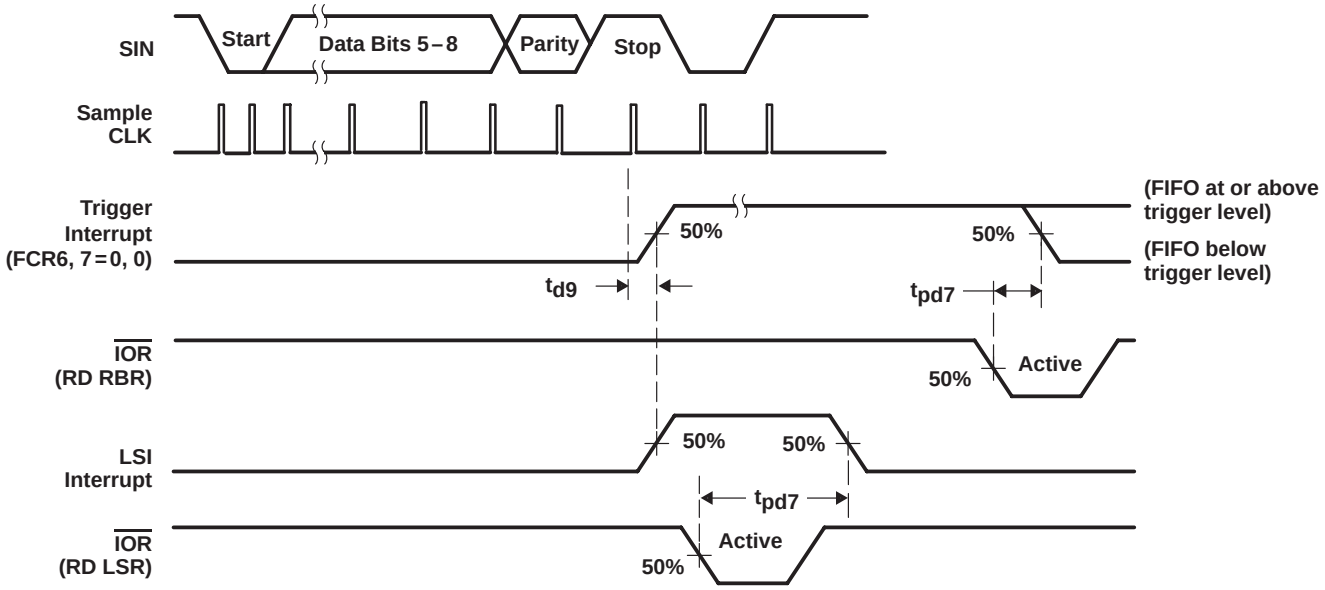
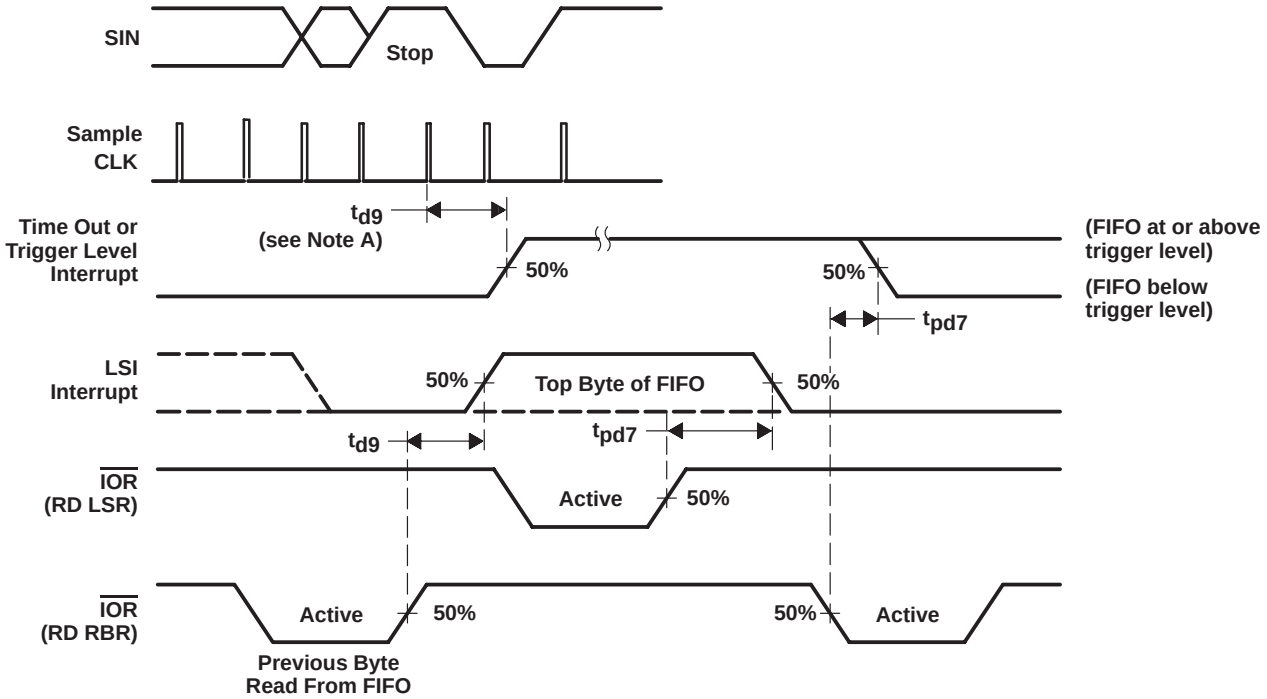


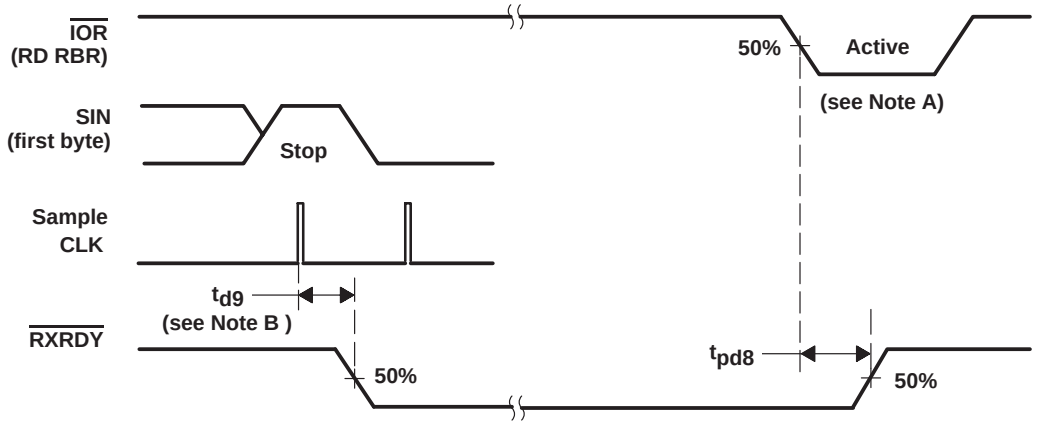
Figure 10. Receiver FIFO First Byte (Sets RDR) Waveforms



NOTE A: This is the reading of the last byte in the FIFO.

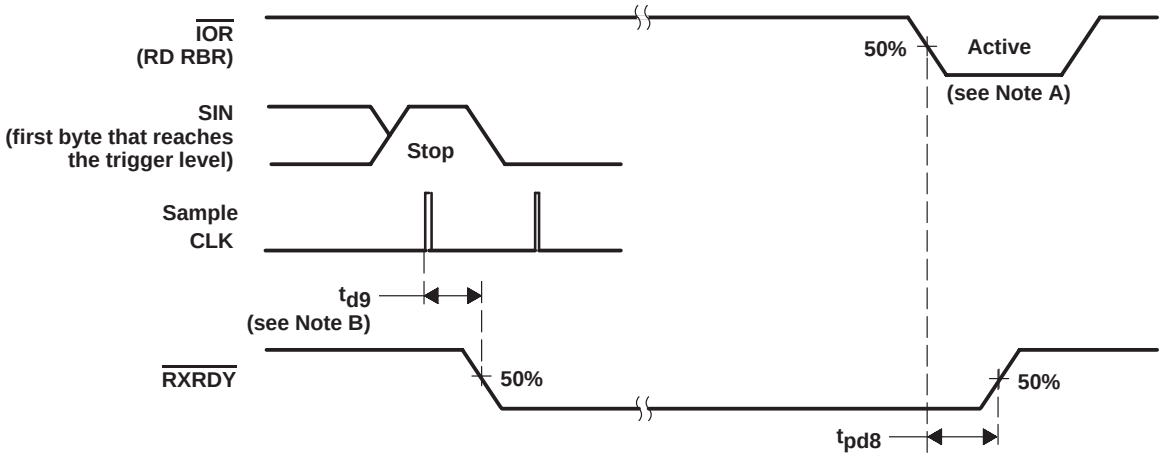
Figure 11. Receiver FIFO After First Byte (After RDR Set) Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0 = 1, t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

Figure 12. Receiver Ready Mode 0 Waveforms



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0–1, t_{d9} = 3 RCLK cycles. For a trigger change level interrupt, t_{d9} = 8 RCLK.

Figure 13. Receiver Ready Mode 1 Waveforms

PARAMETER MEASUREMENT INFORMATION

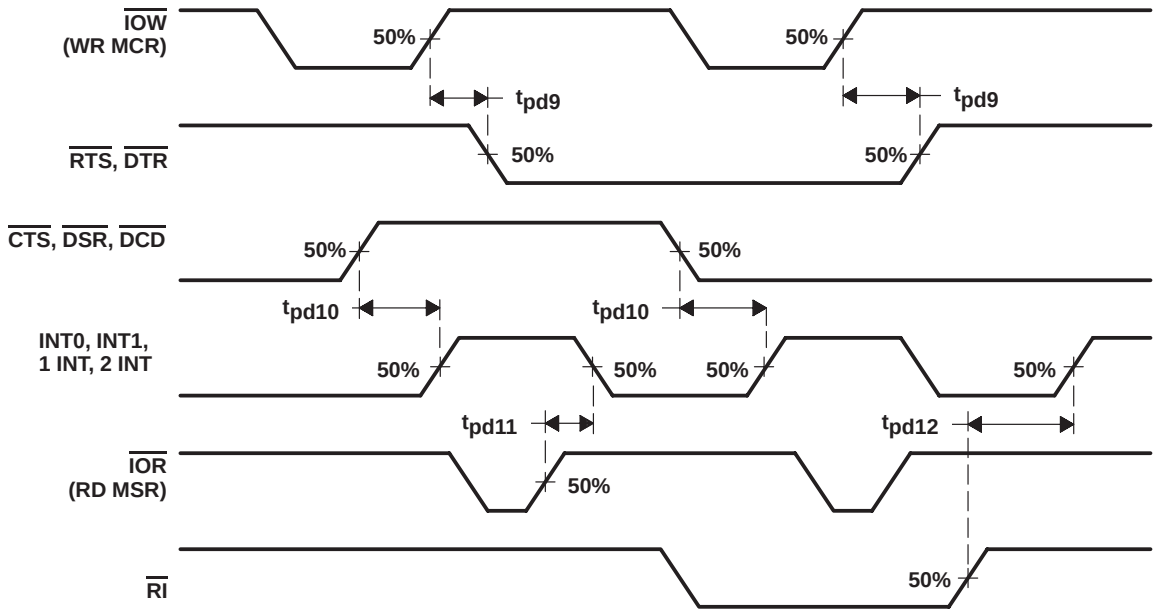


Figure 14. Modem Control Timing Waveforms

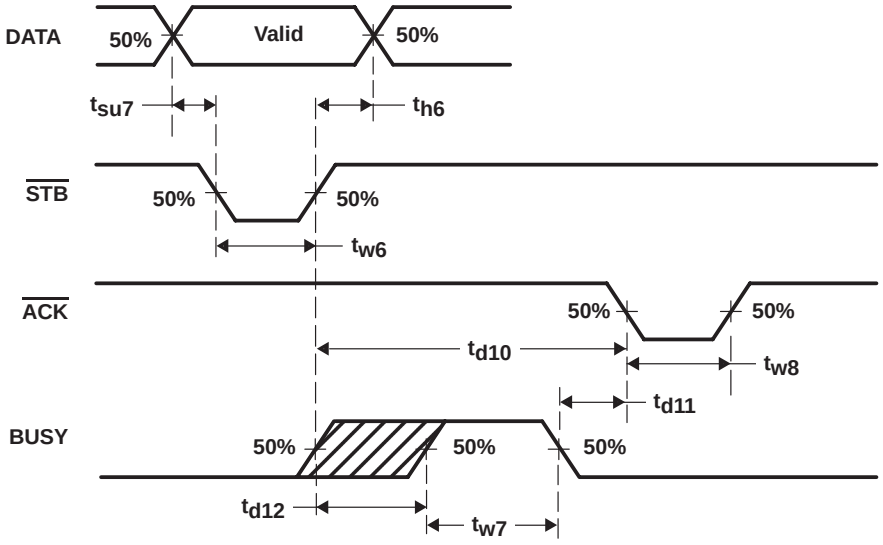
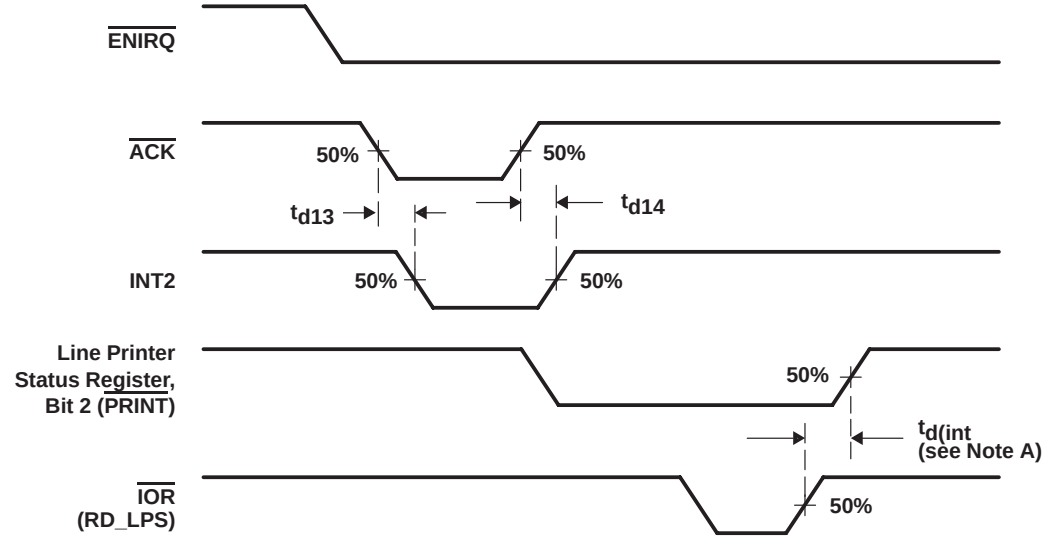


Figure 15. Parallel Port Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: A timing value is not provided for $t_{d(int)}$ in the tables because the line printer status register, bit 2 ($\overline{PRINT}$) is an internal signal.

Figure 16. Parallel Port AT Mode Timing (ENIRQ = Low) Waveforms

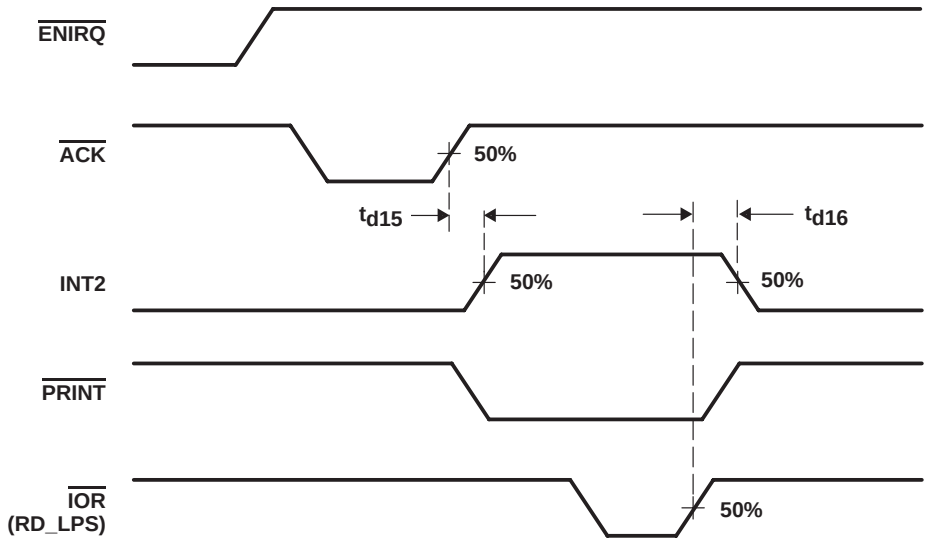


Figure 17. Parallel Port PS/2 Mode Timing (ENIRQ = High) Waveforms

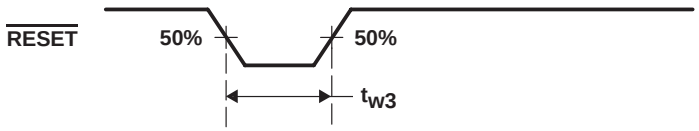


Figure 18. $\overline{RESET}$ Voltage Waveform

PRINCIPLES OF OPERATION

Three types of information are stored in the internal registers used in the ACE: control, status, and data. Mnemonic abbreviations for the internal registers are shown in Table 1.

Table 1. Internal Register Mnemonic Abbreviations

CONTROL	MNEMONIC	STATUS	MNEMONIC	DATA	MNEMONIC
Line control register	LCR	Line status register	LSR	Receiver buffer register	RBR
FIFO control register	FCR	Modem status register	MSR	Transmitter holding register	THR
Modem control register	MCR				
Divisor latch LSB	DLL				
Divisor latch MSB	DLM				
Interrupt enable register	IER				

The address, read, and write inputs are used with the divisor latch access bit (DLAB) in the line control register (bit 7) to select the register to be written to or read from (see Table 2). Individual bits within the registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR7 refers to line control register bit 7.

The transmitter holding register and receiver buffer register are data registers that hold from five to eight bits of data. If fewer than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered (TL16C450 mode) or FIFO buffered (FIFO mode) so that read and write operations can be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

Table 2. Register Selection†

DLAB	A2	A1	A0	MNEMONIC	REGISTER
L	L	L	L	RBR	Receiver buffer register (read only)
L	L	L	L	THR	Transmitter holding register (write only)
L	L	L	H	IER	Interrupt enable register
X	L	H	L	IIR	Interrupt identification register (read only)
X	L	H	L	FCR	FIFO control register (write only)
X	L	H	H	LCR	Line control register
X	H	L	L	MCR	Modem control register
X	H	L	H	LSR	Line status register
X	H	H	L	MSR	Modem status register
X	H	H	H	SCR	Scratch pad register
H	L	L	L	DLL	LSB divisor latch
H	L	L	H	DLM	MSB divisor latch

† The serial channel is accessed when either $\overline{CS0}$ or $\overline{CS1}$ is low.
X = irrelevant, L = low level, H = high level

PRINCIPLES OF OPERATION

accessible registers

Using the CPU, the system programmer has access to and control over any of the ACE registers that are summarized in Table 1. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

ADDRESS	REGISTER MNEMONIC	REGISTER BIT NUMBER							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RBR (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0†	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1†	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable modem status interrupt	(ERLSI) Enable receiver line status interrupt	(ETBEI) Enable transmitter holding register empty interrupt	(ERBFI) Enable received data available interrupt
2	FCR (write only)	Receiver trigger (MSB)	Receiver trigger (LSB)	Reserved	Reserved	DMA mode select	Transmitter FIFO reset	Receiver FIFO reset	FIFO enable
2	IIR (read only)	FIFOs enabled‡	FIFOs enabled‡	0	0	Interrupt ID bit 3‡	Interrupt ID bit 2	Interrupt ID bit 1	0 if interrupt pending
3	LCR	(DLAB) Divisor latch access bit	Set break	Stick parity	(EPS) Even parity select	(PEN) Parity enable	(STB) Number of stop bits	(WLSB1) Word length select bit 1	(WLSB0) Word length select bit 0
4	MCR	0	0	0	Loop	OUT2 Enable external interrupt (INT0 or INT1)	OUT1 (an unused internal signal)	(RTS) Request to send	(DTR) Data terminal ready
5	LSR	Error in receiver FIFO‡	(TEMT) Transmitter empty	(THRE) Transmitter holding register empty	(BI) Break interrupt	(FE) Framing error	(PE) Parity error	(OE) Overrun error	(DR) Data ready
6	MSR	(DCD) Data carrier detect	(RI) Ring indicator	(DSR) Data set ready	(CTS) Clear to send	(ΔDCD) Delta data carrier detect	(TERI) Trailing edge ring indicator	(ΔDSR) Delta data set ready	(ΔCTS) Delta clear clear to send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

† DLAB = 1
‡ These bits are always 0 when FIFOs are disabled.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

This write-only register is at the same location as the interrupt identification register. It enables and clears the FIFOs, sets the trigger level of the receiver FIFO, and selects the type of DMA signaling.

- Bit 0: FCR0 enables both the transmitter and receiver FIFOs. All bytes in both FIFOs can be cleared by clearing FCR0. Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode and vice versa. Programming of other FCR bits is enabled by setting FCR0.
- Bit 1: When set, FCR1 clears all bytes in the receiver FIFO and resets the counter. This does not clear the shift register.
- Bit 2: When set, FCR2 clears all bytes in the transmitter FIFO and resets the counter. This does not clear the shift register.
- Bit 3: When set, FCR3 changes the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ terminals from mode 0 to mode 1 when FCR0 is set.
- Bits 4 and 5: FCR4 and FCR5 are reserved for future use.
- Bits 6 and 7: FCR6 and FCR7 set the trigger level for the receiver FIFO interrupt (see Table 4).

Table 4. Receiver FIFO Trigger Level

BIT		RECEIVER FIFO TRIGGER LEVEL (BYTES)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

The following receiver status occurs when the receiver FIFO and receiver interrupts are enabled:

1. LSR0 is set when a character is transferred from the shift register to the receiver FIFO. When the FIFO is empty, it is reset.
2. IIR = 06 receiver line status interrupt has higher priority than the received data available interrupt IIR = 04.
3. Receive data available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. When the FIFO drops below its programmed trigger level, it is cleared.
4. IIR = 04 (receive data available indicator) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following receiver FIFO character time-out status occurs when receiver FIFO and receiver interrupts are enabled.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

1. When the following conditions exist, a FIFO character time-out interrupt occurs:
   a. Minimum of one character in FIFO
   b. The last received serial character is longer than four previous continuous-character times (if two stop bits are programmed, the second one is included in the time delay).
   c. The last CPU read of the FIFO is more than four previous continuous-character times. At 300 baud and 12-bit characters, the FIFO time-out interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the RCLK input for a clock signal, the character times can be calculated. The delay is proportional to the baud rate.
3. The time-out timer is reset after the CPU reads the receiver FIFO or after a new character is received when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the receiver FIFO.

Transmitter interrupts occur as follows when the transmitter and transmitter FIFO interrupts are enabled (FCR0 = 1, IER = 1).

1. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR = 02) occurs. The interrupt is cleared when the transmitter holding register is written to or the IIR is read. One to sixteen characters can be written to the transmit FIFO when servicing this interrupt.
2. The transmitter FIFO empty indicators are delayed one character time minus the last stop bit time when the following occurs:

   THRE = 1 and there is not a minimum of two bytes at the same time in transmitter FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate, assuming it is enabled.

Receiver FIFO trigger level and character time-out interrupts have the same priority as the received data available interrupt. The transmitter holding register empty interrupt has the same priority as the transmitter FIFO empty interrupt.

FIFO polled mode operation

Clearing IER0, IER1, IER2, IER3, or all with FCR0 = 1 puts the ACE into the FIFO polled mode. The receiver and transmitter are controlled separately. Either one or both can be in the polled mode.

In the FIFO polled mode, there is no time-out condition indicated or trigger level reached. However, the receiver and transmitter FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

interrupt enable register (IER)

The IER independently enables the four serial channel interrupt sources that activate the interrupt (INT0 or INT1) output. All interrupts are disabled by clearing IER0 – IER3. Interrupts are enabled by setting the appropriate bits of the IER. Disabling the interrupt system inhibits the interrupt identification register and the active (high) interrupt output. All other system functions operate in their normal manner, including the setting of the LSRs and MSRs. The contents of the IER shown in Table 3 are described in the following bulleted list.

- Bit 0: When IER0 is set, IER0 enables the received data available interrupt and the time-out interrupts in the FIFO mode.

PRINCIPLES OF OPERATION

interrupt enable register (IER) (continued)

- Bit 1: When IER1 is set, the transmitter holding register empty interrupt is enabled.
- Bit 2: When IER2 is set, the receiver line status interrupt is enabled.
- Bit 3: When IER3 is set, the modem status interrupt is enabled.
- Bits 4 – 7: IER4 through IER7 are cleared.

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the IIR. The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 5.

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	None	None	None	None
0	1	1	0	First	Receiver line status	OE, PE, FE, or BI	LSR read
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	RBR read until FIFO drops below the trigger level
1	1	0	0	Second	Character time-out indicator	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time.	RBR read
0	0	1	0	Third	THRE	THRE	IIR read if THRE is the interrupt source or THR write
0	0	0	0	Fourth	Modem status	$\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{RI}}$, or $\overline{\text{DCD}}$	MSR read

- Bit 0: IIR0 indicates whether an interrupt is pending. When IIR0 is cleared, an interrupt is pending.
- Bits 1 and 2: IIR1 and IIR2 identify the highest priority interrupt pending, as indicated in Table 5.
- Bit 3: IIR3 is always cleared in TL16C450 mode. This bit is set along with bit 2 in FIFO mode and when a trigger change level interrupt is pending.
- Bits 4 and 5: IIR4 and IIR5 are always cleared.
- Bits 6 and 7: IIR6 and IIR7 are set when FCR0 = 1.

PRINCIPLES OF OPERATION

line control register (LCR)

The format of the data character is controlled by the LCR. The LCR can be read. Its contents are described in the following bulleted list and shown in Figure 19.

- Bits 0 and 1: LCR0 and LCR1 are the word length select bits. The number of bits in each serial character is programmed as shown.
- Bit 2: LCR2 is the stop bit select bit. LCR2 specifies the number of stop bits in each transmitted character. The receiver always checks for one stop bit.
- Bit 3: LCR3 is the parity enable bit. When LCR3 is set, a parity bit between the last data word bit and stop bit is generated and checked.
- Bit 4: LCR4 is the even parity select bit. When LCR4 is set, even parity is enabled.
- Bit 5: LCR5 is the stick parity bit. When parity is enabled (LCR3 = 1), LCR5 = 1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR4. This forces parity to a known state and allows the receiver to check the parity bit in a known state.
- Bit 6: LCR6 is the break control bit. When LCR6 is set, the serial output (SOUT1/SOUT0) is forced to the spacing state (low). The break control bit acts only on the serial output and does not affect the transmitter logic. When the following sequence is used, no invalid characters are transmitted because of the break:

  Step 1: Load a zero byte in response to the transmitter holding register empty (THRE) status indicator.

  Step 2: Set the break in response to the next THRE status indicator.

  Step 3: Wait for the transmitter to be idle when transmitter empty status signal is set high (TEMT = 1); then clear the break when the normal transmission has to be restored.
- Bit 7: LCR7 is the divisor latch access bit (DLAB) bit. LCR7 must be set to access the divisor latches DLL and DLM of the baud rate generator during a read or write operation. LCR7 must be cleared to access the receiver buffer register, the transmitter holding register, or the interrupt enable register.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

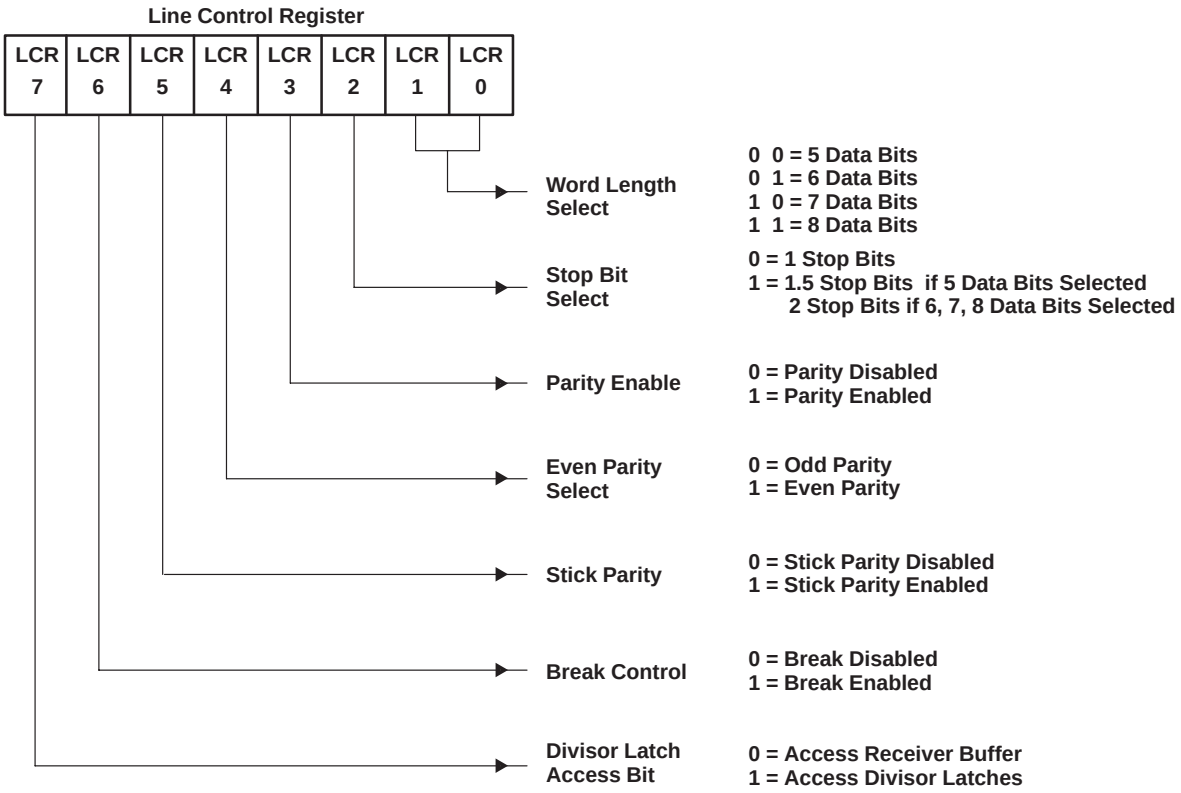


Figure 19. Line Control Register Contents

line printer port

The line printer port contains the functionality of the port included in the TL16C452 but offers a hardware programmable extended mode controlled by the printer enhancement mode (PE) terminal. This enhancement is the addition of a direction control bit and an interrupt status bit.

register 0 line printer data register

The line printer (LPT) port is either output only or bidirectional depending on the state of the extended mode terminal and data direction control bits.

Compatibility mode (PEMD = L)

Reads to the LPT data register and returns the last data that was written to the port. Write operations immediately output data to PD0–PD7.

Extended mode (PEMD = H)

Read operations return either the data last written to the LPT data register when the direction bit is cleared or return the data that is present on PD0 – PD7 when the direction is set to read. Write operations to the LPT data register latch data into the output register; however, they only drive the LPT port when the direction bit is cleared.

PRINCIPLES OF OPERATION

line printer port (continued)

Table 6 summarizes the configuration of the PD port based on the combinations of the logic level on the PEMD terminal and the value of the direction control bit (DIR).

Table 6. Extended Mode and Direction Control Bit Combinations

PEMD	DIR	PD0 – PD7 FUNCTION
L	X	PC/AT mode – output
H	0	PS/2 mode – output
H	1	PS/2 mode – input

register 1 read line printer status register

The line printer status (LPS) register is a read-only register that contains interrupt and printer status of the LPT connector terminals. Table 7 (in the default column) shows the values of each bit after reset in the case of the printer being disconnected from the port.

Table 7. LPS Register Bit Description

BIT	DESCRIPTION	DEFAULT
0	Reserved	1
1	Reserved	1
2	$\overline{\text{PRINT}}$	1
3	$\overline{\text{ERR}}$	†
4	SLCT	†
5	PE	†
6	$\overline{\text{ACK}}$	†
7	$\overline{\text{BSY}}$	†

† Outputs are dependent upon device inputs.

- Bits 0 and 1: LPS0 and LPS1 are reserved and always set.
- Bit 2: LPS2 is the printer interrupt ($\overline{\text{PRINT}}$, active low) status bit. When cleared, LPS2 indicates that the printer has acknowledged the previous transfer with an ACK handshake (if bit 4 of the control register is set). The bit is cleared on the active-to-inactive transition of the $\overline{\text{ACK}}$ signal. This bit is set after a read of the status port.
- Bit 3: $\overline{\text{ERR}}$ is the error status bit and corresponds to $\overline{\text{ERR}}$ input.
- Bit 4: SLCT is the select status bit and corresponds to SLCT input.
- Bit 5: PE is the paper empty status bit and corresponds to PE input.
- Bit 6: $\overline{\text{ACK}}$ is the acknowledge status bit corresponds to $\overline{\text{ACK}}$ input.
- Bit 7: $\overline{\text{BSY}}$ is the busy status bit and corresponds to BUSY input (active high).

PRINCIPLES OF OPERATION

register 2 line printer control register

The line printer control (LPC) register is a read/write port that controls the PD0–PD7 direction and drives the printer control lines. Write operations set or clear these bits, whereas read operations return the state of the last write operation to this register. The bits in this register are defined in Table 8 and the following bulleted list.

Table 8. LPC Register Bit Description

BIT	DESCRIPTION
0	STB
1	AFD
2	$\overline{\text{INIT}}$
3	SLIN
4	INT2 EN
5	DIR
6	Reserved 0
7	Reserved 0

- Bit 0: STB is the printer strobe control bit. When STB is set, the $\overline{\text{STB}}$ signal is asserted on the LPT interface. When STB is cleared, the $\overline{\text{STB}}$ signal is negated.
- Bit 1: AFD is the autofeed control bit. When AFD is set, the $\overline{\text{AFD}}$ signal is asserted on the LPT interface. When AFD is cleared, the signal is negated.
- Bit 2: $\overline{\text{INIT}}$ is the initialize printer control bit. When $\overline{\text{INIT}}$ is set, the $\overline{\text{INIT}}$ signal is negated. When $\overline{\text{INIT}}$ is cleared, the $\overline{\text{INIT}}$ signal is asserted on the LPT interface.
- Bit 3: SLIN is the select input control bit. When SLIN is set, the $\overline{\text{SLIN}}$ signal is asserted on the LPT interface. When SLIN is cleared, the signal is negated.
- Bit 4: INT2 EN is the interrupt request enable control bit. When set, INT2 EN enables interrupts from the LPT port. When cleared, INT2 EN disables interrupts and places INT2 signal in the high-impedance state.
- Bit 5: DIR is the direction control bit which is only used when PEMD is high. When DIR is set, the output buffers in the LPD port are disableded to allow data driven from external sources to be read from the LPD port. When DIR is cleared, the LPD port is in the output mode.
- Bits 6 and 7: These bits are reserved and are always cleared.

PRINCIPLES OF OPERATION

line status register (LSR)

The LSR is a single register that provides status indicators. The LSR bits shown in Table 9 are described in the following bulleted list.

- Bit 0: DR is the data ready bit. When set, an incoming character is received and transferred into the receiver buffer register or in the FIFO. LSR0 is cleared by a CPU read of the data in the receiver buffer register or in the FIFO.
- Bit 1: OE is the overrun error bit. An OE indicates that data in the receiver buffer register is not read by the CPU before the next character is transferred into the receiver buffer register overwriting the previous character. The OE indicator is cleared whenever the CPU reads the contents of the LSR. An overrun error occurs in FIFO mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO, but it is overwritten.
- Bit 2: PE is the parity error bit. A PE indicates that the received data character does not have the correct parity as selected by LCR3 and LCR4. The PE bit is set upon detection of a parity error and is cleared when the CPU reads the contents of the LSR. In FIFO mode, the parity error is associated with a particular character in the FIFO. LSR2 reflects the error when the character is at the top of the FIFO.
- Bit 3: FE is the framing error bit. An FE indicates that the received character does not have a valid stop bit. LSR3 is set when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is cleared when the CPU reads the contents of the LSR. In FIFO mode, the framing error is associated with a particular character in the FIFO. LSR3 reflects the error when the character is at the top of the FIFO.
- Bit 4: BI is the break interrupt bit. BI is set when the received data input is held in the spacing (low) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is cleared when the CPU reads the contents of the LSR. In FIFO mode, this is associated with a particular character in the FIFO. LSR4 reflects BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR1 – LSR4 are the error conditions that produce a receiver line status interrupt (priority 1 interrupt in the interrupt identification register) when any of the conditions are detected. This interrupt is enabled by setting IER2 in the interrupt enable register.

- Bit 5: THRE is the transmitter holding register empty bit. THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set when a character is transferred from the transmitter holding register into the transmitter shift register. LSR5 is cleared by the loading of the transmitter holding register by the CPU. LSR5 is not cleared by a CPU read of the LSR. In FIFO mode when the transmitter FIFO is empty, this bit is set. It is cleared when one byte is written to the transmitter FIFO. When the THRE interrupt is enabled by IER1, THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.
- Bit 6: TEMT is the transmitter empty bit. TEMT is set when the transmitter holding register (THR) and the transmitter shift register are both empty. LSR6 is cleared when a character is loaded into the THR and remains cleared until the character is transferred out of SOUT. TEMT is not cleared by a CPU read of the LSR. In FIFO mode, when both the transmitter FIFO and shift register are empty, TEMT is set.
- Bit 7: LSR7 is the receiver FIFO error bit. The LSR7 bit is always cleared in TL16C450 mode. In FIFO mode, it is set when at least one of the following data errors occurs in the FIFO: parity error, framing error, or break interrupt indicator. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)

NOTE:
The LSR may be written to. However, this function is intended only for factory test. It should be considered as read only by applications software.

Table 9. Line Status Register Bits

LSR BITS	1	0
LSR0 data ready (DR)	Ready	Not ready
LSR1 overrun error (OE)	Error	No error
LSR2 parity error (PE)	Error	No error
LSR3 framing error (FE)	Error	No error
LSR4 break interrupt (BI)	Break	No break
LSR5 transmitter holding register empty (THRE)	Empty	Not empty
LSR6 transmitter empty (TEMT)	Empty	Not empty
LSR7 receiver FIFO error	Error in FIFO	No error in FIFO

master reset

After power up, the ACE $\overline{\text{RESET}}$ input should be held low for one microsecond to reset the ACE circuits to an idle mode until initialization. A low on $\overline{\text{RESET}}$ causes the following:

- It initializes the transmitter and receiver clock counters.
- It clears the LSR except for transmitter shift register empty (TEMT) and transmit holding register empty (THRE), which are set. The MCR is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The LCR, divisor latches, receiver buffer register, and transmitter holding buffer register are not affected.

Following the removal of the reset condition ($\overline{\text{RESET}}$ high), the ACE remains in idle mode until programmed. A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE. A summary of the effect of a reset on the ACE is given in Table 10.

PRINCIPLES OF OPERATION

master reset (continued)

Table 10. $\overline{\text{RESET}}$ Effects on Registers and Signals

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt enable register	Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt identification register	Reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 are cleared, and bits 4–5 are permanently cleared.
Line control register	Reset	All bits are cleared.
Modem control register	Reset	All bits are cleared (5–7 permanently).
FIFO control register	Reset	All bits are cleared.
Line status register	Reset	All bits are cleared, except bits 5 and 6 are set.
Modem status register	Reset	Bits 0–3 are cleared, bits 4–7 input signal.
SOUT	Reset	High
Interrupt (RCVR errors)	Read LSR/Reset	Low
Interrupt (receiver data ready)	Read RBR/Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (modem status changes)	Read MSR/Reset	Low
$\overline{\text{OUT2}}$	Reset	High
$\overline{\text{RTS}}$	Reset	High
$\overline{\text{DTR}}$	Reset	High
$\overline{\text{OUT1}}$	Reset	High

modem control register (MCR)

The MCR controls the interface with the modem or data set as described in Figure 20. MCR can be written to and read from. The $\overline{\text{RTS}}$ and $\overline{\text{DTR}}$ outputs are directly controlled by their control bits in this register. A high input asserts a low signal (active) at the output terminals. The MCR bits are defined in the following bulleted list.

- Bit 0: When MCR0 is set, the $\overline{\text{DTR}}$ output is forced low. When MCR0 is cleared, the $\overline{\text{DTR}}$ output is forced high. The $\overline{\text{DTR}}$ output of the serial channel can be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.
- Bit 1: When MCR1 is set, the $\overline{\text{RTS}}$ output is forced low. When MCR1 is cleared, the $\overline{\text{RTS}}$ output is forced high. The $\overline{\text{RTS}}$ output of the serial channel can be input into an inverting line driver to obtain the proper polarity input at the modem or data set.
- Bit 2: MCR2 has no effect on operation.
- Bit 3: When MCR3 is set, the external serial channel interrupt is enabled.
- Bit 4: MCR4 provides a local loopback feature for diagnostic testing of the channel. When MCR4 is set, SOUT is set to the marking (high) state and the SIN is disconnected. The output of the transmitter shift register is looped back into the receiver shift register input. The four modem control inputs ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, and $\overline{\text{RI}}$) are disconnected. The modem control outputs ($\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{OUT1}}$, and $\overline{\text{OUT2}}$) are internally connected to the four modem control inputs. The modem control output terminals are forced to their inactive (high) state on the TL16C552A. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Interrupt control is fully operational; however, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external terminals represented by those four bits.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bits 5 – 7: MCR5 – MCR7 are permanently cleared.

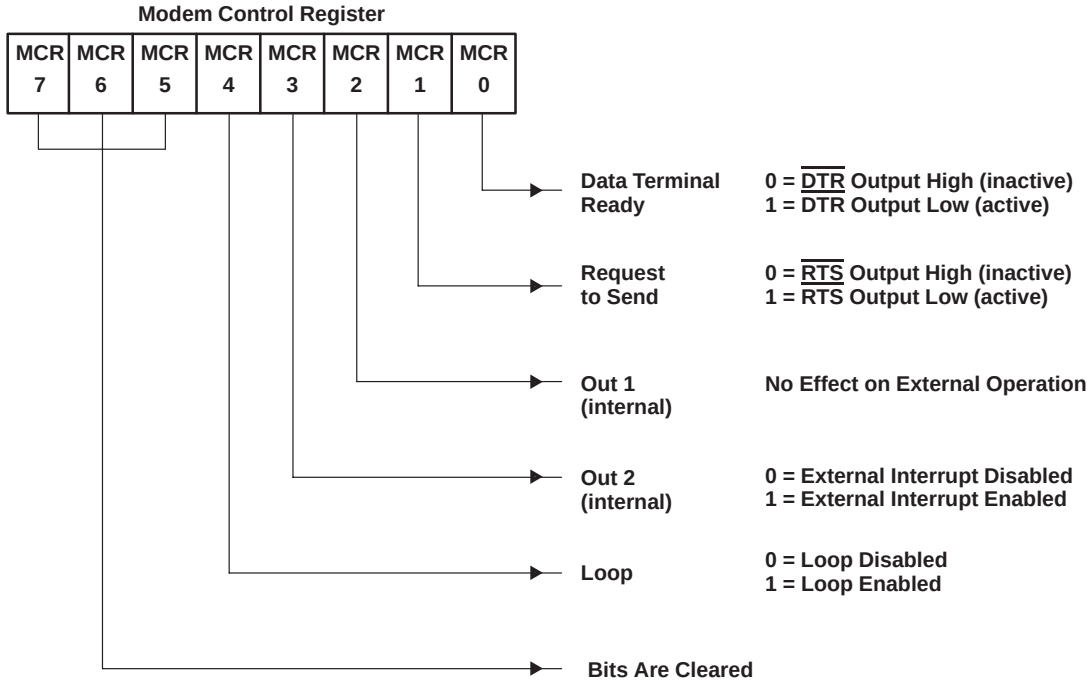


Figure 20. Modem Control Register Contents

modem status register (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs. This is done by accessing the data bus interface of the ACE in addition to the current status of four bits of the MSR. These four bits indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set when a control input from the modem changes state and are cleared when the CPU reads the MSR.

The modem input lines are $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{RI}}$, and $\overline{\text{DCD}}$. MSR4 – MSR7 are status indicators of these lines. A set status bit indicates that the input is low. A cleared status bit indicates that the input is high. When the modem status interrupt in the interrupt enable register is enabled (IER3), an interrupt is generated whenever MSR0 – MSR3 is set. The MSR is a priority-4 interrupt. The contents of the MSR are described in Table 11.

- Bit 0: MSR0 is the delta clear-to-send (ΔCTS) bit. ΔCTS displays that the $\overline{\text{CTS}}$ input to the serial channel has changed states since it was last read by the CPU.
- Bit 1: MSR1 is the delta data set ready (ΔDSR) bit. ΔDSR indicates that the $\overline{\text{DSR}}$ input to the serial channel has changed states since the last time it was read by the CPU.
- Bit 2: MSR2 is the trailing edge of the ring indicator (TERI) bit. TERI indicates that the $\overline{\text{RI}}$ input to the serial channel has changed states from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

- Bit 3: MSR3 is the delta data carrier detect (ΔDCD) bit. ΔDCD indicates that the $\overline{DCD}$ input to the serial channel has changed states since the last time it was read by the CPU.
- Bit 4: MSR4 is the clear-to-send (CTS) bit. CTS is the complement of the $\overline{CTS}$ input from the modem that indicates to the serial channel that the modem is ready to receive data from SOUT. When the serial channel is in the loop mode (MCR4 is set), MSR4 reflects the value of RTS in the MCR.
- Bit 5: MSR5 is the data set ready (DSR) bit. DSR is the complement of the $\overline{DSR}$ input from the modem to the serial channel that indicates that the modem is ready to provide received data to the serial channel receiver circuitry. When the channel is in loop mode (MCR4 is set), MSR5 reflects the value of DTR in the MCR.
- Bit 6: MSR6 is the ring indicator (RI) bit. RI is the complement of the $\overline{RI}$ input. When the channel is in loop mode (MCR4 is set), MSR6 reflects the value of $\overline{OUT1}$ in the MCR.
- Bit 7: MSR7 is the data carrier detect (DCD) bit. Data carrier detect indicates the status of the data carrier detect ($\overline{DCD}$) input. When the channel is in loop mode (MCR4 is set), MSR7 reflects the value of OUT2 in the MCR.

  Reading the MSR register clears the delta modem status indicators but has no effect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read $\overline{IOR}$ operation, the status bit is not set until the trailing edge of the read. When a status bit is set during a read operation and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again. In loop back mode, when modem status interrupts are enabled, the $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$ input terminals are ignored; however, a modem status interrupt can still be generated by writing to MCR3–MCR0. Applications software should not write to the MSR.

Table 11. Modem Status Register Bits

MSR BIT	MNEMONIC	DESCRIPTION
MSR0	ΔCTS	Delta clear to send
MSR1	ΔDSR	Delta data set ready
MSR2	TERI	Trailing edge of ring indicator
MSR3	ΔDCD	Delta data carrier detect
MSR4	CTS	Clear to send
MSR5	DSR	Data set ready
MSR6	RI	Ring indicator
MSR7	DCD	Data carrier detect

PRINCIPLES OF OPERATION

parallel port registers

The TL16C552A parallel port can connect the device to a Centronic-style printer interface. When chip select 2 ($\overline{CS2}$) is low, the parallel port is selected. Table 12 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read ($\overline{IOR}$) and write ($\overline{IOW}$) terminals as shown. The read data register allows the microprocessor to read the information on the parallel bus.

The read status register allows the microprocessor to read the status of the printer in the six most significant bits. The status bits are printer busy $\overline{BSY}$, acknowledge ($\overline{ACK}$) (a handshake function), paper empty (PE), printer selected ($\overline{SLCT}$), error ($\overline{ERR}$), and printer interrupt ($\overline{PRINT}$). The read control register allows the state of the control lines to be read. The write control register sets the state of the control lines. They are direction (DIR), interrupt enable (INT2 EN), select in ($\overline{SLIN}$), initialize the printer ($\overline{INIT}$), autofeed the paper ($\overline{AFD}$), and strobe ($\overline{STB}$), which informs the printer of the presence of a valid byte on the parallel bus. The write data register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM serial parallel adapter.

Table 12. Parallel Port Registers

REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read status	$\overline{BSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERR}$	$\overline{PRINT}$	1	1
Read control	0	0	PEMD • DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB
Write data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write control	0	0	DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB

Table 13. Parallel Port Register Select

CONTROL PINS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read data
L	H	L	L	H	Read status
L	H	L	H	L	Read control
L	H	L	H	H	Invalid
H	L	L	L	L	Write data
H	L	L	L	H	Invalid
H	L	L	H	L	Write control
H	L	L	H	H	Invalid

programmable baud rate generator

The ACE serial channel contains a programmable baud rate generator (BRG) that divides the clock (dc to 8 MHz) by any divisor from 1 to ($2^{16}-1$). The output frequency of the baud generator is 16x the data rate [divisor # = clock ÷ (baud rate x 16)], referred to in this document as RCLK. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These divisor latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 to 512 kbps are available. Tables 14, 15, 16, and 17 illustrate the divisors needed to obtain standard rates using these three frequencies.

PRINCIPLES OF OPERATION

programmable baud rate generator (continued)

Table 14. Baud Rates Using a 1.8432-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.690
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.860

Table 15. Baud Rates Using a 3.072-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.230
9600	20	–
19200	10	–
38400	5	–

PRINCIPLES OF OPERATION

programmable baud rate generator (continued)

Table 16. Baud Rates Using an 8-MHz Clock

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

Table 17. Baud Rates Using a 16-MHz Clock

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	20000	0.00
75	13334	0.00
110	9090	0.01
134.5	7434	0.01
150	6666	0.01
300	3334	–0.02
600	1666	0.04
1200	834	–0.08
1800	554	0.28
2000	500	0.00
2400	416	0.16
3600	278	–0.08
4800	208	0.16
7200	138	0.64
9600	104	0.16
19200	52	0.16
38400	26	0.16
56000	18	–0.79
128000	8	–2.34
256000	4	–2.34
512000	2	–2.34
1000000	1	0.00

PRINCIPLES OF OPERATION

programming

The serial channel of the ACE is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written to in any order, the IER should be written to last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

receiver

Serial asynchronous data is input into SIN. The ACE continually searches for a high-to-low transition from the idle state. When the transition is detected, a counter is reset and counts the 16× clock to 7 1/2, which is the center of the start bit. The start bit is valid if SIN is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low-going noise spike on the SIN input.

The LCR determines the number of data bits in a character (LCR0 and LCR1). When parity is used, LCR3 and the polarity of parity LCR4 is needed. Status for the receiver is provided in the LSR. When a full character is received, including parity and stop bits, the data received indicator in LSR0 is set. The CPU reads the receiver buffer register, which clears LSR0. If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indicator is set in LSR1. If there is a parity error, the parity error is set in LSR2. If a stop bit is not detected, a framing error indicator is set in LSR3.

If the data into SIN is a symmetrical square wave, the center of the data cells occurs within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16× clock cycle prior to being detected.

scratchpad register

The scratch register is an 8-bit read/write register that has no effect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9755001QXA	ACTIVE	CFP	HV	68	1	Non-RoHS & Non-Green	Call TI	N / A for Pkg Type	-55 to 125	5962-9755001QX A TL16C552AMHVB	Samples
TL16C552AFN	ACTIVE	PLCC	FN	68	18	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TL16C552AFN	Samples
TL16C552AFNG4	ACTIVE	PLCC	FN	68	18	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TL16C552AFN	Samples
TL16C552AFNR	ACTIVE	PLCC	FN	68	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR		TL16C552AFN	Samples
TL16C552AIFN	ACTIVE	PLCC	FN	68	18	RoHS & Green	NIPDAU	Level-3-260C-168 HR		TL16C552AIFN	Samples
TL16C552AMHV	ACTIVE	CFP	HV	68	1	Non-RoHS & Non-Green	Call TI	N / A for Pkg Type	-55 to 125	TL16C552AMHV	Samples
TL16C552AMHVB	ACTIVE	CFP	HV	68	1	Non-RoHS & Non-Green	Call TI	N / A for Pkg Type	-55 to 125	5962-9755001QX A TL16C552AMHVB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

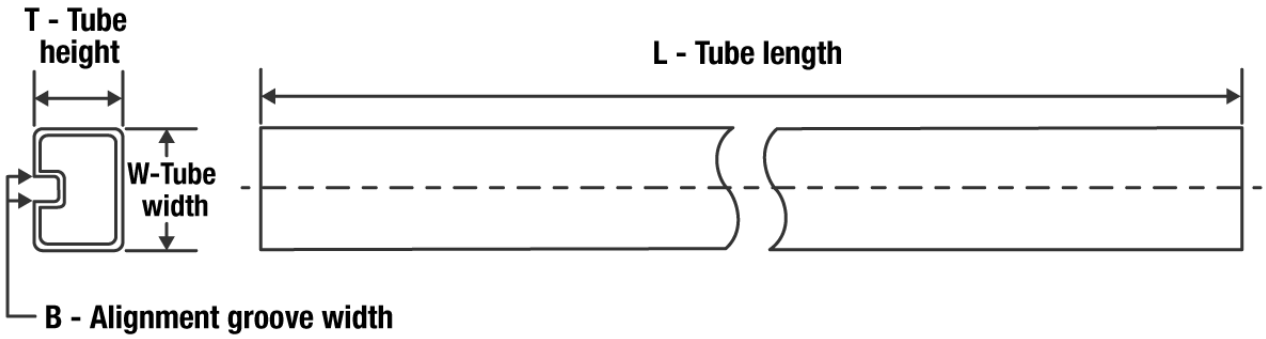
OTHER QUALIFIED VERSIONS OF TL16C552A, TL16C552AM :

- Catalog : TL16C552A
- Military : TL16C552AM

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9755001QXA	HV	CFP	68	1	506.98	17.91	12570	5.46
TL16C552AFN	FN	PLCC	68	18	506.98	25.91	5330	5.33
TL16C552AFNG4	FN	PLCC	68	18	506.98	25.91	5330	5.33
TL16C552AIFN	FN	PLCC	68	18	506.98	25.91	5330	5.33
TL16C552AMHV	HV	CFP	68	1	506.98	17.91	12570	5.46
TL16C552AMHVB	HV	CFP	68	1	506.98	17.91	12570	5.46

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