DLPC3437 Display Controller

1 Features

- Display controller for DLP3310 (.33 1080p) DMD
  - Two DLP3437 controllers drive the DLP3310 DMD
  - Supports input image sizes up to 1080p
  - Low-power DMD interface with interface training
- Input frame rates up to 120 Hz (60 Hz at 1080p resolution)
- Pixel data processing:
  - IntelliBright™ suite of image processing algorithms
    - Content adaptive illumination control (CAIC)
    - Local area brightness boost (LABB)
  - Color coordinate adjustment
  - Programmable degamma
  - Image resizing (scaling)
  - Color space conversion
- 24-bit, input pixel interface support:
  - Parallel interface protocol
  - Pixel clock up to 155 MHz
  - Multiple input pixel data format options
- Dual FPD-link input pixel interface support utilize with required FPGA:
  - LVDS interface
  - Effective pixel clock up to 155 MHz
- External flash support
- Auto DMD parking at power down
- Embedded frame memory (eDRAM)
- System features:
  - I^2C control of device configuration
  - Programmable splash screens
  - Programmable LED current control
  - One frame latency
- Pair with DLPA3000 or DLPA3005 PMIC (power management integrated circuit) and LED driver

2 Applications

- DLP signage
- Mobile projector
- Mobile smart TV
- Smart home displays
- Pico projectors

3 Description

The DLPC3437 digital controller, part of the DLP3310 (.33 1080p) chipset, supports reliable operation of the DLP3310 digital micromirror device (DMD). The DLPC3437 controller provides a convenient, multifunctional interface between system electronics and the DMD, enabling small form factor, low power, and high resolution full HD displays.

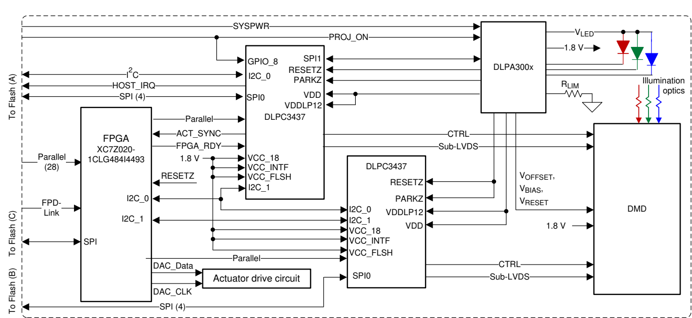
Visit the getting started with TI DLP®Pico™ display technology page, and view the programmer's guide to learn how to get started.

The chipsets include established resources to help the user accelerate the design cycle, which include production ready optical modules, optical module manufacturers, and design houses.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DLPC3437	NFBGA (201)	13.00 mm × 13.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Simplified System

Table of Contents

4 Revision History

Changes from Revision C (June 2019) to Revision D (August 2021)	Page
• General datasheet formatting and ordering refresh	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.	1
• Globally changed instances of legacy terminology to primary and secondary where I^2C or SPI is mentioned.	1
• Deleted mention of mirror parking time from PARKZ pin description and moved to a specification table	4
• Changed JTAG pin names from Reserved to proper names	4
• Deleted support for adjustable DATAEN_CMD polarity	4
• Deleted support for adjusting PCLK capture edge in software	4
• Added DSI pin information	4
• Changed the description of how to use the CMP_OUT pin and corrected how the comparator must use GPIO_10 (RC_CHARGE) instead of CMP_PWM	4
• Deleted support for CMP_PWM	4
• Deleted mention of unsupported light sensor on GPIO_13 and GPIO_12	4
• Deleted reference of the LS_PWR circuit being used for the light sensor	4
• Deleted mention of the unsupported LABB output sample and hold sensor control signal	4
• Clarified GPIO_03 - GPIO_01 pins are required to be used as a SPI1 port	4
• Deleted unneeded VCC_INTF and VCC_FLSH absolute maximum values	12
• Changed Updated VDDLP12 information	13
• Changed incorrect pin tolerance	13
• Changed and fixed incorrect test conditions for current drive strengths	15
• Deleted redundant $\|V_{OD}\|$ specification which is referenced in later sections	15
• Added minimum and maximum values for V_{OH} for I/O type 4	15
• Added minimum and maximum values for V_{OL} for I/O type 4	15

Changes from Revision B (January 2018) to Revision C (June 2019) **Page**

5 Pin Configuration and Functions

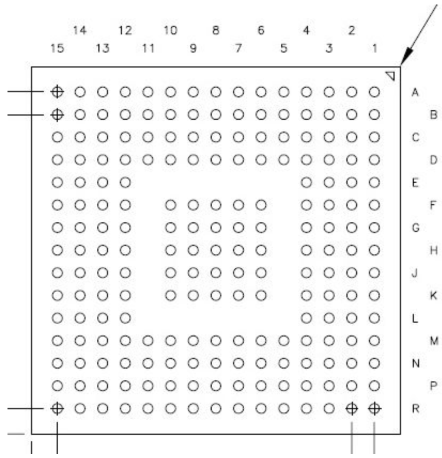


Figure 5-1. ZEZ Package 201-Pin NFBGA Bottom View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DMD_LS_CLK	DMD_LS_WDATA	DMD_HS_WDATAH_P	DMD_HS_WDATAG_P	DMD_HS_WDATAF_P	DMD_HS_WDATAE_P	DMD_HS_CLK_P	DMD_HS_WDATAD_P	DMD_HS_WDATAC_P	DMD_HS_WDATAB_P	DMD_HS_WDATAA_P	CMP_OUT	SPI0_CLK	SPI0_CSZ0	CMP_PWM
B	DMD_DEN_ARSTZ	DMD_LS_RDATA	DMD_HS_WDATAH_N	DMD_HS_WDATAG_N	DMD_HS_WDATAF_N	DMD_HS_WDATAE_N	DMD_HS_CLK_N	DMD_HS_WDATAD_N	DMD_HS_WDATAC_N	DMD_HS_WDATAB_N	DMD_HS_WDATAA_N	SPI0_DIN	SPI0_DOUT	LED_SEL_1	LED_SEL_0
C	NC	NC	VDDLP12	VSS	VDD	VSS	VCC	VSS	VCC	HWTEST_EN	RESETZ	SPI0_CSZ1	PARKZ	GPIO_00	GPIO_01
D	NC	NC	VDD	VCC	VDD	VSS	VDD	VSS	VDD	VSS	VCC_FLSH	VDD	VDD	GPIO_02	GPIO_03
E	NC	NC	VDD	VSS								VCC	VSS	GPIO_04	GPIO_05
F	NC	NC	RREF	VSS		VSS	VSS	VSS	VSS	VSS		VCC	VDD	GPIO_06	GPIO_07
G	NC	NC	VSS_PLLM	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VSS	GPIO_08	GPIO_09
H	PLL_REFCLK_I	VDD_PLLM	VSS_PLLD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VDD	GPIO_10	GPIO_11
J	PLL_REFCLK_O	VDD_PLLD	VSS	VDD		VSS	VSS	VSS	VSS	VSS		VDD	VSS	GPIO_12	GPIO_13
K	PDATA_1	PDATA_0	VDD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VCC	GPIO_14	GPIO_15
L	PDATA_3	PDATA_2	VSS	VDD								VDD	VDD	GPIO_16	GPIO_17
M	PDATA_5	PDATA_4	VCC_INTF	VSS	VSS	VDD	VCC_INTF	VSS	VDD	VDD	VCC	VSS	JTAGTMS1	GPIO_18	GPIO_19
N	PDATA_7	PDATA_6	VCC_INTF	PDM_CVS_TE	HSYNC_CS	3DR	VCC_INTF	HOST_IRQ	IIC0_SDA	IIC0_SCL	JTAGTMS2	JTAGTDO2	JTAGTDO1	TSTPT_6	TSTPT_7
P	VSYNC_WE	DATEN_CMD	PCLK	PDATA_11	PDATA_13	PDATA_15	PDATA_17	PDATA_19	PDATA_21	PDATA_23	JTAGTRSTZ	JTAGTCK	JTAGTDI	TSTPT_4	TSTPT_5
R	PDATA_8	PDATA_9	PDATA_10	PDATA_12	PDATA_14	PDATA_16	PDATA_18	PDATA_20	PDATA_22	IIC1_SDA	IIC1_SCL	TSTPT_0	TSTPT_1	TSTPT_2	TSTPT_3

Note: The lower image view is from the top.

Table 5-1. Test Pins and General Control

PIN		I/O	TYPE[4]	DESCRIPTION
NAME	NO.			
HWTEST_EN	C10	I	6	Manufacturing test enable signal. Connect this signal directly to ground on the PCB for normal operation.
PARKZ	C13	I	6	DMD fast park control (active low Input with a hysteresis buffer). This signal is used to quickly park the DMD when loss of power is imminent. The longest lifetime of the DMD may not be achieved with the fast park operation, therefore, this signal is intended to only be asserted when a normal park operation is unable to be completed. The PARKZ signal is typically provided from the DLPAxxxx interrupt output signal.
JTAGTCK	P12	I	6	TI internal use. Leave this pin unconnected.
JTAGTDI	P13	I	6	TI internal use. Leave this pin unconnected.
JTAGTDO1	N13[1]	O	1	TI internal use. Leave this pin unconnected.
JTAGTDO2	N12[1]	O	1	TI internal use. Leave this pin unconnected.
JTAGTMS1	M13	I	6	TI internal use. Leave this pin unconnected.
JTAGTMS2	N11	I	6	TI internal use. Leave this pin unconnected.
JTAGTRSTZ	P11	I	6	TI internal use. This pin must be tied to ground, through an external resistor for normal operation. Failure to tie this pin low during normal operation can cause start-up and initialization problems.[2]
RESETZ	C11	I	6	Power-on reset (active low input with a hysteresis buffer). Self-configuration starts when a low-to-high transition is detected on RESETZ. All controller power and clocks must be stable before this reset is de-asserted. No signals are in their active state while RESETZ is asserted. This pin is typically connected to the RESET_Z pin of the DLPA300x.
TSTPT_0	R12	I/O	1	Test pins (includes weak internal pulldown). Pins are tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ, and then driven as outputs.[2] [3] Normal use: reserved for test output. Leave open for normal use. Note: An external pullup may put the DLPC3437 in a test mode. See Section 7.3.8 for more information.
TSTPT_1	R13	I/O	1	
TSTPT_2	R14	I/O	1	
TSTPT_3	R15	I/O	1	
TSTPT_4	P14	I/O	1	
TSTPT_5	P15	I/O	1	
TSTPT_6	N14	I/O	1	
TSTPT_7	N15	I/O	1	

(1) If the application design does not require an external pullup, and there is no external logic that can overcome the weak internal pulldown resistor, then this I/O pin can be left open or unconnected for normal operation. If the application design does not require an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown is recommended to ensure a logic low.
(2) External resistor must have a value of 8 kΩ or less to compensate for pins that provide internal pullup or pulldown resistors.
(3) If the application design does not require an external pullup and there is no external logic that can overcome the weak internal pulldown, then the TSTPT I/O can be left open (unconnected) for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.
(4) See Table 5-10 for type definitions.

Table 5-2. Parallel Port Input

PIN		I/O	TYPE[4]	DESCRIPTION
NAME[1] [2]	NO.			PARALLEL RGB MODE
PCLK	P3	I	10	Pixel clock
PDM_CVS_TE	N4	I/O	5	Parallel data mask. Programable polarity with default of active high. Optional signal.
VSYNC_WE	P1	I	10	Vsync[3]
HSYNC_CS	N5	I	10	Hsync[3]
DATAEN_CMD	P2	I	10	Data valid
PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	K2 K1 L2 L1 M2 M1 N2 N1	I	10	**(TYPICAL RGB 888)** Blue (bit weight 1) Blue (bit weight 2) Blue (bit weight 4) Blue (bit weight 8) Blue (bit weight 16) Blue (bit weight 32) Blue (bit weight 64) Blue (bit weight 128)
PDATA_8 PDATA_9 PDATA_10 PDATA_11 PDATA_12 PDATA_13 PDATA_14 PDATA_15	R1 R2 R3 P4 R4 P5 R5 P6	I	10	**(TYPICAL RGB 888)** Green (bit weight 1) Green (bit weight 2) Green (bit weight 4) Green (bit weight 8) Green (bit weight 16) Green (bit weight 32) Green (bit weight 64) Green (bit weight 128)
PDATA_16 PDATA_17 PDATA_18 PDATA_19 PDATA_20 PDATA_21 PDATA_22 PDATA_23	R6 P7 R7 P8 R8 P9 R9 P10	I	10	**(TYPICAL RGB 888)** Red (bit weight 1) Red (bit weight 2) Red (bit weight 4) Red (bit weight 8) Red (bit weight 16) Red (bit weight 32) Red (bit weight 64) Red (bit weight 128)
3DR	N6	I	10	3D reference • For 3D applications: left or right 3D reference (left = 1, right = 0). To be provided by the host. Must transition in the middle of each frame (no closer than 1 ms to the active edge of VSYNC) • If a 3D application is not used, pull this input low through an external resistor.

(1) PDATA(23:0) bus mapping depends on pixel format and source mode. See later sections for details.
(2) Connect unused inputs to ground or pulldown to ground through an external resistor (8 kΩ or less).
(3) VSYNC and HSYNC polarity can be adjusted by software.
(4) See Table 5-10 for type definitions.

Table 5-3. DSI Input Data and Clock

PIN		I/O	TYPE(1)	DESCRIPTION
NAME	NO.			
DCLKN DCLKP	E2 E1			Unused; leave unconnected and floating.
DD0N DD0P DD1N DD1P DD2N DD2P DD3N DD3P	G2 G1 F2 F1 D2 D1 C2 C1			
RREF	F3	—		

(1) See Table 5-10 for type definitions.

Table 5-4. DMD Reset and Bias Control

PIN		I/O	TYPE(1)	DESCRIPTION
NAME	NUMBER			
DMD_DEN_ARSTZ	B1	O	2	DMD driver enable (active high). DMD reset (active low). When corresponding I/O power is supplied, the controller drives this signal low after the DMD is parked and before power is removed from the DMD. If the 1.8-V power to the DLPC3437 is independent of the 1.8-V power to the DMD, then TI recommends including a weak, external pulldown resistor to hold the signal low in case DLPC3437 power is inactive while DMD power is applied.
DMD_LS_CLK	A1	O	3	DMD, low speed interface clock
DMD_LS_WDATA	A2	O	3	DMD, low speed serial write data
DMD_LS_RDATA	B2	I	6	DMD, low speed serial read data

(1) See Table 5-10 for type definitions.

Table 5-5. DMD Sub-LVDS Interface

PIN		I/O	TYPE(1)	DESCRIPTION
NAME	NUMBER			
DMD_HS_CLK_P DMD_HS_CLK_N	A7 B7	O	4	DMD high speed interface
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	A3 B3 A4 B4 A5 B5 A6 B6 A8 B8 A9 B9 A10 B10 A11 B11	O	4	DMD sub-LVDS high speed (HS) interface write data lanes. The true numbering and application of the DMD_HS_WDATA pins depend on the software configuration. See Table 7-8.

(1) See Table 5-10 for type definitions.

Table 5-6. Peripheral Interface

PIN		I/O	TYPE[3]	DESCRIPTION
NAME[1]	NO.			
CMP_OUT	A12	I	6	Successive approximation ADC (analog-to-digital converter) comparator output (DLPC3437 Input). To implement, use a successive approximation ADC (DLPAxxxx) with a thermistor feeding one input of the external comparator and the DLPC3437 controller GPIO_10 (RC_CHARGE) pin driving the other side of the comparator. CMP_OUT must be pulled down to ground if this function is not used. (hysteresis buffer).
CMP_PWM	A15	O	1	TI internal use. Leave this pin unconnected.
HOST_IRQ[2]	N8	O	9	Host interrupt (output) HOST_IRQ indicates when the DLPC3437 auto-initialization is in progress and most importantly, when it completes. This pin is tri-stated during reset. An external pullup must be included on this signal.
IIC0_SCL[4]	N10	I/O	7	I^{2}C target (port 0) SCL (bidirectional, open-drain signal with input hysteresis): This pin requires an external pullup resistor. The target I^{2}C I/Os are 3.6-V tolerant (high-voltage-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^{2}C pullups must be connected to a host supply with an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage does not typically satisfy the V_{IH} specification of the target I^{2}C input buffers).
IIC1_SCL	R11	I/O	8	TI internal use. TI recommends an external pullup resistor.
IIC0_SDA[4]	N9	I/O	7	I^{2}C target (port 0) SDA. (bidirectional, open-drain signal with input hysteresis): This pin requires an external pullup resistor. The target I^{2}C port is the control port of controller. The target I^{2}C I/O pins are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^{2}C pullups must be connected to a host supply with an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage does not typically satisfy the V_{IH} specification of the target I^{2}C input buffers).
IIC1_SDA	R10	I/O	8	TI internal use. TI recommends an external pullup resistor.
LED_SEL_0	B15	O	1	LED enable select. Automatically controlled by the DLPC3437 programmable DMD sequence LED_SEL(1:0) — Enabled LED 00 — None 01 — Red 10 — Green 11 — Blue
LED_SEL_1	B14	O	1	The controller drives these signals low when RESETZ is asserted and the corresponding I/O power is supplied. The controller continues to drive these signals low throughout the auto-initialization process. A weak, external pulldown resistor is recommended to ensure that the LEDs are disabled when I/O power is not applied.
SPI0_CLK	A13	O	13	SPI (Serial Peripheral Interface) port 0, clock. This pin is typically connected to the flash memory clock.
SPI0_CSZ0	A14	O	13	SPI port 0, chip select 0 (active low output). This pin is typically connected to the flash memory chip select. TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during controller reset assertion.
SPI0_CSZ1	C12	O	13	SPI port 0, chip select 1 (active low output). This pin typically remains unused. TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during controller reset assertion.
SPI0_DIN	B12	I	12	Synchronous serial port 0, receive data in. This pin is typically connected to the flash memory data out.
SPI0_DOUT	B13	O	13	Synchronous serial port 0, transmit data out. This pin is typically connected to the flash memory data in.

(1) External pullup resistor must be 8 kΩ or less.
(2) For more information about usage, see Section 7.3.2.
(3) See Table 5-10 for type definitions.

(4) When VCC_INTF is powered and VDD is not powered, the controller may drive the IIC0_xxx pins low which prevents communication on this I^2C bus. Do not power up the VCC_INTF pin before powering up the VDD pin for any system that has additional target devices on this bus.

Table 5-7. GPIO Peripheral Interface

PIN(1)		I/O	TYPE(1) (3)	DESCRIPTION(2)
NAME	NO.			
GPIO_19	M15	I/O	1	HBT_ODAT (Output): Connect to the HBT_IDAT (GPIO_17) pin of the second DLPC3437.
GPIO_18	M14	I/O	1	HBT_OCLK (Output): Connect to the HBT_ICLK (GPIO_16) pin of the second DLPC3437.
GPIO_17	L15	I/O	1	HBT_IDAT (Input): Connect to the HBT_ODAT (GPIO_19) pin of the second DLPC3437.
GPIO_16	L14	I/O	1	HBT_ICLK (Input): Connect to the HBT_OCLK (GPIO_18) pin of the second DLPC3437.
GPIO_15	K15	I/O	1	DA_SYNC (BiDir): Connect to the DA_SYNC (GPIO_15) pin of the second DLPC3437.
GPIO_14	K14	I/O	1	SEQ_SYNC (BiDir): Connect to the SEQ_SYNC (GPIO_14) pin of the second DLPC3437 with a 7.87k pullup resistor to VCC18.
GPIO_13	J15	I/O	1	General purpose I/O 13 (hysteresis buffer). Optional GPIO. If unused, TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise, this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_12	J14	I/O	1	General purpose I/O 12 (hysteresis buffer). Optional GPIO. If unused, TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise, this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_11	H15	I/O	1	General purpose I/O 11 (hysteresis buffer). Options: 1. Thermistor power enable (output). Turns on the power to the thermistor when it is used and enabled. 2. Optional GPIO. If unused, TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise, this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_10	H14	I/O	1	General Purpose I/O 10 (hysteresis buffer). Options: 1. RC_CHARGE (output): Intended to feed the RC charge circuit of the thermistor interface. 2. Optional GPIO. If unused, TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise, this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_09	G15	I/O	1	General purpose I/O 09 (hysteresis buffer). Optional GPIO. If unused, TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise, this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_08	G14	I/O	1	General purpose I/O 08 (hysteresis buffer). Normal mirror parking request (active low): To be driven by the PROJ_ON output of the host. A logic low on this signal causes the DLPC3437 to PARK the DMD, but it does not power down the DMD (the DLPAxxxx does that instead). The minimum high time is 200 ms. The minimum low time is 200 ms.
GPIO_07	F15	I/O	1	General purpose I/O 07 (hysteresis buffer). If unused, TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise, this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_06	F14	I/O	1	General purpose I/O 06 (hysteresis buffer). Optional GPIO. If unused, TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise, this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_05	E15	I/O	1	General purpose I/O 05 (hysteresis buffer). Optional GPIO. If unused, TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise, this pin requires an external pullup or pulldown to avoid a floating GPIO input.
GPIO_04	E14	I/O	1	MST_SLVZ (Input): Primary or secondary controller identifier signal (Primary = 1, Secondary = 0).
GPIO_03	D15	I/O	1	General purpose I/O 03 (hysteresis buffer). SPI1_CSZ0 (active low output): SPI1 chip select 0 signal. This pin is typically connected to the DLPAxxxx SPI_CSZ pin. Requires an external pullup resistor to deactivate this signal during reset and auto-initialization processes.
GPIO_02	D14	I/O	1	General purpose I/O 02 (hysteresis buffer). SPI1_DOUT (output): SPI1 data output signal. This pin is typically connected to the DLPAxxxx SPI_DIN pin.
GPIO_01	C15	I/O	1	General purpose I/O 01 (hysteresis buffer). SPI1_CLK (output): SPI1 clock signal. This pin is typically connected to the DLPAxxxx SPI_CLK pin.

Table 5-7. GPIO Peripheral Interface (continued)

PIN[(1)]		I/O	TYPE[(1)] [(3)]	DESCRIPTION[(2)]
NAME	NO.			
GPIO_00	C14	I/O	1	General purpose I/O 00 (hysteresis buffer). SPI1_DIN (input): SPI1 data input signal. This pin is typically connected to the DLPAxxxx SPI_DOUT pin.

(1) GPIO pins must be configured through software for input, output, bidirectional, or open-drain operation. Some GPIO pins have one or more alternative use modes, which are also software configurable. An external pullup resistor is required for each signal configured as open-drain.
(2) General purpose I/O for the DLPC3437 controller. These GPIO pins are software configurable.
(3) See Table 5-10 for type definitions.

Table 5-8. Clock and PLL Support

PIN		I/O	TYPE[(1)]	DESCRIPTION
NAME	NUMBER			
PLL_REFCLK_I	H1	I	11	Reference clock crystal input. If an external oscillator is used in place of a crystal, this pin is the oscillator input.
PLL_REFCLK_O	J1	O	5	Reference clock crystal return. If an external oscillator is used in place of a crystal, leave this pin unconnected (that is floating with no added capacitive load).

(1) See Table 5-10 for type definitions.

Table 5-9. Power and Ground

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDD	C5, D5, D7, D12, J4, J12, K3, L4, L12, M6, M9, D9, D13, F13, H13, L13, M10, D3, E3	—	PWR	Core 1.1-V power (main 1.1 V)
VDDLP12	C3	—	PWR	Reserved – tie to the VDD rail
VSS	C4, D6, D8, D10, E4, E13, F4, G4, G12, H4, H12, J3, J13, K4, K12, L3, M4, M5, M8, M12, G13, C6, C8, F6, F7, F8, F9, F10, G6, G7, G8, G9, G10, H6, H7, H8, H9, H10, J6, J7, J8, J9, J10, K6, K7, K8, K9, K10	—	GND	Core ground (eDRAM, I/O ground, thermal ground)
VCC18	C7, C9, D4, E12, F12, K13, M11	—	PWR	All 1.8-V I/O power: 1.8-V power supply for all I/O pins (RESETZ, PARKZ, LED_SEL, CMP_OUT, GPIO, IIC1, TSTPT, and JTAG) except the host or parallel interface and the SPI flash interface.
VCC_INTF	M3, M7, N3, N7	—	PWR	Host or parallel interface I/O power: 1.8 V to 3.3 V (Includes IIC0, PDATA, video syncs, and HOST_IRQ pins)
VCC_FLSH	D11	—	PWR	Flash interface I/O power: 1.8 V to 3.3 V (Dedicated SPI0 power pin)

Table 5-9. Power and Ground (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDD_PLLM	H2	—	PWR	MCG PLL (primary clock generator phase lock loop) 1.1-V power
VSS_PLLM	G3	—	RTN	MCG PLL return
VDD_PLLD	J2	—	PWR	DCG PLL (DMD clock generator phase lock loop) 1.1-V power
VSS_PLLD	H3	—	RTN	DCG PLL return

Table 5-10. I/O Type Subscript Definition

I/O		SUPPLY REFERENCE	ESD STRUCTURE
SUBSCRIPT	DESCRIPTION		
1	1.8-V LVCMOS I/O buffer with 8-mA drive	V_{cc18}	ESD diode to GND and supply rail
2	1.8-V LVCMOS I/O buffer with 4-mA drive	V_{cc18}	ESD diode to GND and supply rail
3	1.8-V LVCMOS I/O buffer with 24-mA drive	V_{cc18}	ESD diode to GND and supply rail
4	1.8-V sub-LVDS output with 4-mA drive	V_{cc18}	ESD diode to GND and supply rail
5	1.8-V, 2.5-V, 3.3-V LVCMOS with 4-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
6	1.8-V LVCMOS input	V_{cc18}	ESD diode to GND and supply rail
7	1.8-V, 2.5-V, 3.3-V I^2C with 3-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
8	1.8-V I^2C with 3-mA drive	V_{cc18}	ESD diode to GND and supply rail
9	1.8-V, 2.5-V, 3.3-V LVCMOS with 8-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
10	Reserved		
11	1.8-V, 2.5-V, 3.3-V LVCMOS input	V_{cc_INTF}	ESD diode to GND and supply rail
12	1.8-V, 2.5-V, 3.3-V LVCMOS input	V_{cc_FLSH}	ESD diode to GND and supply rail
13	1.8-V, 2.5-V, 3.3-V LVCMOS with 8-mA drive	V_{cc_FLSH}	ESD diode to GND and supply rail

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

		MIN	MAX	UNIT
SUPPLY VOLTAGE[2]				
$V_{(VDD)}$		–0.3	1.21	V
$V_{(VDDLP12)}$		–0.3	1.32	V
$V_{(VCC18)}$		–0.3	1.96	V
DMD sub-LVDS interface (DMD_HS_CLK_x and DMD_HS_WDATA_x_y)		–0.3	1.96	V
$V_{(VCC\_INTF)}$		–0.3	3.60	V
$V_{(VCC\_FLSH)}$		–0.3	3.60	V
$V_{(VDD\_PLLM)}$ (MCG PLL)		–0.3	1.21	V
$V_{(VDD\_PLLD)}$ (DCG PLL)		–0.3	1.21	V
$V_{I2C\ buffer}$ (I/O type 7)		–0.3	See [3]	V
GENERAL				
T_J	Operating junction temperature	–30	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under Section 6.1 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Section 6.3. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VSS (GND).
(3) I/O is high voltage tolerant; that is, if VCC_INTF = 1.8 V, the input is 3.3-V tolerant, and if VCC_INTF = 3.3 V, the input is 5-V tolerant.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(VDD)}$	Core power 1.1 V (main 1.1 V)		1.045	1.10	1.155	V
$V_{(VDDLP12)}$	Reserved	See[3]	1.045	1.10	1.155	V
$V_{(VCC18)}$	All 1.8-V I/O power: 1.8-V power supply for all I/O pins (RESETZ, PARKZ LED_SEL, CMP_OUT, GPIO, IIC1, TSTPT, and JTAG) except the host or parallel interface and the SPI flash interface.		1.64	1.80	1.96	V
$V_{(VCC\_INTF)}$	Host or parallel interface I/O power: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	See [1]	1.64	1.80	1.96	V
			2.28	2.50	2.72	
			3.02	3.30	3.58	
$V_{(VCC\_FLSH)}$	Flash interface I/O power: 1.8 V to 3.3 V	See [1]	1.64	1.80	1.96	V
			2.28	2.50	2.72	
			3.02	3.30	3.58	
$V_{(VDD\_PLLM)}$	MCG PLL 1.1-V power	See [2]	1.025	1.100	1.155	V
$V_{(VDD\_PLLD)}$	DCG PLL 1.1-V power	See [2]	1.025	1.100	1.155	V
T_A	Operating ambient temperature [4]		–30		85	°C
T_J	Operating junction temperature		–30		105	°C

(1) These supplies have multiple valid ranges.
(2) The minimum voltage is lower than other 1.1-V supply minimum to enable additional filtering. This filtering may result in an IR drop across the filter.
(3) VDDLP12 must be tied to the VDD rail.
(4) The operating ambient temperature range assumes 0 forced air flow, a JEDEC JESD51 junction-to-ambient thermal resistance value at 0 forced air flow ($R_{θJA}$ at 0 m/s), a JEDEC JESD51 standard test card and environment, along with minimum and maximum estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, and this affects $R_{θJA}$. Thus, maximum operating ambient temperature varies by application.
- $T_{a\_min} = T_{j\_min} – (P_{d\_min} × R_{θJA})$ = –30°C – (0.0 W × 28.8°C/W) = –30°C
- $T_{a\_max} = T_{j\_max} – (P_{d\_max} × R_{θJA})$ = +105°C – (0.348 W × 28.8°C/W) = +95.0°C

6.4 Thermal Information

THERMAL METRIC[1]			DLPC3437 ZEZ (NFBGA) 201 PINS	UNIT
$R_{θJC}$	Junction-to-case top thermal resistance		10.1	°C/W
$R_{θJA}$	Junction-to-air thermal resistance	at 0 m/s of forced airflow[2]	28.8	°C/W
		at 1 m/s of forced airflow[2]	25.3	
		at 2 m/s of forced airflow[2]	24.4	
$Ψ_{JT}$	Temperature variance from junction to package top center temperature, per unit power dissipation[3]		0.23	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{θJA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC34xx PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance.
(3) Example: (0.5 W) × (0.2 °C/W) ≈ 0.1°C temperature rise.

6.5 Power Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER[(1) (2) (3)]		TEST CONDITIONS	MIN	TYP[(4)]	MAX[(5)]	UNIT
$I_{(VDD)}$ + $I_{(VDD\_PLLM)}$ + $I_{(VDD\_PLLD)}$	1.1V rails	Frame rate = 50 Hz input=1920x1080 to FPGA		196	330	mA
		Frame rate = 60 Hz input=1920x1080 to FPGA		216	347	
$I_{(VDD\_PLLM)}$	MCG PLL 1.1-V current	Frame rate = 50 Hz input=1920x1080 to FPGA		6		mA
		Frame rate = 60 Hz input=1920x1080 to FPGA		6		
$I_{(VDD\_PLLD)}$	DCG PLL 1.1-V current	Frame rate = 50 Hz input=1920x1080 to FPGA		6		mA
		Frame rate = 60 Hz input=1920x1080 to FPGA		6		
$I_{(VCC18)}$	All 1.8-V I/O current: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface)	Frame rate = 50 Hz input=1920x1080 to FPGA		31	45	mA
		Frame rate = 60 Hz input=1920x1080 to FPGA		31	45	
$I_{(VCC\_INTF)}$	Host or parallel interface I/O current: 1.8 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	Frame rate = 50 Hz input=1920x1080 to FPGA		2		mA
		Frame rate = 60 Hz input=1920x1080 to FPGA		2		
$I_{(VCC\_FLSH)}$	Flash interface I/O current:1.8 to 3.3 V	Frame rate = 50 Hz input=1920x1080 to FPGA		1		mA
		Frame rate = 60 Hz input=1920x1080 to FPGA		1		

(1) Values assume all pins using 1.1 V are tied together (including VDDLP12), and programmable host and flash I/O are at the minimum nominal voltage (that is 1.8 V).
(2) Input image is 1920 x 1080 (1080p) 24-bits using VESA reduced blanking v2 timings on the parallel interface at the frame rate shown with the 0.33-inch 1080p (DLP3310) DMD. The controller has the CAIC and LABB algorithms turned off.
(3) The values do not take into account software updates or customer changes that may affect power performance.
(4) Assumes nominal process, voltage, and temperature (25°C nominal ambient) with nominal input images.
(5) Assumes worst case process, maximum voltage, and high nominal ambient temperature of 65°C with worst case input image.

6.6 Pin Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER(3)			TEST CONDITIONS(4)	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	I²C buffer (I/O type 7)		0.7 × VCC_INTF		See (1)	V
		I/O type 1, 2, 3, 6, 8 except pins noted in (2)	VCC18 = 1.8 V	1.17		3.6	
		I/O type 1, 6 for pins noted in (2)	VCC18 = 1.8 V	1.3		3.6	
		I/O type 5, 9, 11	VCC_INTF = 1.8 V	1.17		3.6	
		I/O type 12, 13	VCC_FLSH = 1.8 V	1.17		3.6	
		I/O type 5, 9, 11	VCC_INTF = 2.5 V	1.7		3.6	
		I/O type 12, 13	VCC_FLSH = 2.5 V	1.7		3.6	
		I/O type 5, 9, 11	VCC_INTF = 3.3 V	2.0		3.6	
		I/O type 12, 13	VCC_FLSH = 3.3 V	2.0		3.6	
V_{IL}	Low-level input threshold voltage	I²C buffer (I/O type 7)		–0.5		0.3 × VCC_INTF	V
		I/O type 1, 2, 3, 6, 8 except pins noted in (2)	VCC18 = 1.8 V	–0.3		0.63	
		I/O type 1, 6 for pins noted in (2)	VCC18 = 1.8 V	–0.3		0.5	
		I/O type 5, 9, 11	VCC_INTF = 1.8 V	–0.3		0.63	
		I/O type 12, 13	VCC_FLSH = 1.8 V	–0.3		0.63	
		I/O type 5, 9, 11	VCC_INTF = 2.5 V	–0.3		0.7	
		I/O type 12, 13	VCC_FLSH = 2.5 V	–0.3		0.7	
		I/O type 5, 9, 11	VCC_INTF = 3.3 V	–0.3		0.8	
		I/O type 12, 13	VCC_FLSH = 3.3 V	–0.3		0.8	
V_{OH}	High-level output voltage	I/O type 1, 2, 3, 6, 8	VCC18 = 1.8 V	1.35			V
		I/O type 5, 9, 11	VCC_INTF = 1.8 V	1.35			
		I/O type 12, 13	VCC_FLSH = 1.8 V	1.35			
		I/O type 5, 9, 11	VCC_INTF = 2.5 V	1.7			
		I/O type 12, 13	VCC_FLSH = 2.5 V	1.7			
		I/O type 5, 9, 11	VCC_INTF = 3.3 V	2.4			
		I/O type 12, 13	VCC_FLSH = 3.3 V	2.4			
V_{OL}	Low-level output voltage	I²C buffer (I/O type 7)	VCC_INTF > 2 V			0.4	V
		I²C buffer (I/O type 7)	VCC_INTF < 2 V			0.2 × VCC_INTF	
		I/O type 1, 2, 3, 6, 8	VCC18 = 1.8 V			0.45	
		I/O Type 5, 9, 11	VCC_INTF = 1.8 V			0.45	
		I/O Type 12, 13	VCC_FLSH = 1.8 V			0.45	
		I/O Type 5, 9, 11	VCC_INTF = 2.5 V			0.7	
		I/O Type 12, 13	VCC_FLSH = 2.5 V			0.7	
		I/O Type 5, 9, 11	VCC_INTF = 3.3 V			0.4	
		I/O Type 12, 13	VCC_FLSH = 3.3 V			0.4	

6.6 Pin Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER[3]			TEST CONDITIONS[4]	MIN	TYP	MAX	UNIT
I_{OH}	High-level output current[5]	I/O type 2, 4	VCC18 = 1.8 V	2			mA
		I/O type 5	VCC_INTF = 1.8 V	2			
		I/O type 1	VCC18 = 1.8 V	3.5			
		I/O type 9	VCC_INTF = 1.8 V	3.5			
		I/O type 13	VCC_FLSH = 1.8 V	3.5			
		I/O type 3	VCC18 = 1.8 V	10.6			
		I/O type 5	VCC_INTF = 2.5 V	5.4			
		I/O type 9, 13	VCC_INTF = 2.5V	10.8			
		I/O type 13	VCC_FLSH = 2.5 V	10.8			
		I/O type 5	VCC_INTF = 3.3 V	7.8			
		I/O type 9	VCC_INTF = 3.3 V	15			
		I/O type 13	VCC_FLSH = 3.3 V	15			
I_{OL}	Low-level output current[6]	I^2C buffer (I/O type 7)		3			mA
		I/O type 2, 4	VCC18 = 1.8 V	2.3			
		I/O type 5	VCC_INTF = 1.8 V	2.3			
		I/O type 1	VCC18 = 1.8 V	4.6			
		I/O type 9	VCC_INTF = 1.8 V	4.6			
		I/O type 13	VCC_FLSH = 1.8 V	4.6			
		I/O type 3	VCC18 = 1.8 V	13.9			
		I/O type 5	VCC_INTF = 2.5 V	5.2			
		I/O type 9	VCC_INTF = 2.5 V	10.4			
		I/O type 13	VCC_FLSH = 2.5 V	10.4			
		I/O type 5	VCC_INTF = 3.3 V	4.4			
		I/O type 9	VCC_INTF = 3.3 V	8.9			
		I/O type 13	VCC_FLSH = 3.3 V	8.9			
I_{OZ}	High-impedance leakage current	I^2C buffer (I/O type 7)	$V_{I2C\ buffer}$ < 0.1 × VCC_INTF or $V_{I2C\ buffer}$ > 0.9 × VCC_INTF	–10		10	µA
		I/O type 1, 2, 3, 6, 8,	VCC18 = 1.8 V	–10		10	
		I/O Type 5, 9, 11	VCC_INTF = 1.8 V	–10		10	
		I/O Type 12, 13	VCC_FLSH = 1.8 V	–10		10	
		I/O type 5, 9, 11	VCC_INTF = 2.5 V	–10		10	
		I/O Type 12, 13	VCC_FLSH = 2.5 V	–10		10	
		I/O Type 5, 9, 11	VCC_INTF = 3.3 V	–10		10	
		I/O type 12, 13	VCC_FLSH = 3.3 V	–10		10	

6.6 Pin Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER(3)			TEST CONDITIONS(4)	MIN	TYP	MAX	UNIT
C_I	Input capacitance (including package)	I^2C buffer (I/O type 7)				5	pF
		I/O type 1, 2, 3, 6, 8	VCC18 = 1.8 V	2.6		3.5	
		I/O Type 5, 9, 11	VCC_INTF = 1.8 V	2.6		3.5	
		I/O Type 12, 13	VCC_FLSH = 1.8 V	2.6		3.5	
		I/O type 5, 9, 11	VCC_INTF = 2.5 V	2.6		3.5	
		I/O type 12, 13	VCC_FLSH = 2.5 V	2.6		3.5	
		I/O type 5, 9, 11	VCC_INTF = 3.3 V	2.6		3.5	
		I/O type 12, 13	VCC_FLSH = 3.3 V	2.6		3.5	
		sub-LVDS – DMD high speed (I/O type 4)	VCC18 = 1.8 V			3	

(1) I/O is high voltage tolerant; that is, if VCC_INTF = 1.8 V, the input is 3.3-V tolerant, and if VCC_INTF = 3.3 V, the input is 5-V tolerant.
(2) Controller pins CMP_OUT, PARKZ, RESETZ, and GPIO_00 through GPIO_19 have slightly varied V_{IH} and V_{IL} range from other 1.8-V I/O.
(3) The I/O type refers to the type defined in Table 5-10.
(4) Test conditions that define a value for VCC18, VCC_INTF, or VCC_FLSH show the nominal voltage that the specified I/O supply reference is set to.
(5) At a high level output signal, the given I/O outputs at least the minimum current specified.
(6) At a low level output signal, the given I/O sinks at least the minimum current specified.

6.7 Internal Pullup and Pulldown Electrical Characteristics

over operating free-air temperature (unless otherwise noted) [2]

INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS	TEST CONDITIONS[1]	MIN	MAX	UNIT
Weak pullup resistance	VCCIO = 3.3 V	29	63	kΩ
	VCCIO = 2.5 V	38	90	kΩ
	VCCIO = 1.8 V	56	148	kΩ
Weak pulldown resistance	VCCIO = 3.3 V	30	72	kΩ
	VCCIO = 2.5 V	36	101	kΩ
	VCCIO = 1.8 V	52	167	kΩ

(1) The resistance is dependent on VCCIO, the supply reference for the pin (see Table 5-10).
(2) An external 8-kΩ pullup or pulldown (if needed) works for any voltage condition to correctly pull enough to override any associated internal pullups or pulldowns.

6.8 DMD Sub-LVDS Interface Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CM}	Common mode voltage		0.8	0.9	1.0	V
V_{CM} (Δpp)[1]	V_{CM} change peak-to-peak (during switching)				75	mV
V_{CM} (Δss)[1]	V_{CM} change steady state		–10		10	mV
$\lvert V_{OD}\rvert$[2]	Differential output voltage magnitude		170	250	350	mV
V_{OD} (Δ)	V_{OD} change (between logic states)		–10		10	mV
V_{OH}	Single-ended output voltage high		0.825	1.025	1.175	V
V_{OL}	Single-ended output voltage low		0.625	0.775	0.975	V
Tx_{term}	Internal differential termination		80	100	120	Ω
Tx_{load}	100-Ω differential PCB trace (50-Ω transmission lines)		0.5		6	inches

(1) See Figure 6-1
(2) V_{OD} is the differential voltage measured across a 100-Ω termination resistance connected directly between the transmitter differential pins. $V_{OD} = V_P - V_N$, where P and N are the differential output pins. $\lvert V_{OD}\rvert$ is the magnitude of the peak-to-peak voltage swing across the P and N output pins (see Figure 6-2). V_{CM} cancels out between signals when measured differentially, thus the reason V_{OD} swings relative to zero.

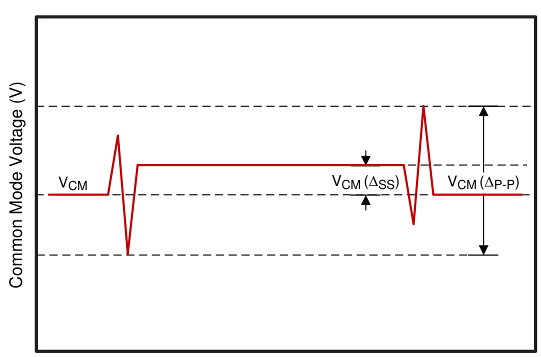
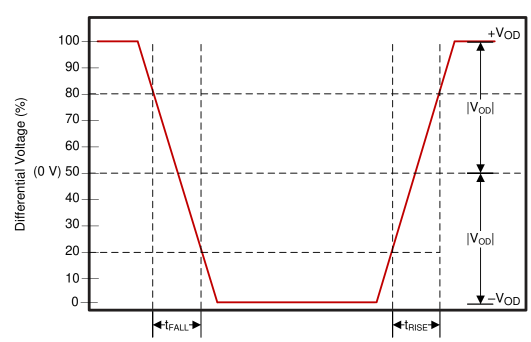


Figure 6-1. Common Mode Voltage



V_{CM} is removed when the signals are viewed differentially

Figure 6-2. Differential Output Signal

6.9 DMD Low-Speed Interface Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER[3]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(DC)}$	DC output high voltage for DMD_LS_WDATA and DMD_LS_CLK		0.7 × VCC18			V
$V_{OL(DC)}$	DC output low voltage for DMD_LS_WDATA and DMD_LS_CLK				0.3 × VCC18	V
$V_{OH(AC)}$ [1]	AC output high voltage for DMD_LS_WDATA and DMD_LS_CLK		0.8 × VCC18		VCC18 + 0.5	V
$V_{OL(AC)}$ [2]	AC output low voltage for DMD_LS_WDATA and DMD_LS_CLK		-0.5		0.2 × VCC18	V
Slew rate	DMD_LS_WDATA and DMD_LS_CLK	$V_{OL(DC)}$ to $V_{OH(AC)}$ for rising edge and $V_{OH(DC)}$ to $V_{OL(AC)}$ for rising edge	1.0		3.0	V/ns
	DMD_DEN_ARSTZ	$V_{OL(AC)}$ to $V_{OH(AC)}$ for rising edge	0.25			
	DMD_LS_RDATA		0.5			

(1) $V_{OH(AC)}$ maximum applies to overshoot. When the DMD_LS_WDATA and DMD_LS_CLK lines include a proper 43-Ω series termination resistor, the DMD operates within the LPSDR input AC specifications.
(2) $V_{OL(AC)}$ minimum applies to undershoot. When the DMD_LS_WDATA and DMD_LS_CLK lines include a proper 43-Ω series termination resistor, the DMD operates within the LPSDR input AC specifications.
(3) See Figure 6-3 for DMD_LS_CLK, and DMD_LS_WDATA rise and fall times. See Figure 6-4 for DMD_DEN_ARSTZ rise and fall times.

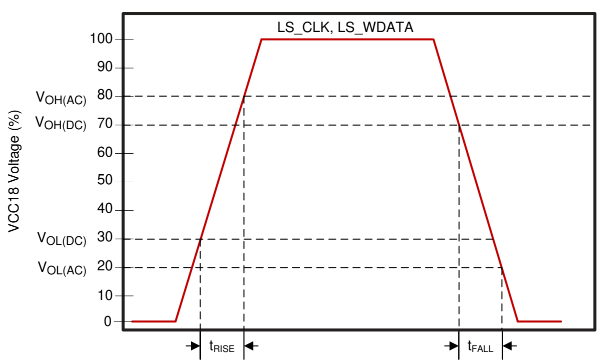


Figure 6-3. LS_CLK and LS_WDATA Slew Rate

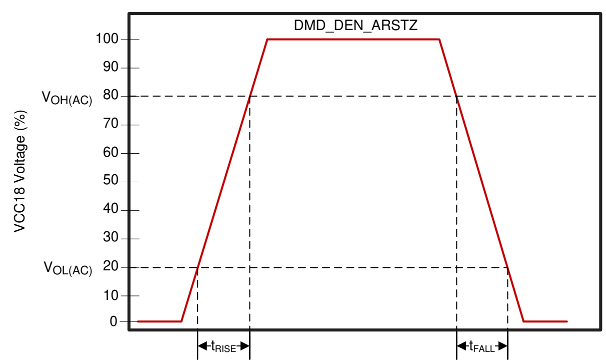


Figure 6-4. DMD_DEN_ARSTZ Slew Rate

6.10 System Oscillators Timing Requirements

			MIN	NOM	MAX	UNIT
f_{clk}	Clock frequency, MOSC (primary oscillator clock)[1]		23.998	24.000	24.002	MHz
t_c	Cycle time, MOSC (clock period)[1]	See Figure 6-5	41.663	41.667	41.670	ns
$t_{w(H)}$	Pulse duration as percent of t_c [2], MOSC, high	50% to 50% reference points (signal)	40%	50%		
$t_{w(L)}$	Pulse duration as percent of t_c [2], MOSC, low	50% to 50% reference points (signal)	40%	50%		
t_t	Transition time[2], MOSC	20% to 80% reference points (rising signal) 80% to 20% reference points (falling signal)			10	ns
t_{jp}	Long-term, peak-to-peak, period jitter[2], MOSC (that is the deviation in period from ideal period due solely to high frequency jitter)				2%	

(1) The frequency accuracy for MOSC is ±200 PPM. This requirement includes any impact to accuracy due to aging, temperature, and trim sensitivity. The MOSC input cannot support spread spectrum clock spreading.
(2) Applies only when driven by an external digital oscillator.

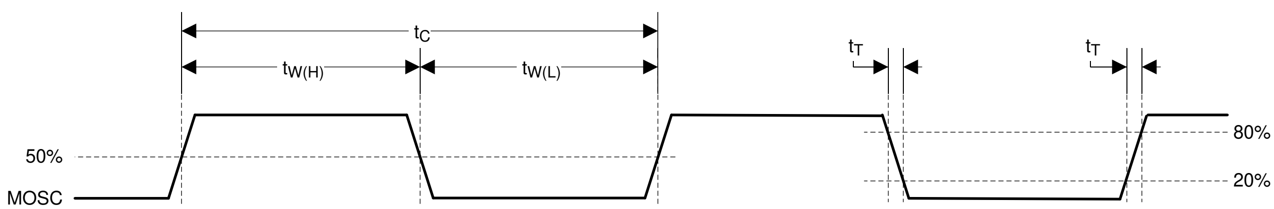


Figure 6-5. System Oscillators

6.11 Power Supply and Reset Timing Requirements

			MIN	MAX	UNIT
$t_{w(L)}$	Pulse duration, inactive low, RESETZ	50% to 50% reference points (signal)	1.25		µs
t_r	Rise time, RESETZ[1]	20% to 80% reference points (signal)		0.5	µs
t_f	Fall time, RESETZ[1]	80% to 20% reference points (signal)		0.5	µs
t_{rise}	Rise time, VDD (during VDD ramp up at turn-on)	0.3 V to 1.045 V (VDD)		1	ms

(1) For more information on RESETZ, see *Section 5*.

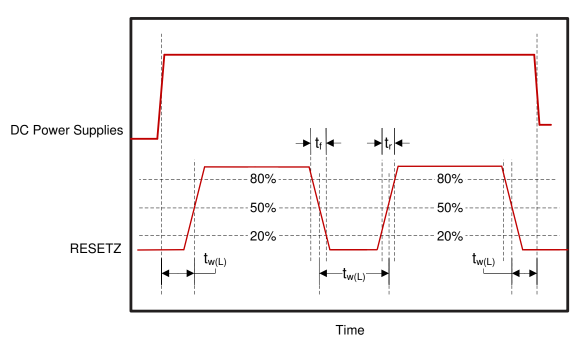


Figure 6-6. Power-Up and Power-Down RESETZ Timing

6.12 Parallel Interface Frame Timing Requirements

			MIN	MAX	UNIT
t_{p_vsw}	Pulse duration – default VSYNC_WE high	50% reference points	1		lines
t_{p_vbp}	Vertical back porch (VBP) – time from the active edge of VSYNC_WE to the active edge of HSYNC_CS for the first active line(1)	50% reference points	2		lines
t_{p_vfp}	Vertical front porch (VFP) – time from the active edge of the HSYNC_CS following the last active line in a frame to the active edge of VSYNC_WE(1)	50% reference points	1		lines
t_{p_tvb}	Total vertical blanking – the sum of VBP and VFP (t_{p_vbp} + t_{p_vfp})	50% reference points	See (1)		lines
t_{p_hsw}	Pulse duration – default HSYNC_CS high	50% reference points	4	128	PCLKs
t_{p_hbp}	Horizontal back porch (HBP) – time from the active edge of HSYNC_CS to the rising edge of DATAEN_CMD	50% reference points	4		PCLKs
t_{p_hfp}	Horizontal front porch (HFP) – time from the falling edge of DATAEN_CMD to the active edge of HSYNC_CS	50% reference points	8		PCLKs

(1) The minimum total vertical blanking is defined by the following equation: t_{p_tvb}(min) = 6 + [8 × Max(1, Source_ALPF/ DMD_ALPF)] lines where:

- SOURCE_ALPF = Input source active lines per frame
- DMD_ALPF = Actual DMD used lines per frame supported

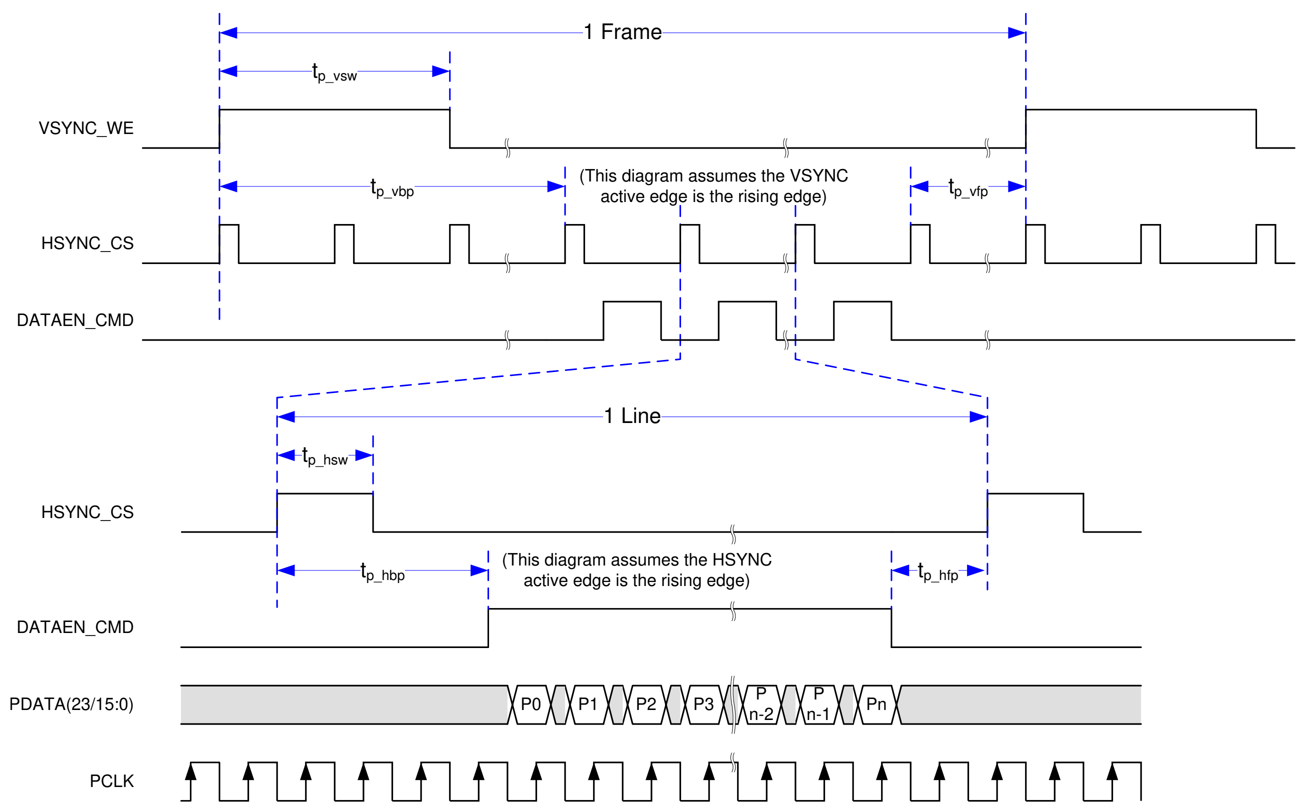


Figure 6-7. Parallel Interface Frame Timing

6.13 Parallel Interface General Timing Requirements

			MIN	MAX	UNIT
f_{clock}	PCLK frequency		1.0	155.0	MHz
t_{p_clkper}	PCLK period	50% reference points	6.45	1000	ns
t_{p_clkjit}	PCLK jitter	Max f_{clock}		see (1)	
t_{p_wh}	PCLK pulse duration high	50% reference points	2.43		ns
t_{p_wl}	PCLK pulse duration low	50% reference points	2.43		ns
t_{p_su}	Setup time – HSYNC_CS, DATAEN_CMD, PDATA(23:0) valid before the active edge of PCLK	50% reference points	0.9		ns
t_{p_h}	Hold time – HSYNC_CS, DATAEN_CMD, PDATA(23:0) valid after the active edge of PCLK	50% reference points	0.9		ns
t_t	Transition time – all signals	20% to 80% reference points (rising signal) 80% to 20% reference points (falling signal)	0.2	2.0	ns
t_{setup}, 3DR	Setup time with respect to VSYNC(2)	50% reference points	1.0		ms
t_{hold}, 3DR	Hold time with respect VSYNC(3)	50% reference points	1.0		ms

(1) Calculate clock jitter (in ns) using this formula: Jitter = [1 / f_{clock} – 5.76 ns]. Setup and hold times must be met even with clock jitter.
(2) In other words, the 3DR signal must change at least 1.0 ms before VSYNC changes
(3) In other words, the 3DR signal must not change for at least 1.0 ms after VSYNC changes

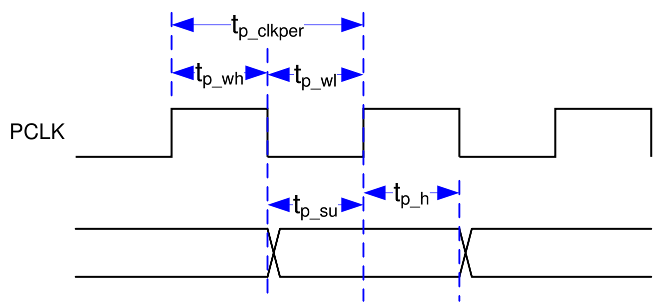


Figure 6-8. Parallel Interface General Timing

6.14 Flash Interface Timing Requirements

The DLPC3437 controller flash memory interface consists of a SPI flash serial interface with a programmable clock rate. The DLPC3437 can support 1- to 128-Mb flash memories.(1) (2) (4)

			MIN	MAX	UNIT
f_{clock}	SPI_CLK frequency	See (3)	1.4	36.0	MHz
t_{p_clkper}	SPI_CLK period	50% reference points	27.8	704	ns
t_{p_wh}	SPI_CLK pulse duration high	50% reference points	352		ns
t_{p_wl}	SPI_CLK pulse duration low	50% reference points	352		ns
t_t	Transition time – all signals	20% to 80% reference points (rising signal) 80% to 20% reference points (falling signal)	0.2	3.0	ns
t_{p_su}	Setup time – SPI_DIN valid before SPI_CLK falling edge	50% reference points	10.0		ns
t_{p_h}	Hold time – SPI_DIN valid after SPI_CLK falling edge	50% reference points	0.0		ns
t_{p_clqv}	SPI_CLK clock falling edge to output valid time – SPI_DOUT and SPI_CSZ	50% reference points		1.0	ns
t_{p_clqx}	SPI_CLK clock falling edge output hold time – SPI_DOUT and SPI_CSZ	50% reference points	–3.0	3.0	ns

(1) Standard SPI protocol is to transmit data on the falling edge of SPI_CLK and capture data on the rising edge. The DLPC3437 does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This feature provides support for SPI devices with long clock-to-Q timing. DLPC3437 hold capture timing has been set to facilitate reliable operation with standard external SPI protocol devices.
(2) With the above output timing, DLPC3437 provides the external SPI device 8.2-ns input set-up and 8.2-ns input hold, relative to the rising edge of SPI_CLK.
(3) This range includes the 200 ppm of the external oscillator (but no jitter).
(4) For additional requirements of the external flash device view Section 7.3.3.1.

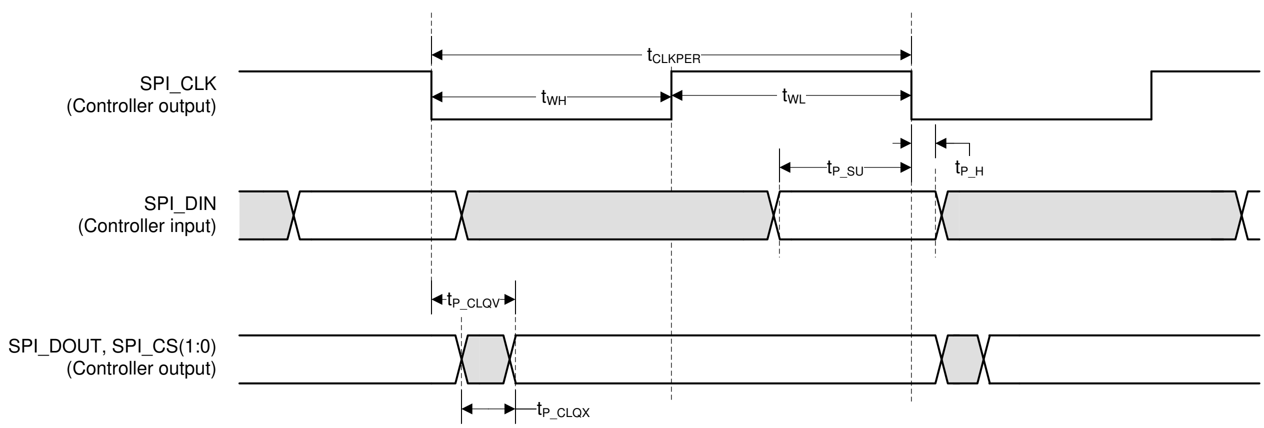


Figure 6-9. Flash Interface Timing

6.15 Other Timing Requirements

		MIN	MAX	UNIT
t_{rise}, all[(1) (2)]	20% to 80% reference points		10	ns
t_{fall}, all[(1) (2)]	80% to 20% reference points		10	ns
t_{rise}, PARKZ[(2)]	20% to 80% reference points		150	ns
t_{fall}, PARKZ[(2)]	80% to 20% reference points		150	ns
t_w, GPIO_08 (normal park) pulse width[(3)]		200		ms
I^2C baud rate			100	kHz

(1) Unless noted elsewhere, the following signal transition times are for all DLPC34xx signals.
(2) This is the recommended signal transition time to avoid input buffer oscillations.
(3) When the controller is turned off by setting PROJ_ON low, PROJ_ON must not be brought high again for at least 200 ms. See Section 9.3 for additional requirements.

6.16 DMD Sub-LVDS Interface Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R [(1)]	Differential output rise time				250	ps
t_F [(1)]	Differential output fall time				250	
t_{switch}	DMD HS Clock switching rate			1200		Mbps
f_{clock}	DMD HS Clock frequency			600		MHz
DCout	DMD HS Clock output duty cycle		45%	50%	55%	

(1) Rise and fall times are defined for the differential V_{OD} signal as shown in Figure 6-2.

6.17 DMD Parking Switching Characteristics

See [(2)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{park}	Normal park time[(1)]				20	ms
$t_{fast\ park}$	Fast park time[(3)]				40	µs

(1) Normal park time is defined as how long it takes the DLPC34xx controller to complete the parking of the DMD after it receives the normal park request (GPIO_08 goes low).
(2) The oscillator and power supplies must remain active for at least the duration of the park time. The power supplies must additionally be held on for a time after parking is completed to satisfy DMD requirements. See Section 9.2 and the appropriate DMD or PMIC datasheet for more information.
(3) Fast park time is defined as how long it takes the DLPC34xx controller to complete the parking of the DMD after it receives the fast park request (PARKZ goes low).

6.18 Chipset Component Usage Specification

Reliable function and operation of the DLP chipset requires that it be used with all components (DMD, PMIC, and controller) of the applicable DLP chipset.

Table 6-1. DLPC3437 Supported DMDs and PMICs

DLPC3437 DLP CHIPSET	
DMD	DLP3310
PMIC	DLPA3000
	DLPA3005

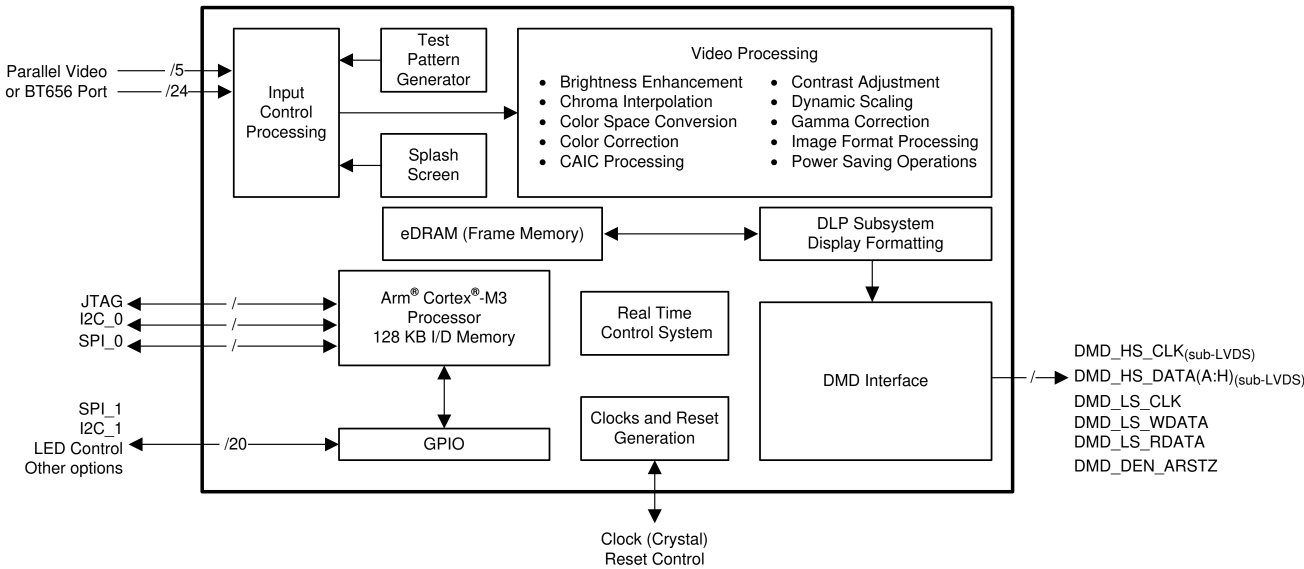
In addition to the required DLP chipset, the XC7Z020-1CLG484I4493 FPGA is required to be used in conjunction with this particular DLP chipset.

7 Detailed Description

7.1 Overview

The DLPC3437 is the display controller for the DLP3310 (0.33 1080p) DMD. The DLPC3437 is part of the chipset comprising the DLPC3437 controller, the DLP3310 (0.33 1080p) DMD, and the DLPA300X PMIC (which includes an LED driver). All three components of the chipset must be used in conjunction with each other, along with the XC7Z020-1CLG484I4493 FPGA for reliable operation of the DLP3310 (0.33 1080p) DMD. See Table 6-1. The DLPC3437 display controller provides data and image processing functions that are optimized for small form factor and power-constrained full HD display applications. Applications include pico projectors, wearable displays, and digital signage. Standalone projectors must include a separate front-end chip to interface to the outside world (for example, video decoder, HDMI receiver, triple ADC, or USB I/F chip).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Source Requirements

7.3.1.1 Supported Resolution and Frame Rates

This section defines the timing requirements for the external interfaces for the DLPC3437 controller.

Table 7-1. Supported Input Source Ranges

INTERFACE(1)	BITS / PIXEL (4)	IMAGE TYPE(2)	SOURCE RESOLUTION RANGE(3) (5)				FRAME RATE RANGE
			HORIZONTAL		VERTICAL		
			LANDSCAPE	PORTRAIT	LANDSCAPE	PORTRAIT	
Parallel	24	2D - 1080p	1920	N/A	1080	N/A	50 ± 2 Hz, 60 ± 2 Hz
Parallel	24	2D - WXGA	1366	N/A	768	N/A	50 ± 2 Hz, 60 ± 2 Hz
Parallel	24	2D - 720p	1280	N/A	720	N/A	50 ± 2 Hz, 60 ± 2 Hz
Parallel	24	3D - 720p	1280	N/A	720	N/A	100 ± 2 Hz, 120 ± 2 Hz

(1) The application must remain within specifications for all source interface parameters such as maximum clock rate and maximum line rate.
(2) The maximum DMD pixel display resolution is 1920x1080 while system actuator is enabled.
(3) To achieve the ranges stated, the firmware must support the source parameters. Review the firmware release notes or contact TI to determine the latest available frame rate and input resolution support for a given firmware image.
(4) Bits per pixel does not necessarily equal the number of data pins used on the DLPC34xx controller. Fewer pins are used if multiple clocks are used per pixel transfer.
(5) The DLPC3437 only supports Landscape orientation.

7.3.1.2 3D Display

For 3D sources on the video input interface, images must be frame sequential (L, R, L, ...) when input to the DLPC34xx controller. Any processing required to unpack 3D images and to convert them to frame sequential input must be done by external electronics prior to inputting the images to the controller. Each 3D source frame input must contain a single eye frame of data, separated by a VSYNC, where an eye frame contains image data for a single left or right eye. The signal 3DR input to the controller indicates whether the input frame is for the left eye or right eye.

Each DMD frame is displayed at the same rate as the input interface frame rate. Figure 7-1 below shows the typical timing for a 50-Hz or 60-Hz 3D HDMI source frame, the input interface of the DLPC34xx controller, and the DMD. In general, video frames sent over the HDMI interface pack both the left and right content into the same video frame. GPIO_04 is optionally sent to a transmitter on the system PCB for wirelessly transmitting a synchronization signal to 3D glasses (usually an IR sync signal). The glasses are then in phase with the DMD images displayed. Alternately, the *3D Glasses Operation* section shows how DLP link pulses can be used instead.

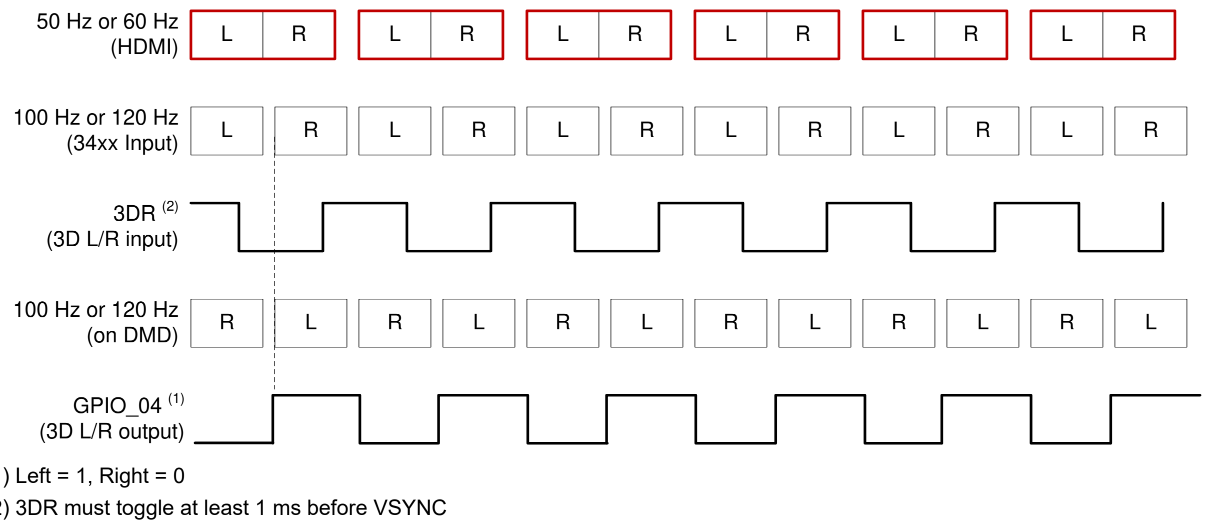


Figure 7-1. 3D Display Left and Right Frame Timing

The frame and sub-frame timing for 2D sources is shown in Figure 7-2 while the frame and sub-frame timing for 3D sources is shown in Figure 7-3.

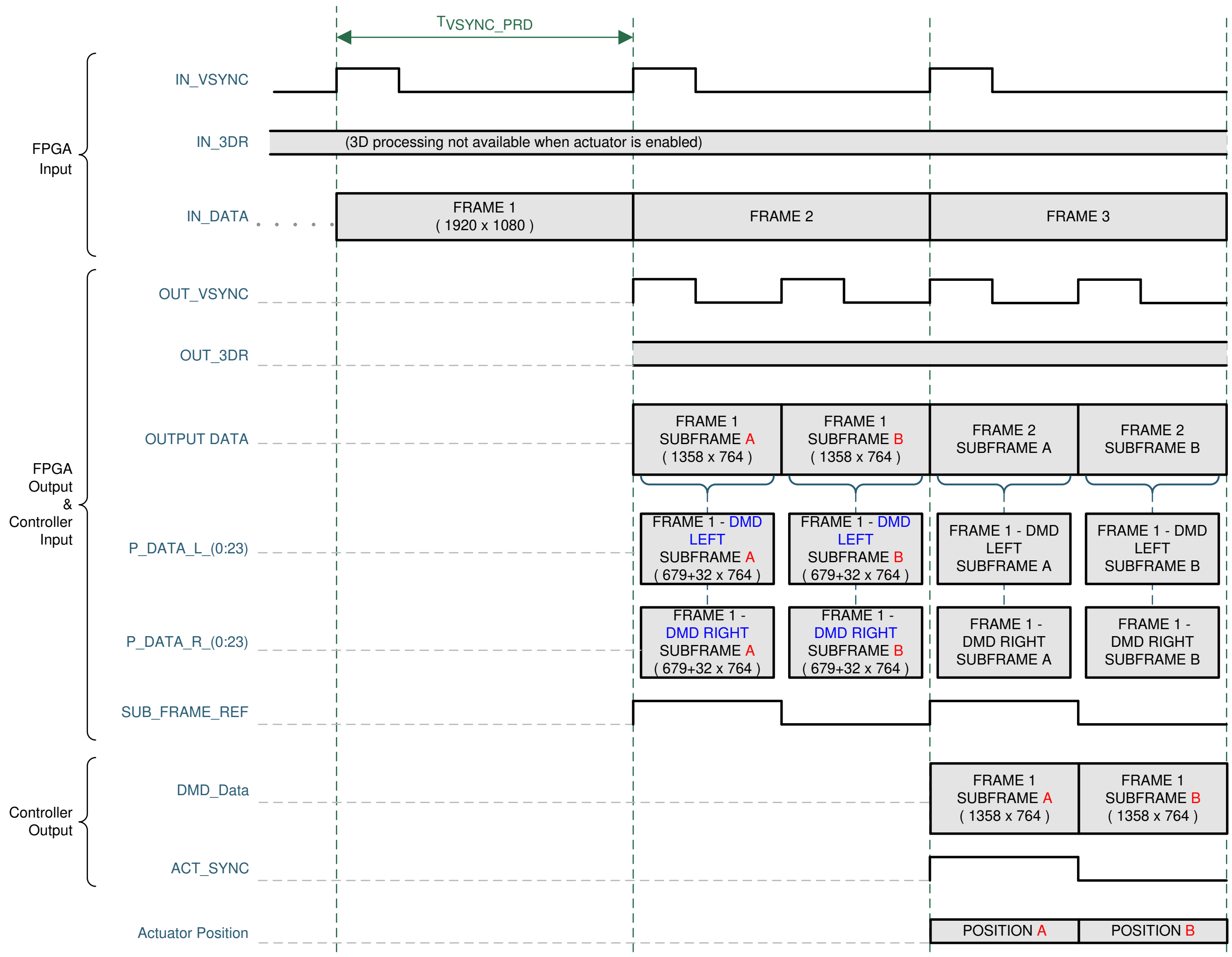


Figure 7-2. DLPC3437 2D Actuator Frame and Signal Timing

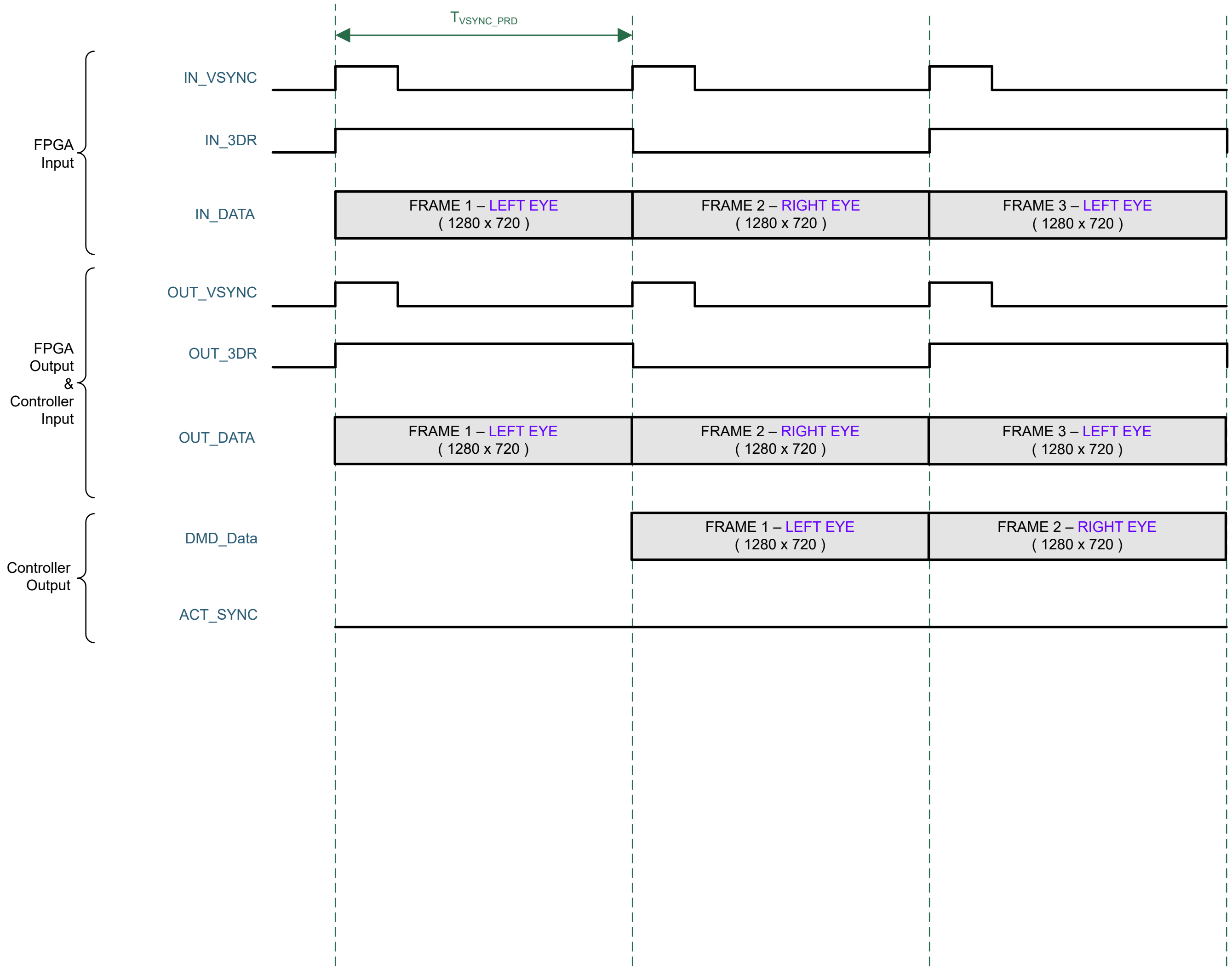


Figure 7-3. DLPC3437 3D Frame and Signal Timing

7.3.1.3 Parallel Interface

The parallel interface complies with standard graphics interface protocol, with the addition of the SUB_FRAME signal (which is a necessary output from the XC7Z020-1CLG484I4493 FPGA). The standard graphics interface protocol includes a vertical sync signal (VSYNC_WE), horizontal sync signal (HSYNC_CS), optional data valid signal (DATAEN_CMD), a 24-bit data bus (PDATA), and a pixel clock (PCLK). The polarity of both syncs and the active edge of the clock are programmable. Figure 6-7 shows the relationship of these signals.

Note

VSYNC_WE must remain active at all times (in lock-to-VSYNC mode) or the display sequencer stops and turns off the LEDs.

7.3.1.3.1 Parallel Interface Data Transfer Format

The data format on the PDATA(23:0) bus between the 0.33 1080p FPGA and the DLPC3437 is always RGB888, as shown in Figure 7-4.

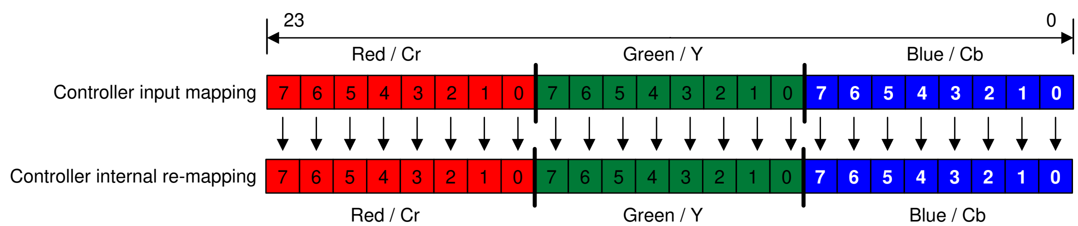
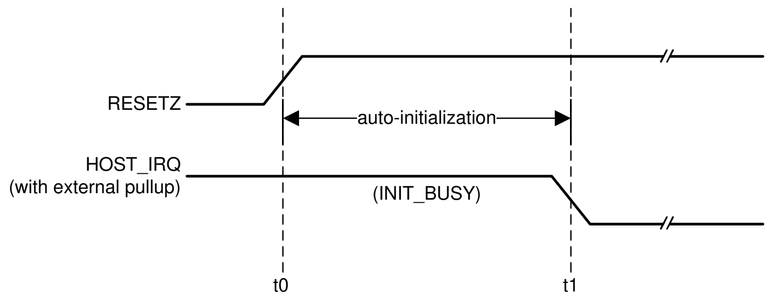


Figure 7-4. RGB-888 I/O Mapping

7.3.2 Device Start-Up

- The HOST_IRQ signal is provided to indicated when the system has completed auto-initialization.
- While reset is applied, HOST_IRQ is tri-stated (an external pullup resistor pulls the line high).
- HOST_IRQ remains tri-stated (pulled high externally) until the boot process completes. While the signal is pulled high, this indicates that the controller is performing boot-up and auto-initialization.
- As soon as possible after the controller boots-up, the controller drives HOST_IRQ to a logic high state to indicate that the controller is continuing to perform auto-initialization (no real state changes occur on the external signal).
- The software sets HOST_IRQ to a logic low state at the completion of the auto-initialization process. At the falling edge of the signal, the initialization is complete.
- The DLPC34xx controller is ready to receive commands through I^{2}C or accept video over the parallel interface only after auto-initialization is complete.
- The controller initialization typically completes (HOST_IRQ goes low) within 3.29 s of RESETZ being asserted. However, this time can vary depending on the software version and the contents of the user configurable auto initialization file.



t0: rising edge of RESETZ; auto-initialization begins
t1: falling edge of HOST_IRQ; auto-initialization is complete

Figure 7-5. HOST_IRQ Timing

7.3.3 SPI Flash

7.3.3.1 SPI Flash Interface

The DLPC34xx controller requires an external SPI serial flash memory device to store the firmware. Follow the below guidelines and requirements in addition to the requirements listed in the *Flash Interface Timing Requirements* section.

The controller supports a maximum flash size of 128 Mb (16 MB). See the DLPC34xx Validated SPI Flash Device Options table for example compatible flash options. The minimum required flash size depends on the size of the utilized firmware. The firmware size depends upon a variety of factors including the number of sequences, lookup tables, and splash images.

The DLPC34xx controller uses a single SPI interface that complies to industry standard SPI flash protocol. The device will begin accessing the flash at a nominal 1.42-MHz frequency before running at a nominal 30-MHz rate. The flash device must support these rates.

The controller has two independent SPI chip select (CS) control lines. Ensure that the chip select pin of the flash device is connects to SPI0_CSZ0 as the controller boot routine is executes from the device connected to chip select zero. The boot routine uploads program code from flash memory to program memory then transfers control to an auto-initialization routine within program memory.

The DLPC34xx is designed to support any flash device that is compatible with the modes of operation, features, and performance as defined in the Additional DLPC34xx SPI Flash Requirements table below Table 7-2, Table 7-3, and Table 7-4.

Table 7-2. Additional DLPC34xx SPI Flash Requirements

FEATURE	DLPC34xx REQUIREMENT
SPI interface width	Single
SPI polarity and phase settings	SPI mode 0
Fast READ addressing	Auto-incrementing
Programming mode	Page mode
Page size	256 B
Sector size	4-KB sector
Block size	Any
Block protection bits	0 = Disabled
Status register bit(0)	Write in progress (WIP), also called flash busy
Status register bit(1)	Write enable latch (WEN)
Status register bits(6:2)	A value of 0 disables programming protection
Status register bit(7)	Status register write protect (SRWP)
Status register bits(15:8) (that is expansion status byte)	Because the DLPC34xx controller supports only single-byte status register R/W command execution, it may not be compatible with flash devices that contain an expansion status byte. However, as long as the expansion status byte is considered optional in the byte 3 position and any write protection control in this expansion status byte defaults to unprotected, then the flash device is likely compatible with the DLPC34xx.

The DLPC34xx controller is intended to support flash devices with program protection defaults of either enabled or disabled. The controller assumes the default is enabled and proceeds to disable any program protection as part of the boot process.

The DLPC34xx issues these commands during the boot process:

- A write enable (WREN) instruction to request write enable, followed by
- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, a write status register (WRSR) instruction that writes 0 to all 8 bits (this disables all programming protection)

Prior to each program or erase instruction, the DLPC34xx controller issues similar commands:

- A write enable (WREN) instruction to request write enable, followed by
- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, the program or erase instruction

Note that the flash device automatically clears the write enable status after each program and erase instruction.

Table 7-3 and Table 7-4 below list the specific instruction OpCode and timing compatibility requirements. The DLPC34xx controller does not adapt protocol or clock rate based on the flash type connected.

Table 7-3. SPI Flash Instruction OpCode and Access Profile Compatibility Requirements

SPI FLASH COMMAND	BYTE 1 (OPCODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Fast READ (1 output)	0x0B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0)[(1)]
Read status	0x05	N/A	N/A	STATUS(0)		
Write status	0x01	STATUS(0)	See [(2)]			
Write enable	0x06					
Page program	0x02	ADDRS(0)	ADDRS(1)	ADDRS(2)	DATA(0)[(1)]	
Sector erase (4 KB)	0x20	ADDRS(0)	ADDRS(1)	ADDRS(2)		
Chip erase	0xC7					

(1) Shows the first data byte only. Data continues.
(2) Access to a second (expansion) write status byte not supported by the DLPC34xx controller.

Table 7-4 below and the *Flash Interface Timing Requirements* section list the specific timing compatibility requirements for a DLPC34xx compatible flash device.

Table 7-4. SPI Flash Key Timing Parameter Compatibility Requirements

SPI FLASH TIMING PARAMETER[(1) (2)]	SYMBOL	ALTERNATE SYMBOL	MIN	MAX	UNIT
Access frequency (all commands)	FR	f_C	≤ 1.4	≥ 30.1	MHz
Chip select high time (also called chip select deselect time)	t_{SHSL}	t_{CSH}	≤ 200		ns
Output hold time	t_{CLQX}	t_{HO}	≥ 0		ns
Clock low to output valid time	t_{CLQV}	t_V		≤ 11	ns
Data in set-up time	t_{DVCH}	t_{DSU}	≤ 5		ns
Data in hold time	t_{CHDX}	t_{DH}	≤ 5		ns

(1) The timing values apply to the specification of the peripheral flash device, not the DLPC34xx controller. For example, the flash device minimum access frequency (FR) must be 1.4 MHz or less and the maximum access frequency must be 30.1 MHz or greater.
(2) The DLPC34xx does not drive the $\overline{\text{HOLD}}$ or $\overline{\text{WP}}$ (active low write protect) pins on the flash device, and thus these pins must be tied to a logic high on the PCB through an external pullup.

In order for the DLPC34xx controller to support 1.8-V, 2.5-V, or 3.3-V serial flash devices, the VCC_FLSH pin must be supplied with the corresponding voltage. The DLPC34xx Validated SPI Flash Device Options table contains a list of validated 1.8-V, 2.5-V, or 3.3-V compatible SPI serial flash devices supported by the DLPC34xx controller.

Table 7-5. DLPC34xx Validated SPI Flash Device Options[(1) (2) (3)]

DENSITY (Mb)	VENDOR	PART NUMBER	PACKAGE SIZE
1.8-V COMPATIBLE DEVICES			
4 Mb	Winbond	W25Q40BWUXIG	2 × 3 mm USON
4 Mb	Macronix	MX25U4033EBAI-12G	1.43 × 1.94 mm WLCSP
8 Mb	Macronix	MX25U8033EBAI-12G	1.68 × 1.99 mm WLCSP
2.5- OR 3.3-V COMPATIBLE DEVICES			
16 Mb	Winbond	W25Q16CLZPIG	5 × 6 mm WSON

(1) The flash supply voltage must equal VCC_FLSH supply voltage on the DLPC34xx controller. Make sure to order the device that supports the correct supply voltage as multiple voltage options are often available.
(2) Numonyx (Micron) serial flash devices typically do not support the 4 KB sector size compatibility requirement for the DLPC34xx controller.
(3) The flash devices in this table have been formally validated by TI. Other flash options may be compatible with the DLPC34xx controller, but they have not been formally validated by TI.

7.3.3.2 SPI Flash Programming

The SPI pins of the flash can directly be driven for flash programming while the DLPC34xx controller I/Os are tri-stated. SPI0_CLK, SPI0_DOUT, and SPI0_CSZ0 I/O can be tri-stated by holding RESETZ in a logic low state while power is applied to the controller. The logic state of the SPI0_CSZ1 pin is not affected by this action. Alternatively, the DLPC34xx controller can program the SPI flash itself when commanded via I^2C if a valid firmware image has already been loaded and the controller is operational.

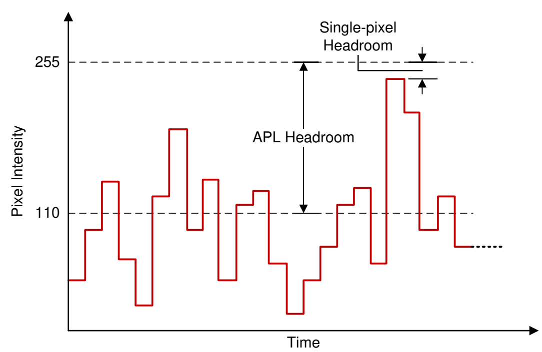
7.3.4 I^2C Interface

Both of the DLPC34xx I^2C interface ports support a 100-kHz baud rate. Because I^2C interface transactions operate at the speed of the slowest device on the bus, there is no requirement to match the speed of all devices in the system.

7.3.5 Content Adaptive Illumination Control (CAIC)

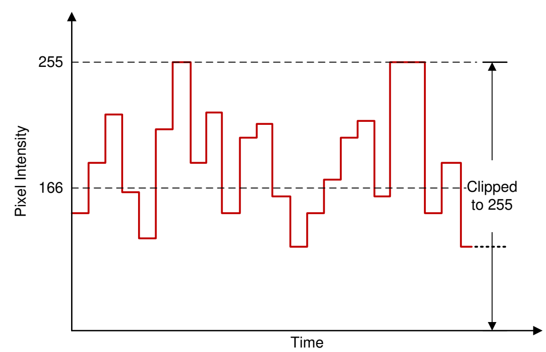
Content Adaptive Illumination control (CAIC) is part of the IntelliBright® suite of advanced image processing algorithms that adaptively enhances brightness and reduces power. In common real-world image content most pixels in the images are well below full scale for the for the R (red), G (green), and B (blue) digital channels input to the DLPC34xx. As a result of this, the average picture level (APL) for the overall image is also well below full scale, and the dynamic range for the collective set of pixel values is not fully used. CAIC takes advantage of the headroom between the source image APL and the top of the available dynamic range of the display system.

CAIC evaluates images on a frame-by-frame basis and derives three unique digital gains, one for each of the R, G, and B color channel. During image processing, CAIC applies each gain to all pixels in the associated color channel. The calculated gain is applied to all pixels in that channel so that the pixels as a group collectively shift upward and as close to full scale as possible. To prevent any image quality degradation, the gains are set at the point where just a few pixels in each color channel are clipped. The Source Pixels for a Color Channel and Pixels for a Color Channel After CAIC Processing figures below show an example of the application of CAIC for one color channel.



(1) APL = 110

Figure 7-6. Source Pixels for a Color Channel

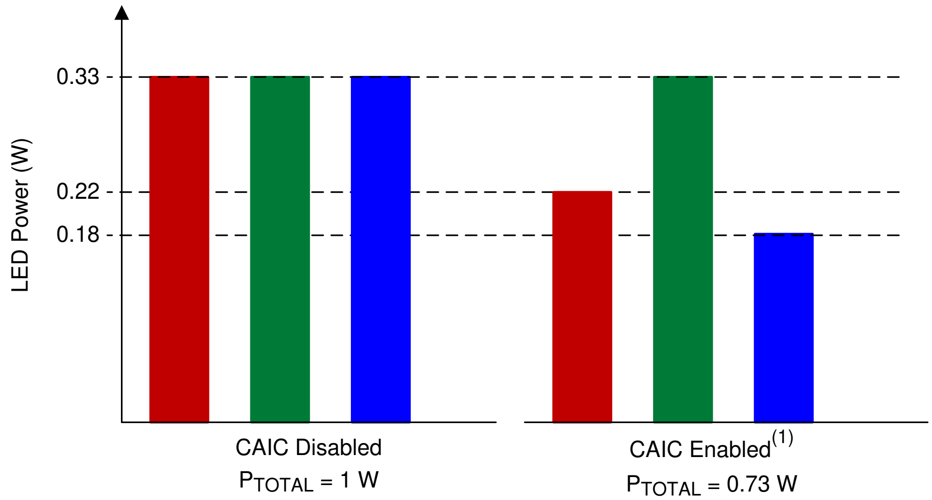


(1) APL = 166

(2) Channel gain = 166/110 = 1.51

Figure 7-7. Pixels for a Color Channel After CAIC Processing

Above, Figure 7-7 shows the gain that is applied to a color processing channel inside the DLPC34xx. Additionally, CAIC adjusts the power for the R, G, and B LED by commanding different LED currents. For each color channel of an individual frame, CAIC intelligently determines the optimal combination of digital gain and LED power. The user configurable CAIC settings heavily influence the amount of digital gain that is applied to a color channel and the LED power for that color.



(1) With CAIC enabled, if red and blue LEDs require less than nominal power for a given input image, the red and blue LED power will reduce.

Figure 7-8. CAIC Power Reduction Mode (for Constant Brightness)

As CAIC applies a digital gain to each color channel and adjusts the power to each LED, CAIC ensures the resulting color balance in the final image matches the target color balance for the projector system. Thus, the effective displayed white point of images is held constant by CAIC from frame to frame.

CAIC can be used to increase the overall image brightness while holding the total power for all LEDs constant, or CAIC can be used to hold the overall image brightness constant while decreasing LED power. In summary, CAIC has two primary modes of operation:

- Power reduction mode holds overall image brightness constant while reducing LED power
- Enhanced brightness mode holds overall LED power constant while enhancing image brightness

In power reduction mode, since the R, G, and B channels can be gained up by CAIC inside the DLPC34xx, the LED power can be reduced for any color channel until the brightness of the color on the screen is unchanged. Thus, CAIC can achieve an overall LED power reduction while maintaining the same overall image brightness as if CAIC was not used. Figure 7-8 shows an example of LED power reduction by CAIC for an image where the red and blue LEDs can consume less power.

In enhanced brightness mode the R, G, and B channels can be gained up by CAIC with LED power generally being held constant. This results in an enhanced brightness with no power savings.

While there are two primary modes of operation described, the DLPC34xx actually operates within the extremes of pure power reduction mode and enhanced brightness mode. The user can configure which operating mode the DLPC34xx will more closely follow by adjusting the CAIC gain setting as described in the software programmer's guide.

In addition to the above functionality, CAIC also can be used as a tool with which FOFO (full-on full-off) contrast on a projection system can be improved. While operating in power reduction mode, the DLPC34xx reduces LED power as the intensity of the image content for each color channel decreases. This will result in the LEDs operating at nominal settings with full-on content (a white screen) and reducing power output until the dimmest possible content (a black screen) is reached. In this latter case, the LEDs will be operating at minimum power output capacity and thus producing the minimum possible amount of off-state light. This optimization provided by CAIC will thereby improve FOFO contrast ratio. The given contrast ratio will further increase as nominal LED current (full-on state) is increased.

7.3.6 Local Area Brightness Boost (LABB)

Local area brightness boost (LABB), part of the IntelliBright™ suite of advanced image processing algorithms, adaptively gains up regions of an image that are dim relative to the average picture level. The controller applies significant gain to some regions of the image, and applies little or no gain to other regions. The LABB algorithm evaluates images frame-by-frame and calculates the local area gains to be used for each image. Since many images have a net overall boost in gain, even if the controller applies no gain to some parts of the image, the controller boosts the overall perceived brightness of the image.

Figure 7-9 shows a split screen example of the impact of the LABB algorithm for an image that includes dark areas.

Figure 7-9. LABB Enabled (Left Side) and LABB Disabled (Right Side)

The LABB algorithm operates most effectively when ambient light conditions are used to help determine the decision about the strength of gains utilized. For this reason, it may be useful to include an ambient light sensor in the system design that is used to measure the display screen's reflected ambient light. This sensor can assist in dynamically controlling the LABB strength. Set the LABB gain higher for bright rooms to help overcome washed out images. Set the LABB gain lower in dark rooms to prevent overdriven pixel intensities in images.

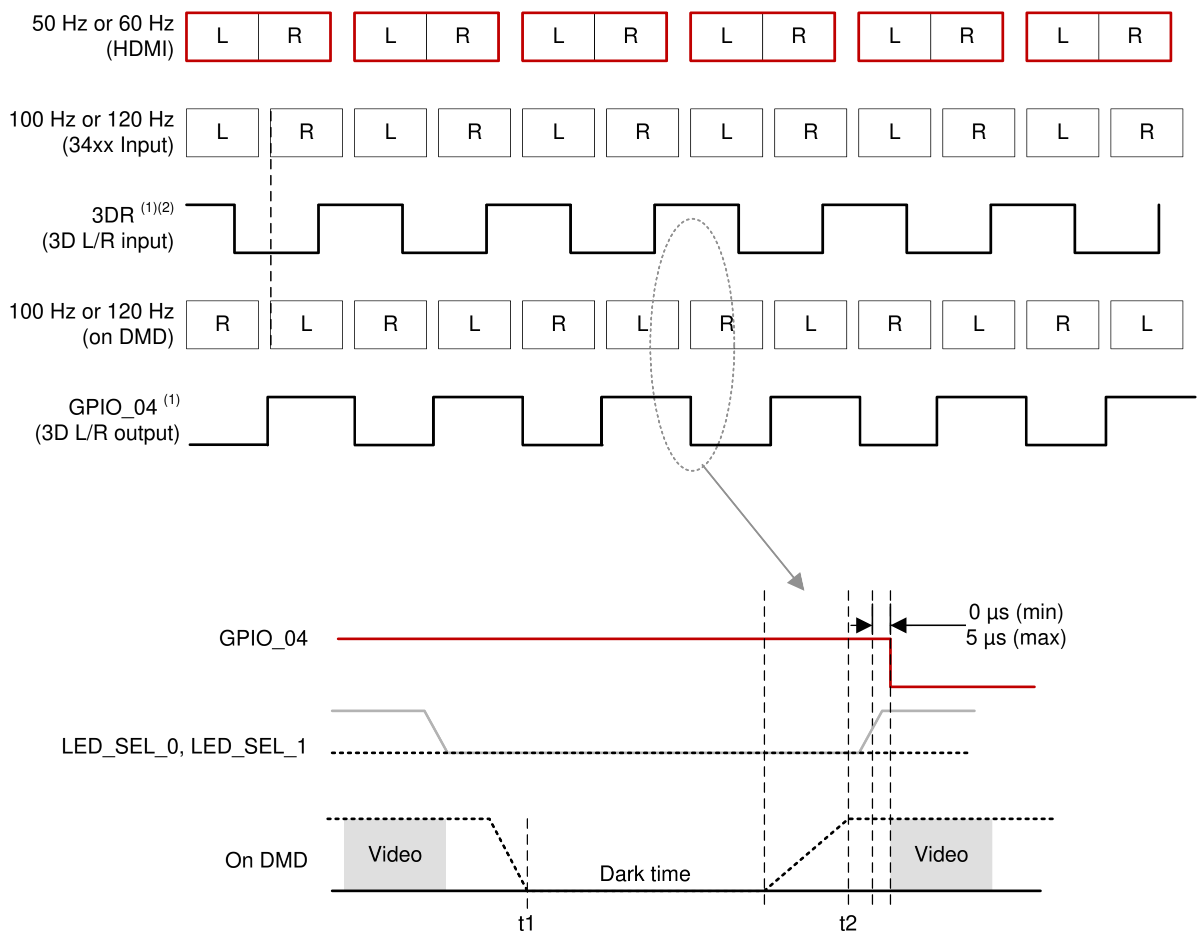
7.3.7 3D Glasses Operation

When using 3D glasses (with 3D video input and appropriate software support), the controller outputs sync information to align the left eye and right eye shuttering in the glasses with the displayed DMD image frames. 3D glasses typically use either Infrared (IR) transmission or DLP Link™ technology to achieve this synchronization.

One glasses type uses an IR transmitter on the system PCB to send an IR sync signal to an IR receiver in the glasses. In this case DLPC34xx controller output signal GPIO_04 can be used to cause the IR transmitter to send an IR sync signal to the glasses. Figure 7-10 shows the timing sequence for the GPIO_04 signal.

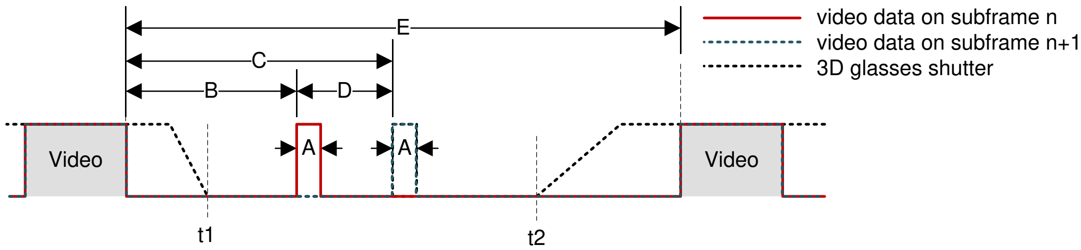
The second type of glasses relies on sync information that is encoded into the light being output from the projection lens. This approach uses the DLP Link feature for 3D video. Many 3D glasses from different suppliers have been built using this method. The advantage of using the DLP Link feature is that it takes advantage of existing projector hardware to transmit the sync information to the glasses. This method may give an advantage in cost, size and power savings in the projector.

When using DLP Link technology, one light pulse per DMD frame is output from the projection lens while the glasses have both shutters closed. To achieve this, the DLPC34xx tells the DLPAxxxx when to turn on the illumination source (typically LEDs or lasers) so that an encoded light pulse is output once per DMD frame. Because the shutters in the glasses are both off when the pulse is sent, the projector illumination source is also off except when the light is sent to create the pulse. The pulses may use any color; however, due to the transmission property of the eye-glass LCD shutter lenses and the sensitivity of the white-light sensor used on the eye-glasses, it is highly recommended that blue is not used for pulses. Red pulses are the recommended color to use. Figure 7-10 shows 3D timing information. Figure 7-11 and Table 7-6 show the timing for the light pulses when using the DLP Link feature.



(1) Left = 1, Right = 0
(2) 3DR must toggle 1 ms before VSYNC
t1: both shutters turned off
t2: next shutter turned on

Figure 7-10. 3D Display Left and Right Frame and Signal Timing



The time offset of DLP Link pulses at the end of a subframe alternates between B and B+D where D is the delta offset.

Figure 7-11. 3D DLP Link Pulse Timing

Table 7-6. 3D DLP Link Timing

HDMI SOURCE FRAME RATE (Hz)(1)	DLPC34xx INPUT FRAME RATE (Hz)	A (µs)	B (µs)	C (µs)	D (µs)	E (µs)
49.0	98	20 - 32 (31.8 nominal)	> 500	> 622	128 - 163 (161.6 nominal)	> 2000
50.0	100	20 - 32 (31.2 nominal)	> 500	> 658	128 - 163 (158.4 nominal)	> 2000
51.0	102	20 - 32 (30.6 nominal)	> 500	> 655	128 - 163 (155.3 nominal)	> 2000
59.0	118	20 - 32 (26.4 nominal)	> 500	> 634	128 - 163 (134.2 nominal)	> 2000
60.0	120	20 - 32 (26.0 nominal)	> 500	> 632	128 - 163 (132.0 nominal)	> 2000
61.0	122	20 - 32 (25.6 nominal)	> 500	> 630	128 - 163 (129.8 nominal)	> 2000

(1) Timing parameter C is always the sum of B+D.

7.3.8 Test Point Support

The DLPC34xx test point output port, TSTPT_(7:0), provides selected system calibration and controller debug support. These test points are inputs when reset is applied. These test points are outputs when reset is released. The controller samples the signal state upon the release of system reset and then uses the captured value to configure the test mode until the next time reset is applied. Because each test point includes an internal pulldown resistor, external pullups must be used to modify the default test configuration.

The default configuration (b000) corresponds to the TSTPT_(2:0) outputs remaining tri-stated to reduce switching activity during normal operation. For maximum flexibility, a jumper to external pullup resistors is recommended for TSTPT_(2:0). The pullup resistors on TSTPT_(2:0) can be used to configure the controller for a specific mode or option. TI does not recommend adding pullup resistors to TSTPT_(7:3) due to potentially adverse effects on normal operation. For normal use TSTPT_(7:3) should be left unconnected. The test points are sampled only during a 0-to-1 transition on the RESETZ input, so changing the configuration after reset is released does not have any effect until the next time reset asserts and releases. Table 7-7 describes the test mode selections for one programmable scenario defined by TSTPT_(2:0).

Table 7-7. Test Mode Selection Scenario Defined by TSTPT_(2:0)

TSTPT OUTPUT VALUE(1)	NO SWITCHING ACTIVITY	CLOCK DEBUG OUTPUT
	TSTPT_(2:0) = 0b000	TSTPT_(2:0) = 0b010
TSTPT_0	HI-Z	60 MHz
TSTPT_1	HI-Z	30 MHz
TSTPT_2	HI-Z	0.7 to 22.5 MHz

Table 7-7. Test Mode Selection Scenario Defined by TSTPT_(2:0) (continued)

TSTPT OUTPUT VALUE(1)	NO SWITCHING ACTIVITY	CLOCK DEBUG OUTPUT
	TSTPT_(2:0) = 0b000	TSTPT_(2:0) = 0b010
TSTPT_3	HI-Z	HIGH
TSTPT_4	HI-Z	LOW
TSTPT_5	HI-Z	HIGH
TSTPT_6	HI-Z	HIGH
TSTPT_7	HI-Z	7.5 MHz

(1) These are default output selections. Software can reprogram the selection at any time.

7.3.9 DMD Interface

The DLPC3437 controller DMD interface consists of a HS 1.8-V sub-LVDS output only interface with a maximum clock speed of 600-MHz DDR and a LS SDR (1.8-V LVCMOS) interface with a fixed clock speed of 120 MHz.

7.3.9.1 Sub-LVDS (HS) Interface

Table 7-8 shows how the 8 sub-LVDS lanes are configured for the DLP3310 (.33 1080p) DMD.

Table 7-8. DLP3310 (.33 1080p) DMD – DLPC to 8-Lane DMD Pin Mapping

DLPC3437 8 LANE DMD ROUTING OPTION #1		
PRIMARY DLPC3437 PINS	**SECONDARY DLPC3437 PINS**	**DMD PINS**
HS_WDATA_D_P HS_WDATA_D_N	HS_WDATA_E_P HS_WDATA_E_N	Input DATA_p_0 Input DATA_n_0
HS_WDATA_C_P HS_WDATA_C_N	HS_WDATA_F_P HS_WDATA_F_N	Input DATA_p_1 Input DATA_n_1
HS_WDATA_B_P HS_WDATA_B_N	HS_WDATA_G_P HS_WDATA_G_N	Input DATA_p_2 Input DATA_n_2
HS_WDATA_A_P HS_WDATA_A_N	HS_WDATA_H_P HS_WDATA_H_N	Input DATA_p_3 Input DATA_n_3
HS_WDATA_H_P HS_WDATA_H_N	HS_WDATA_A_P HS_WDATA_A_N	Input DATA_p_4 Input DATA_n_4
HS_WDATA_G_P HS_WDATA_G_N	HS_WDATA_B_P HS_WDATA_B_N	Input DATA_p_5 Input DATA_n_5
HS_WDATA_F_P HS_WDATA_F_N	HS_WDATA_C_P HS_WDATA_C_N	Input DATA_p_6 Input DATA_n_6
HS_WDATA_E_P HS_WDATA_E_N	HS_WDATA_D_P HS_WDATA_D_N	Input DATA_p_7 Input DATA_n_7
DLPC3437 8 LANE DMD ROUTING OPTION #2		
PRIMARY DLPC3437 PINS	**SECONDARY DLPC3437 PINS**	**DMD PINS**
HS_WDATA_E_P HS_WDATA_E_N	HS_WDATA_D_P HS_WDATA_D_N	Input DATA_p_0 Input DATA_n_0
HS_WDATA_F_P HS_WDATA_F_N	HS_WDATA_C_P HS_WDATA_C_N	Input DATA_p_1 Input DATA_n_1
HS_WDATA_G_P HS_WDATA_G_N	HS_WDATA_B_P HS_WDATA_B_N	Input DATA_p_2 Input DATA_n_2
HS_WDATA_H_P HS_WDATA_H_N	HS_WDATA_A_P HS_WDATA_A_N	Input DATA_p_3 Input DATA_n_3
HS_WDATA_A_P HS_WDATA_A_N	HS_WDATA_H_P HS_WDATA_H_N	Input DATA_p_4 Input DATA_n_4
HS_WDATA_B_P HS_WDATA_B_N	HS_WDATA_G_P HS_WDATA_G_N	Input DATA_p_5 Input DATA_n_5
HS_WDATA_C_P HS_WDATA_C_N	HS_WDATA_F_P HS_WDATA_F_N	Input DATA_p_6 Input DATA_n_6

Table 7-8. DLP3310 (.33 1080p) DMD – DLPC to 8-Lane DMD Pin Mapping (continued)

DLPC3437 8 LANE DMD ROUTING OPTION #1		
HS_WDATA_D_P HS_WDATA_D_N	HS_WDATA_E_P HS_WDATA_E_N	Input DATA_p_7 Input DATA_n_7

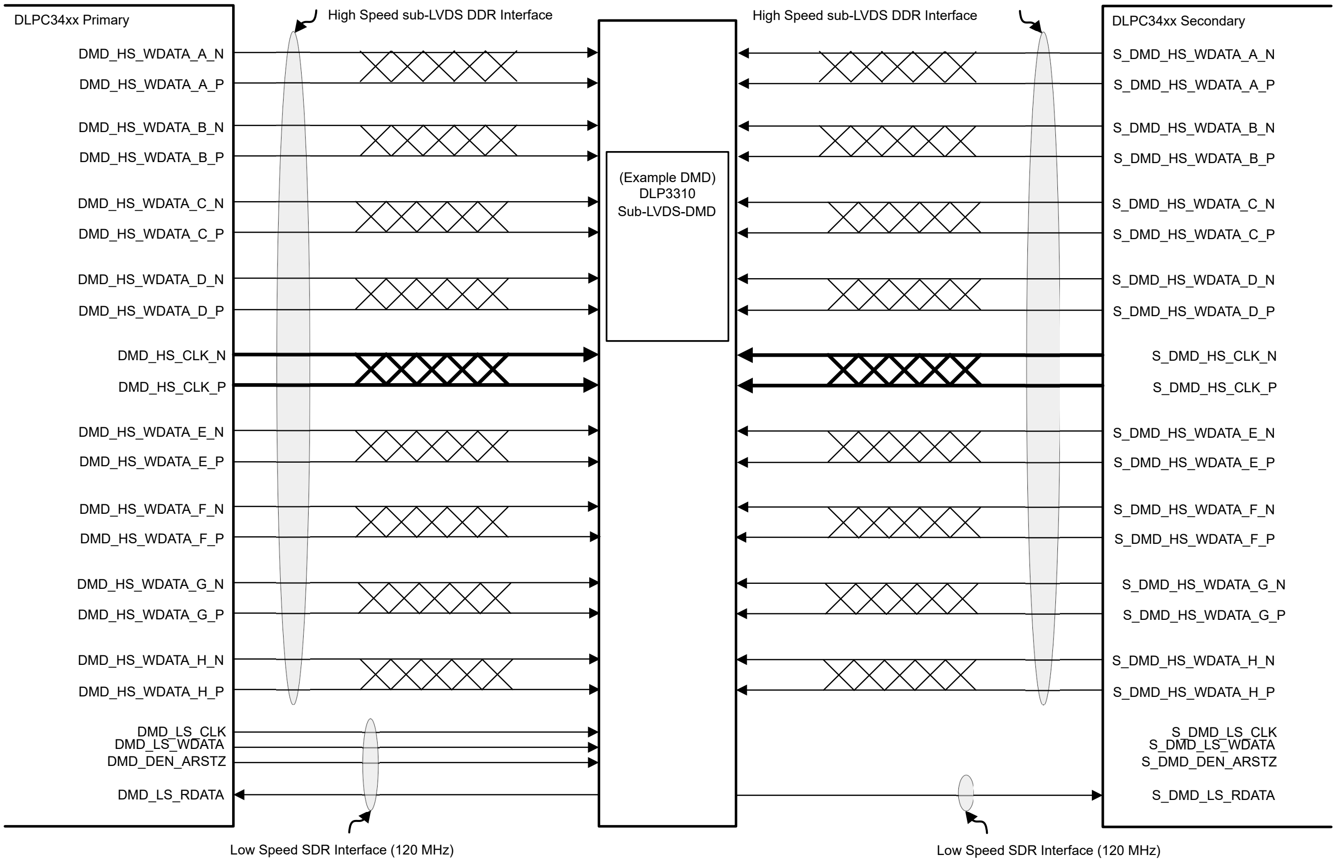


Figure 7-12. DLP3310 (.33 1080p) DMD Interface Example (Option 1 and 2)

The sub-LVDS high-speed interface waveform quality and timing on the DLPC34xx controller depends on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the *DMD Control and Sub-LVDS Signals* layout section is provided as a reference of an interconnect system that satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB signal integrity). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.

7.4 Device Functional Modes

The DLPC34xx controller has two functional modes (ON and OFF) controlled by a single pin, PROJ_ON (GPIO_08).

- When the PROJ_ON pin is set high, the controller powers up and can be programmed to send data to the DMD.
- When the PROJ_ON pin is set low, the controller powers down and consumes minimal power.

7.5 Programming

The DLPC34xx controller contains an Arm® Cortex®-M3 processor with additional functional blocks to enable video processing and control. TI provides software as a firmware image. The customer is required to flash this firmware image onto the SPI flash memory. The DLPC34xx controller loads this firmware during startup and regular operation. The controller and its accompanying DLP chipset requires this proprietary software to operate. The available controller functions depend on the firmware version installed. Different firmware is required for different chipset combinations (such as when using different PMIC devices). See *Documentation Support* at the end of this document or contact TI to view or download the latest published software.

Users can modify software behavior through I^2C interface commands. For a list of commands, view the software user's guide accessible through the *Documentation Support* page.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DLPC3437 controller is required to be coupled with DLP3310 (0.33 1080p) DMD to provide a reliable display solution for various data and video display applications. DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the chipset.

Click on these links to find more information about Applications of interest: Mobile Smart TV, DLP Signage, Mobile projector, Commercial gaming displays, Pico projectors, and Smart home displays.

8.2 Typical Application

A common application when using a DLPC3437 controller with DLP3310 DMD and DLPA300X PMIC/LED driver is for creating an accessory Pico projector. A functional block diagram of a typical Pico projector is shown in Figure 8-1.

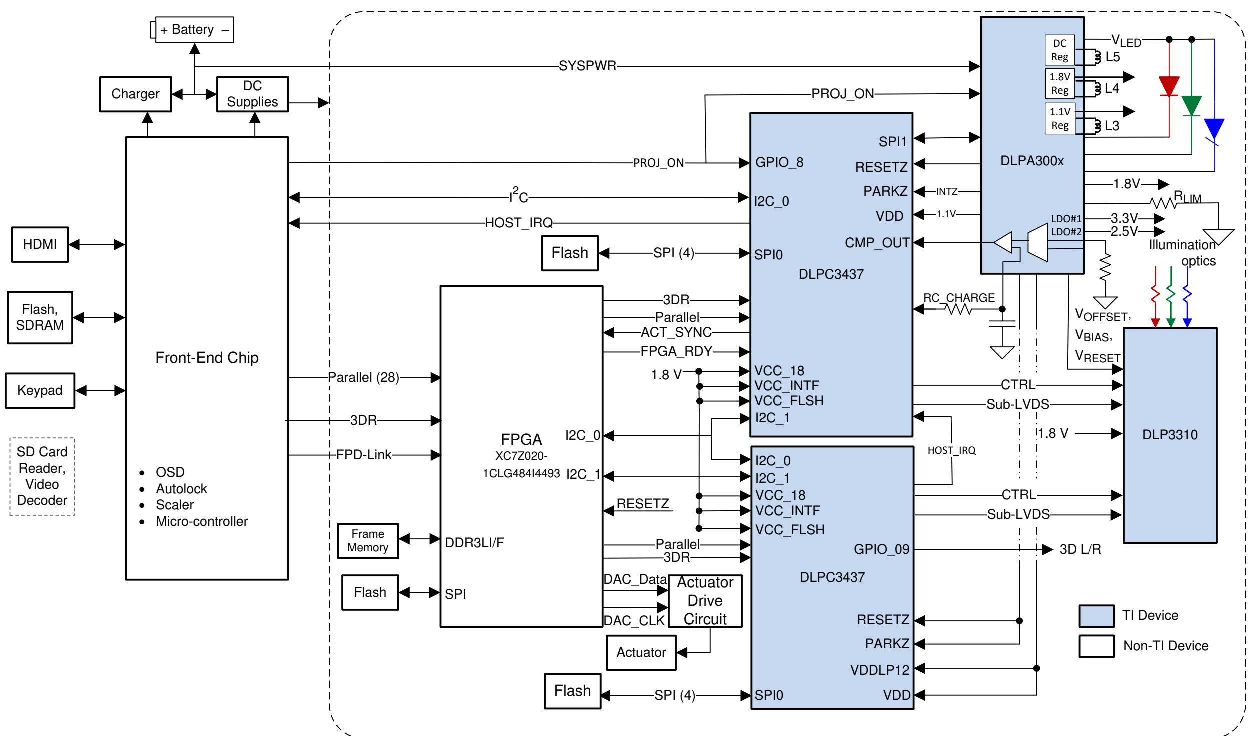


Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

A Pico projector can be created by using the DLP chipset that includes the DLP3310 (.33 1080p) DMD, 2xDLPC3437 controller, a XC7Z020-1CLG484I4493 FPGA, and DLPA300X PMIC/LED driver. The DLPC3437 and FPGA do the digital image processing, the DLPA300X PMIC provides the needed analog functions for the projector, and the DMD displays the projection.

In addition to the four DLP chips in the chipset, other chips can be needed. At a minimum, flash memories are needed to store the software and firmware to control the two DLPC3437s and the FPGA.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These LEDs are often contained in three separate packages, but sometimes more than one color of LED die can be in the same package to reduce the overall size of the pico-projector.

The entire pico-projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR. When PROJ_ON is set low, the 1.8-V supply can continue to be left at 1.8 V and used by other non-projector sections of the product. If PROJ_ON is low, the DLPA300X does not draw current on the 1.8-V supply.

8.2.2 Detailed Design Procedure

For connecting together the DLP3310 (.33 1080p) DMD, 2xDLPC3437 controller, XC7Z020-1CLG484I4493 FPGA, and DLPA3000 PMIC/LED driver, see the reference design schematic and board layoutTIDA-00325. When a circuit board layout is created from this schematic a very small circuit board is possible. Follow the layout guidelines to achieve a reliable projector.

Typically an optical engine manufacturer supplies the optical engine that includes the LED packages and a mounted DMD. These manufacturers specialize in designing optics for DLP projectors. There exists production-ready optical modules, optical module manufacturers, and design houses.

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is shown in Figure 8-2 when using the DLPA3000. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs.

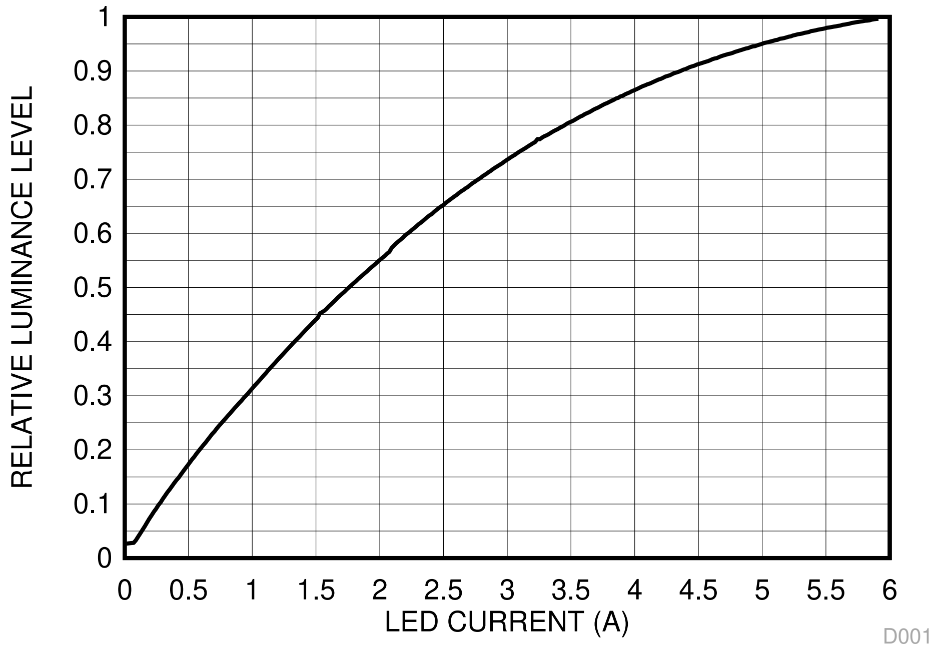


Figure 8-2. Typical Luminance vs Current

9 Power Supply Recommendations

9.1 PLL Design Considerations

It is acceptable for the VDD_PLLD and VDD_PLLM to be derived from the same regulator as the core VDD. However, to minimize the AC noise component, apply a filter as recommended in the *PLL Power Layout* section.

9.2 System Power-Up and Power-Down Sequence

Although the DLPC3437 requires an array of power supply voltages, (for example, VDD, VDDLP12, VDD_PLLM/D, VCC18, VCC_FLSH, VCC_INTF), since VDDLP12 is tied to the 1.1-V VDD supply, then there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC3437 (true for both power-up and power-down scenarios). Similarly, there is no minimum time between powering-up or powering-down the different supplies if VDDLP12 is tied to the 1.1-V VDD supply.

Although there is no risk of damaging the DLPC3437 if the above power sequencing rules are followed, the following additional power sequencing recommendations must be considered to ensure proper system operation.

- To ensure that DLPC3437 output signal states behave as expected, all DLPC3437 I/O supplies must remain applied while VDD core power is applied. If VDD core power is removed while the I/O supply (VCC_INTF) is applied, then the output signal state associated with the inactive I/O supply goes into a high impedance state.
- Additional power sequencing rules can exist for devices that share the supplies with the DLPC3437, and thus these devices may force additional system power sequencing requirements.

Note that when VDD core power is applied, but I/O power is not applied, additional leakage current may be drawn. This added leakage does not affect normal DLPC3437 operation or reliability.

Figure 9-1 and Figure 9-2 show the DLPC3437 power-up and power-down sequence for both the normal PARK and fast PARK operations of the DLPC3437 controller.

Note

During a Normal Park, it is recommended to maintain SYSPWR within specification for at least 50 ms after PROJ_ON goes low to allow the DMD to be parked and the power supply rails to safely power down. After 50 ms, SYSPWR can be turned off. If a DLPA200x is used, it is also recommended that the 1.8-V supply fed into the DLPA200x load switch be maintained within specification for at least 50 ms after PROJ_ON goes low.

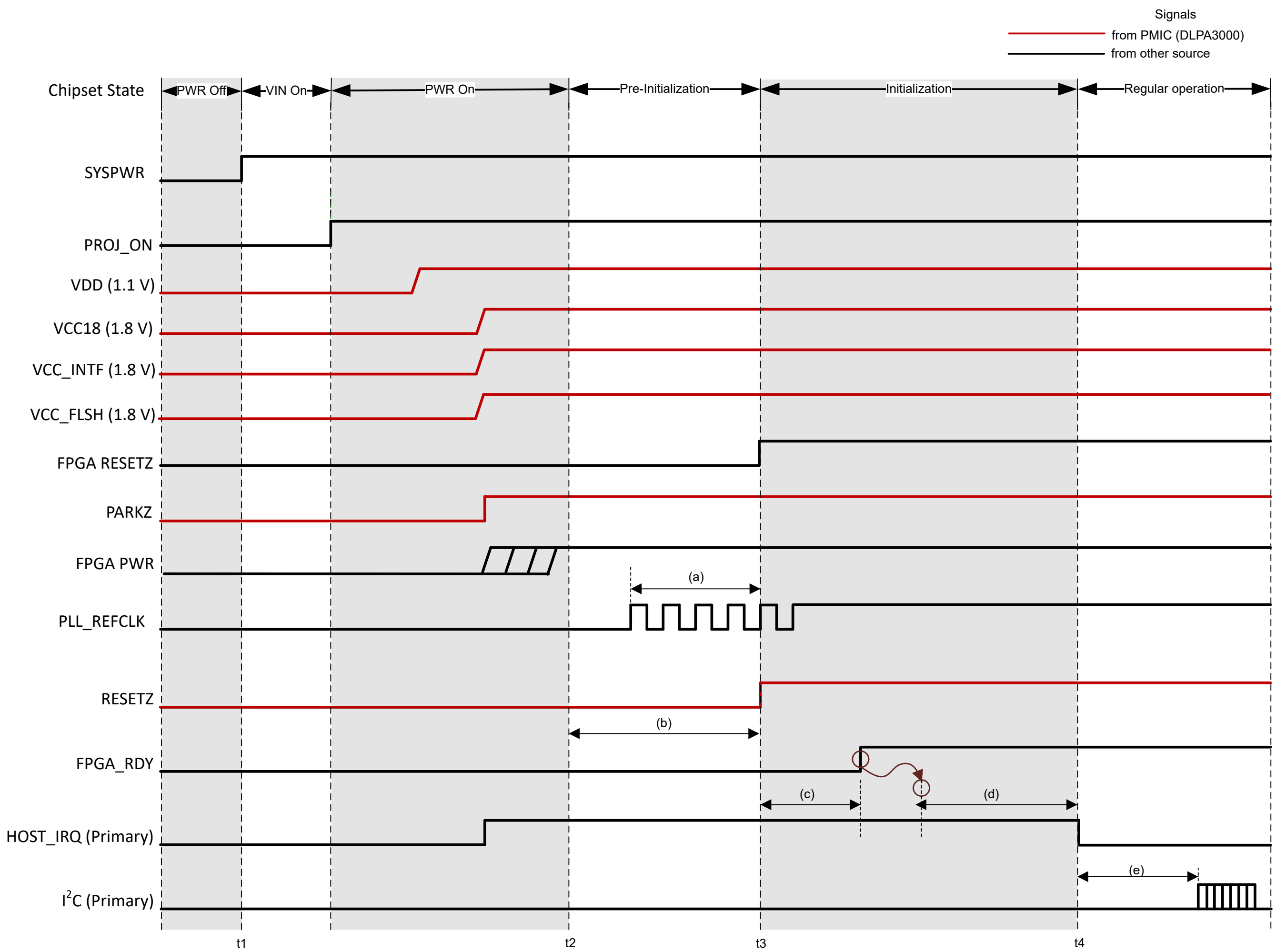


Figure 9-1. DLPC3437 Power-Up Timing

t1:	(VIN) applied to the PMIC. All other voltage rails are derived from SYSPWR.
t2:	All supplies reach 95% of their specified nominal value. Note HOST_IRQ may go high sooner if it is pulled-up to a different external supply.
t3:	Point where RESETZ is deasserted (goes high). Indicates the beginning of the controller auto-initialization routine.
t4:	HOST_IRQ goes low to indicate initialization is complete. I2C is now ready to accept commands.
(a):	The typical delay between the PLL reference clock becoming active and RESETZ being deasserted (going high) is less than 1 ms. PLL_REFCLK must be stable within 5 ms of all power being applied, and may be active before power is applied.
(b):	RESETZ must also be held low for at least 5 ms after the power supplies are in specification.
(c):	There is a typical delay of 1.5 s between being FPGA RESETZ being deasserted and FPGA_RDY being asserted (going high). This duration is due to FPGA boot logic.
(d):	There is a typical controller boot time of 100 ms. PARKZ must be high before RESETZ releases to support auto-initialization.
(e):	There is a typical FPGA setup time of 2.75 ms before the system completes boot process. During this period, the DLPC3437 controller writes startup values to the FPGA registers. After FPGA setup is complete, I^{2}C now accepts commands.

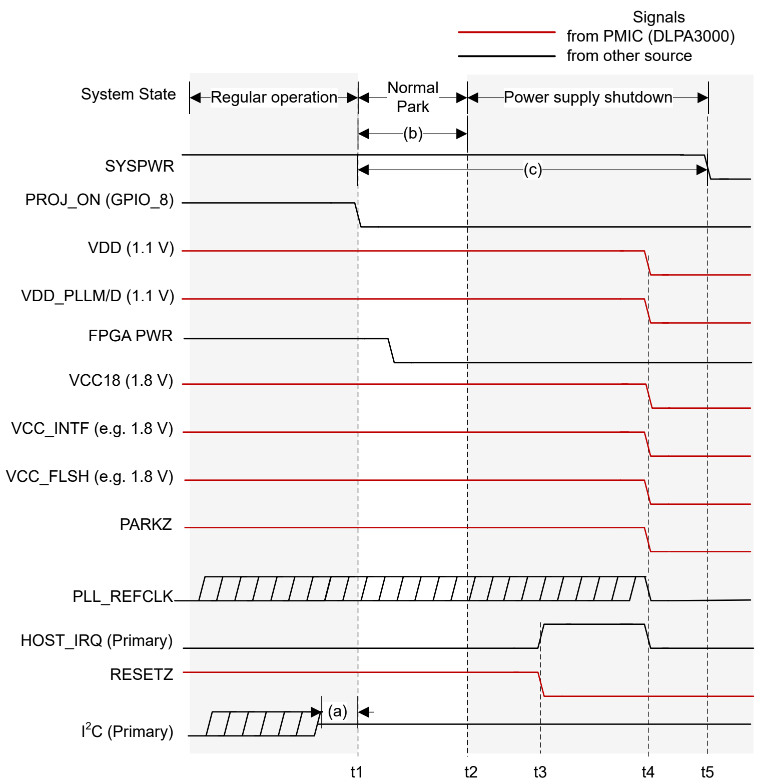


Figure 9-2. DLPC3437 Normal Power-Down

t1:	PROJ_ON goes low to begin the power down sequence.
t2:	The controller finishes parking the DMD.
t3:	RESETZ is asserted which causes HOST_IRQ to be pulled high.
t4:	All controller power supplies are turned off.
t5:	SYSPWR is removed now that all other supplies are turned off.
(a):	I^2C activity must stop before PROJ_ON is deasserted (goes low).
(b):	The DMD parks within 20 ms of PROJ_ON being deasserted (going low). VDD, VDD_PLLM/D, VCC18, VCC_INITF, and VCC_FLSH power supplies and the PLL_REFCLK must be held within specification for a minimum of 20 ms after PROJ_ON is deasserted (goes low). However, 20 ms does not satisfy the typical shutdown timing of the entire chipset. Follow note (c).
(c):	Do not turn off SYSPWR until at least 50 ms after PROJ_ON is deasserted (goes low). This time allows the DMD to be parked, the controller to turn off, and the PMIC supplies to shut down.

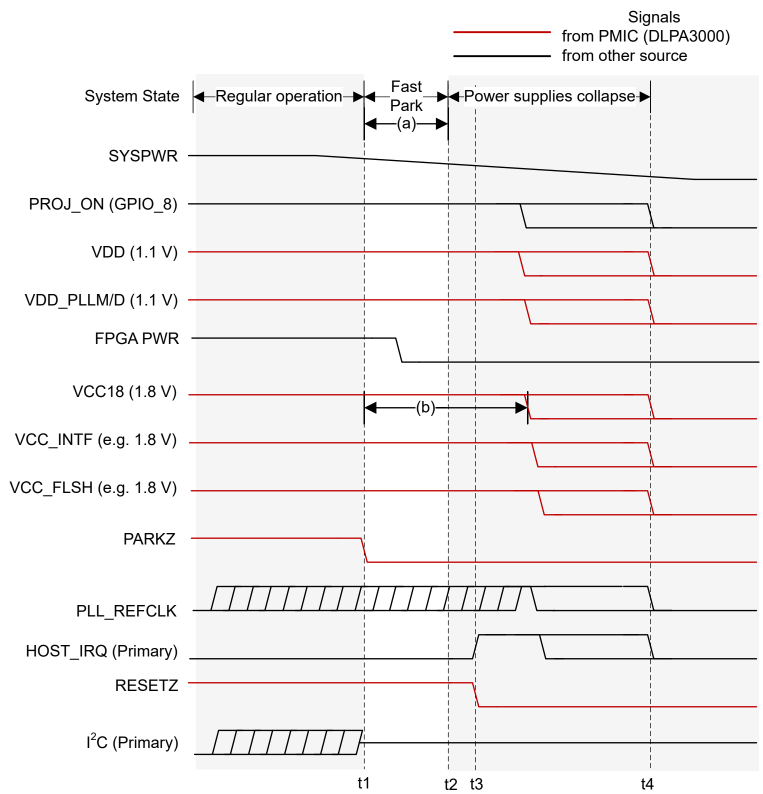


Figure 9-3. DLPC3437 Fast Power-Down

t1: A fault is detected (in this example the PMIC detects a UVLO condition) and PARKZ is asserted (goes low) to tell the controller to initiate a fast park of the DMD.

t2: The controller finishes the fast park procedure.

t3: RESETZ is asserted which puts the controller in a reset state which causes HOST_IRQ to be pulled high.

t4: Eventually all power supplies that were derived from SYSPWR collapse.

(a): VDD, VDD_PLLM/D, VCC18, VCC_INITF, and VCC_FLSH power supplies and the PLL_REFCLK must be held within specification for a minimum of 32 µs after PARKZ is asserted (goes low).

(b): VCC18 must remain in specification long enough to satisfy DMD power sequencing requirements defined in the DMD datasheet. Also see the DLPAxxxx datasheets for more information.

9.3 Power-Up Initialization Sequence

An external power monitor is required to hold the DLPC34xx controller in system reset during the power-up sequence by driving RESETZ to a logic-low state. It shall continue to drive RESETZ low until all controller voltages reach the minimum specified voltage levels, PARKZ goes high, and the input clocks are stable. The external power monitoring is automatically done by the DLPAxxxx PMIC.

No signals output by the DLPC34xx controller will be in their active state while RESETZ is asserted. The following signals are tri-stated while RESETZ is asserted:

- SPI0_CLK
- SPI0_DOUT
- SPI0_CSZ0
- SPI0_CSZ1
- GPIO [19:00]

Add external pullup (or pulldown) resistors to all tri-stated output signals (including bidirectional signals to be configured as outputs) to avoid floating controller outputs during reset if they are connected to devices on the PCB that can malfunction. For SPI, at a minimum, include a pullup to any chip selects connected to devices. Unused bidirectional signals can be configured as outputs in order to avoid floating controller inputs after RESETZ is set high.

The following signals are forced to a logic low state while RESETZ is asserted and the corresponding I/O power is applied:

- LED_SEL_0
- LED_SEL_1
- DMD_DEN_ARSTZ

After power is stable and the PLL_REFCLK_I clock input to the DLPC34xx controller is stable, then RESETZ should be deactivated (set to a logic high). The DLPC34xx controller then performs a power-up initialization routine that first locks its PLL followed by loading self configuration data from the external flash. Upon release of RESETZ, all DLPC34xx I/Os will become active. Immediately following the release of RESETZ, the HOST_IRQ signal will be driven high to indicate that the auto initialization routine is in progress. However, since a pullup resistor is connected to signal HOST_IRQ, this signal will have already gone high before the controller actively drives it high. Upon completion of the auto-initialization routine, the DLPC34xx controller will drive HOST_IRQ low to indicate the initialization done state of the controller has been reached.

To ensure reliable operation, during the power-up initialization sequence, GPIO_08 (PROJ_ON) must not be deasserted. In other words, once the startup routine has begun (by asserting PROJ_ON), the startup routine must complete (indicated by HOST_IRQ going low) before the controller can be commanded off (by deasserting PROJ_ON).

Note

No I^2C or DSI (if applicable) activity is permitted until HOST_IRQ goes low.

9.4 DMD Fast PARK Control (PARKZ)

PARKZ is an input early warning signal that must alert the controller at least 32 µs before DC supply voltages drop below specifications. Typically, the PARKZ signal is provided by the DLPAxxxx interrupt output signal. PARKZ must be deasserted (set high) prior to releasing RESETZ (that is, prior to the low-to-high transition on the RESETZ input) for normal operation. When PARKZ is asserted (set low) the controller performs a Fast Park operation on the DMD which assists in maintaining the lifetime of the DMD. The reference clock must continue running and RESETZ must remain deactivated for at least 32 µs after PARKZ has been asserted (set low) to allow the park operation to complete.

Fast Park operation is only intended for use when loss of power is imminent and beyond the control of the host processor (for example, when the external power source has been disconnected or the battery has dropped below a minimum level). The longest lifetime of the DMD may not be achieved with Fast Park operation.

The longest lifetime is achieved with a Normal Park operation (initiated through GPIO_08). Hence, PARKZ is typically only used instead of a Normal Park request if there is not enough time for a Normal Park. A Normal Park operation takes much longer than 40 µs to park the mirrors. During a Normal Park operation, the DLPAxxxx keeps on all power supplies, and keeps RESETZ high, until the longer mirror parking has completed. Additionally, the DLPAxxxx may hold the supplies on for a period of time after the parking has been completed. View the relevant DLPAxxxx datasheet for more information. The longer mirror parking time ensures the longest DMD lifetime and reliability. Section 6.17 specifies the park timings

9.5 Hot Plug I/O Usage

The DLPC34xx controller provides fail-safe I/O on all host interface signals (signals powered by VCC_INTF). This allows these inputs to externally be driven even when no I/O power is applied. Under this condition, the controller does not load the input signal nor draw excessive current that could degrade controller reliability. For example, the I^2C bus from the host to other components is not affected by powering off VCC_INTF to the DLPC34xx controller. The allows additional devices on the I^2C bus to be utilized even if the controller is not powered on. TI recommends weak pullup or pulldown resistors to avoid floating inputs for signals that feed back to the host.

If the I/O supply (VCC_INTF) powers off, but the core supply (VDD) remains on, then the corresponding input buffer may experience added leakage current; however, the added leakage current does not damage the DLPC34xx controller.

However, if VCC_INTF is powered and VDD is not powered, the controller may drives the IIC0_xx pins low which prevents communication on this I^2C bus. Do not power up the VCC_INTF pin before powering up the VDD pin for any system that has additional target devices on this bus.

10 Layout

10.1 Layout Guidelines

For a summary of the PCB design requirements for the DLPC34xx controller see *PCB Design Requirements for TI DLP Pico TRP Digital Micromirror Devices*. Some applications (such as high frame rate video) may require the use of 1-oz (or greater) copper planes to manage the controller package heat.

10.1.1 PLL Power Layout

Follow these recommended guidelines to achieve acceptable controller performance for the internal PLL. The DLPC34xx controller contains two internal PLLs which have dedicated analog supplies (VDD_PLLM, VSS_PLLM, VDD_PLLD, and VSS_PLLD). At a minimum, isolate the VDD_PLLx power and VSS_PLLx ground pins using a simple passive filter consisting of two series ferrite beads and two shunt capacitors (to widen the spectrum of noise absorption). It is recommended that one capacitor be 0.1 µF and one be 0.01 µF. Place all four components as close to the controller as possible. It is especially important to keep the leads of the high frequency capacitors as short as possible. Connect both capacitors from VDD_PLLM to VSS_PLLM and VDD_PLLD to VSS_PLLD on the controller side of the ferrite beads.

Select ferrite beads with these characteristics:

- DC resistance less than 0.40 Ω
- Impedance at 10 MHz equal to or greater than 180 Ω
- Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the DLPC34xx controller to both capacitors and then through the series ferrites to the power source. Make the power and ground traces as short as possible, parallel to each other, and as close as possible to each other.

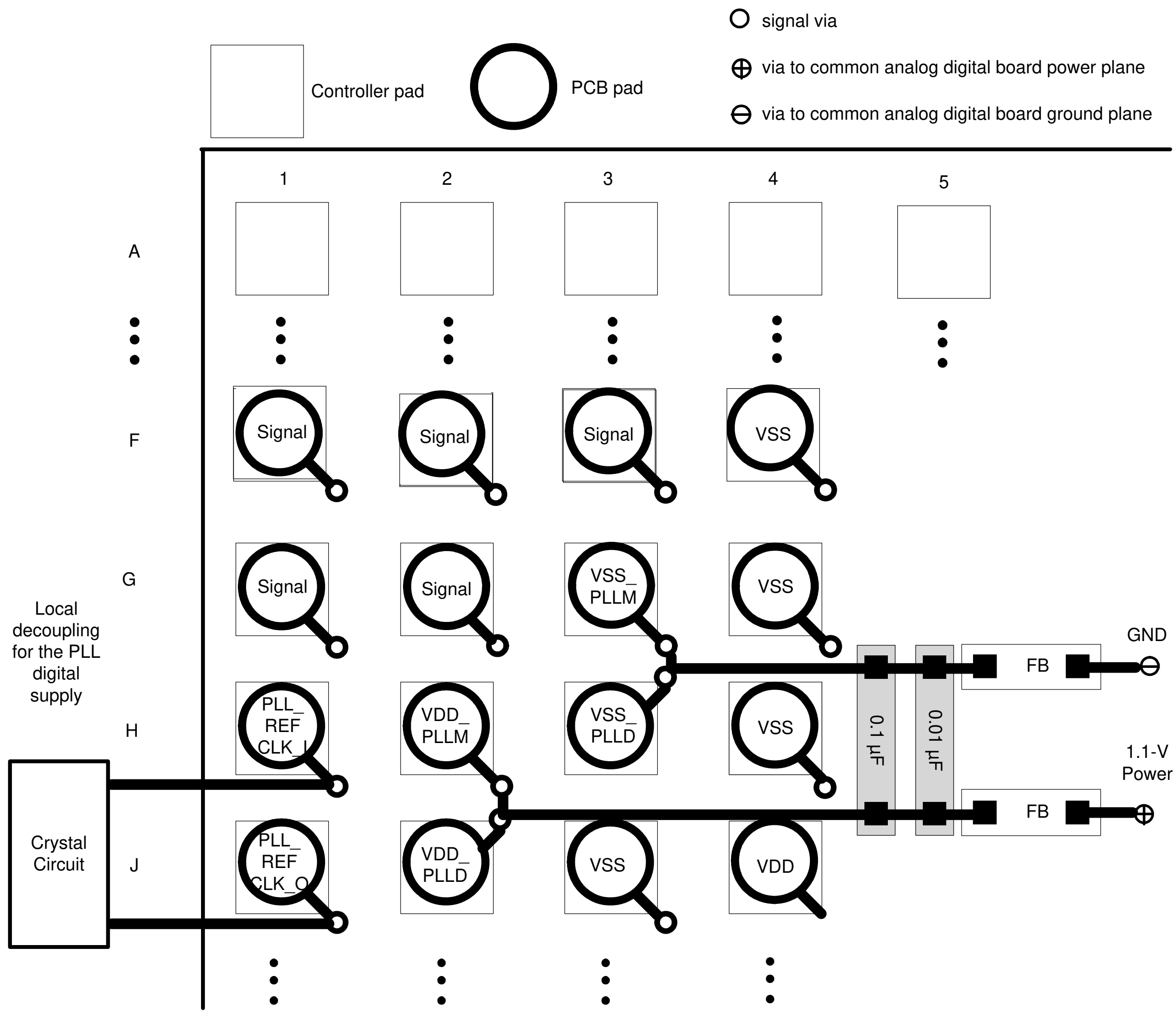
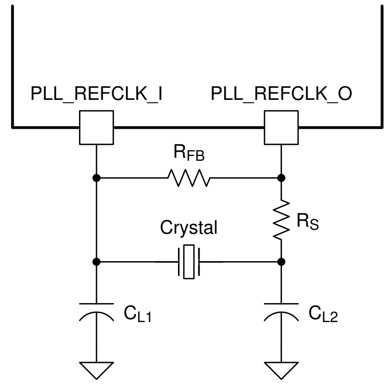


Figure 10-1. PLL Filter Layout

10.1.2 Reference Clock Layout

The DLPC34xx controller requires an external reference clock to feed the internal PLL. Use either a crystal or oscillator to supply this reference. The DLPC34xx reference clock must not exceed a frequency variation of ±200 ppm (including aging, temperature, and trim component variation).

Figure 10-2 shows the required discrete components when using a crystal.



C_L = Crystal load capacitance (farads)
$C_{L1} = 2 \times (C_L - Cstray\_pll\_refclk\_i)$
$C_{L2} = 2 \times (C_L - Cstray\_pll\_refclk\_o)$
where:

- Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the controller pin pll_refclk_i.
- Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the controller pin pll_refclk_o.

Figure 10-2. Required Discrete Components

10.1.2.1 Recommended Crystal Oscillator Configuration

Table 10-1. Crystal Port Characteristics

PARAMETER	NOM	UNIT
PLL_REFCLK_I TO GND capacitance	1.5	pF
PLL_REFCLK_O TO GND capacitance	1.5	pF

Table 10-2. Recommended Crystal Configuration

PARAMETER (1) (2)	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	24	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±200	PPM
Maximum startup time	1.0	ms
Crystal equivalent series resistance (ESR)	120 (max)	Ω
Crystal load	6	pF
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor	See equation in Figure 10-2 notes	pF
C_{L2} external crystal load capacitor	See equation in Figure 10-2 notes	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) Temperature range of –30°C to 85°C.
(2) The crystal bias is determined by the controllers VCC_INTF voltage rail, which is variable (not the VCC18 rail).

If an external oscillator is used, then the oscillator output must drive the PLL_REFCLK_I pin on the DLPC34xx controller, and the PLL_REFCLK_O pin must be left unconnected.

Table 10-3. Recommended Crystal Parts

MANUFACTURER (1) (2)	PART NUMBER	SPEED (MHz)	TEMPERATURE AND AGING (ppm)	MAXIMUM ESR (Ω)	LOAD CAPACITANCE (pF)	PACKAGE DIMENSIONS (mm)
KDS	DSX211G-24.000M-8pF-50-50	24	±50	120	8	2.0 × 1.6
Murata	XRCGB24M000F0L11R0	24	±100	120	6	2.0 × 1.6
NDK	NX2016SA 24M EXS00A-CS05733	24	±145	120	6	2.0 × 1.6

(1) The crystal devices in this table have been validated to work with the DLPC34xx controller. Other devices may also be compatible but have not necessarily been validated by TI.
(2) Operating temperature range: –30°C to 85°C for all crystals.

10.1.3 Unused Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends tying unused controller input pins through a pullup resistor to its associated power supply or a pulldown resistor to ground. For controller inputs with internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Note that internal pullup and pulldown resistors are weak and should not be expected to drive an external device. The DLPC34xx controller implements very few internal resistors and are listed in the tables found in the *Pin Configuration and Functions* section. When external pullup or pulldown resistors are needed for pins that have weak pullup or pulldown resistors, choose a maximum resistance of 8 kΩ.

Never tie unused output-only pins directly to power or ground. Leave them open.

When possible, TI recommends that unused bidirectional I/O pins are configured to their output state such that the pin can remain open. If this control is not available and the pins may become an input, then include an appropriate pullup (or pulldown) resistor.

10.1.4 DMD Control and Sub-LVDS Signals

Table 10-4. Maximum Pin-to-Pin PCB Interconnect Recommendations

DMD BUS SIGNAL(1) (2)	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE-BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 (152.4)	See (3)	in (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N	6.0 (152.4)	See (3)	in (mm)
DMD_LS_CLK	6.5 (165.1)	See (3)	in (mm)
DMD_LS_WDATA	6.5 (165.1)	See (3)	in (mm)
DMD_LS_RDATA	6.5 (165.1)	See (3)	in (mm)
DMD_DEN_ARSTZ	7.0 (177.8)	See (3)	in (mm)

(1) Maximum signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to PCB variations, these recommendations cannot be defined. Any board design should SPICE simulate with the controller IBIS model (found under the *Tools & Software* tab of the controller web page) to ensure routing lengths do not violate signal requirements.

Table 10-5. High Speed PCB Signal Routing Matching Requirements

SIGNAL GROUP LENGTH MATCHING(1) (2) (3)				
INTERFACE	**SIGNAL GROUP**	**REFERENCE SIGNAL**	**MAX MISMATCH(4)**	**UNIT**
DMD(5)	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	in (mm)
DMD	DMD_HS_WDATA_x_P	DMD_HS_WDATA_x_N	±0.025 (±0.635)	in (mm)
DMD	DMD_HS_CLK_P	DMD_HS_CLK_N	±0.025 (±0.635)	in (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	in (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	in (mm)

(1) The length matching values apply to PCB routing lengths only. Internal package routing mismatch associated with the DLPC34xx controller or the DMD require no additional consideration.
(2) Training is applied to DMD HS data lines. This is why the defined matching requirements are slightly relaxed compared to the LS data lines.
(3) DMD LS signals are single ended.
(4) Mismatch variance for a signal group is always with respect to the reference signal.
(5) DMD HS data lines are differential, thus these specifications are pair-to-pair.

Table 10-6. Signal Requirements

PARAMETER	REFERENCE	REQUIREMENT
Source series termination	DMD_LS_WDATA	Required
	DMD_LS_CLK	Required
	DMD_DEN_ARSTZ	Acceptable
	DMD_LS_RDATA	Required
	DMD_HS_WDATA_x_y	Not acceptable
	DMD_HS_CLK_y	Not acceptable
Endpoint termination	DMD_LS_WDATA	Not acceptable
	DMD_LS_CLK	Not acceptable
	DMD_DEN_ARSTZ	Not acceptable
	DMD_LS_RDATA	Not acceptable
	DMD_HS_WDATA_x_y	Not acceptable
	DMD_HS_CLK_y	Not acceptable
PCB impedance	DMD_LS_WDATA	68 Ω ±10%
	DMD_LS_CLK	68 Ω ±10%
	DMD_DEN_ARSTZ	68 Ω ±10%
	DMD_LS_RDATA	68 Ω ±10%
	DMD_HS_WDATA_x_y	100 Ω ±10%
	DMD_HS_CLK_y	100 Ω ±10%
Signal type	DMD_LS_WDATA	SDR (single data rate) referenced to DMD_LS_DCLK
	DMD_LS_CLK	SDR referenced to DMD_LS_DCLK
	DMD_DEN_ARSTZ	SDR
	DMD_LS_RDATA	SDR referenced to DMD_LS_DLCK
	DMD_HS_WDATA_x_y	sub-LVDS
	DMD_HS_CLK_y	sub-LVDS

10.1.5 Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers. Ideally ensure that the signals of a given pair do not change layers.

10.1.6 Stubs

- Avoid using stubs.

10.1.7 Terminations

- DMD_HS differential signals require no external termination resistors.
- Make sure the DMD_LS_CLK and DMD_LS_WDATA signal paths include a 43-Ω series termination resistor located as close as possible to the corresponding controller pins.
- Make sure the DMD_LS_RDATA signal path includes a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- The DMD_DEN_ARSTZ pin requires no series resistor.

10.1.8 Routing Vias

- The number of vias on DMD_HS signals must be minimized and ideally not exceed two.
- Any and all vias on DMD_HS signals must be located as close to the controller as possible.
- The number of vias on the DMD_LS_CLK and DMD_LS_WDATA signals must be minimized and ideally not exceed two.
- Any and all vias on the DMD_LS_CLK and DMD_LS_WDATA signals must be located as close to the controller as possible.

10.1.9 Thermal Considerations

The underlying thermal limitation for the DLPC34xx controller is that the maximum operating junction temperature (T_J) not be exceeded (this is defined in the *Recommended Operating Conditions* section).

Some factors that influence T_J are as follows:

- operating ambient temperature
- airflow
- PCB design (including the component layout density and the amount of copper used)
- power dissipation of the DLPC34xx controller
- power dissipation of surrounding components

The controller package is designed to primarily extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

The recommends maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum DLPC34xx controller power dissipation and $R_{\theta JA}$ at 0 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB with two, 1-oz power planes. This JEDEC test PCB is not necessarily representative of the DLPC34xx controller PCB, so the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. TI highly recommended that thermal performance be measured and validated after the PCB is designed and the application is built.

To evaluate the thermal performance, measure the top center case temperature under the worse case product scenario (maximum power dissipation, maximum voltage, maximum ambient temperature), and validate the controller does not exceed the maximum recommended case temperature (T_C). This specification is based on the measured φ_{JT} for the DLPC34xx controller package and provides a relatively accurate correlation to junction temperature.

Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. Place the bead and thermocouple wire so that they contact the top of the package. Cover the bead and thermocouple wire with a minimal amount of thermally conductive epoxy. Route the wires closely along the package and the board surface to avoid cooling the bead through the wires.

10.2 Layout Example

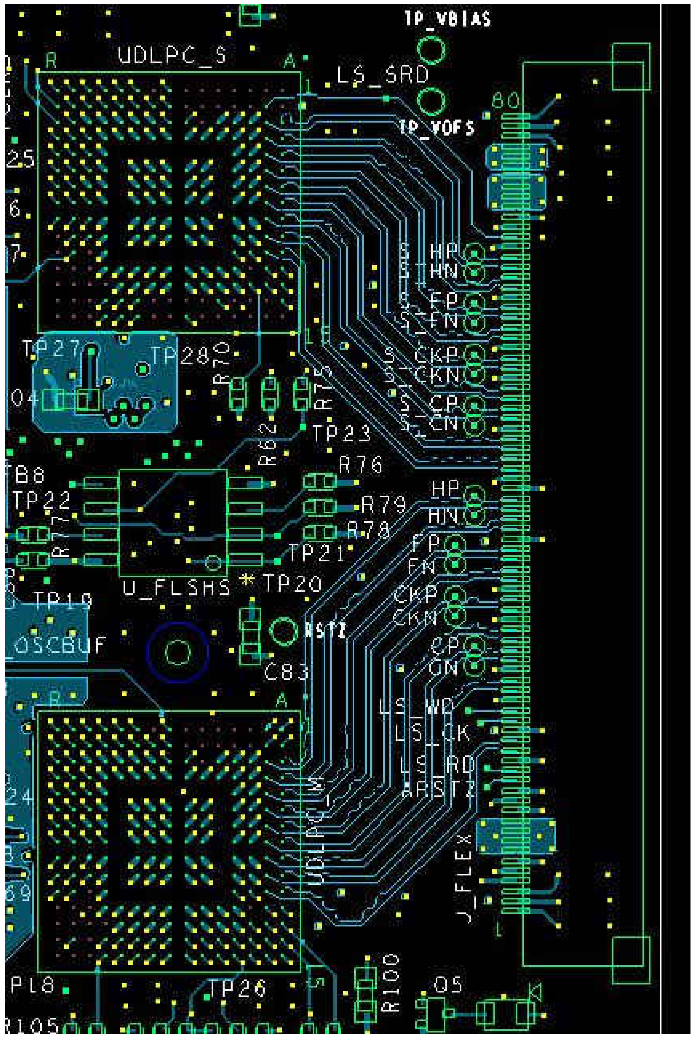


Figure 10-3. Board Layout

11 Device and Documentation Support

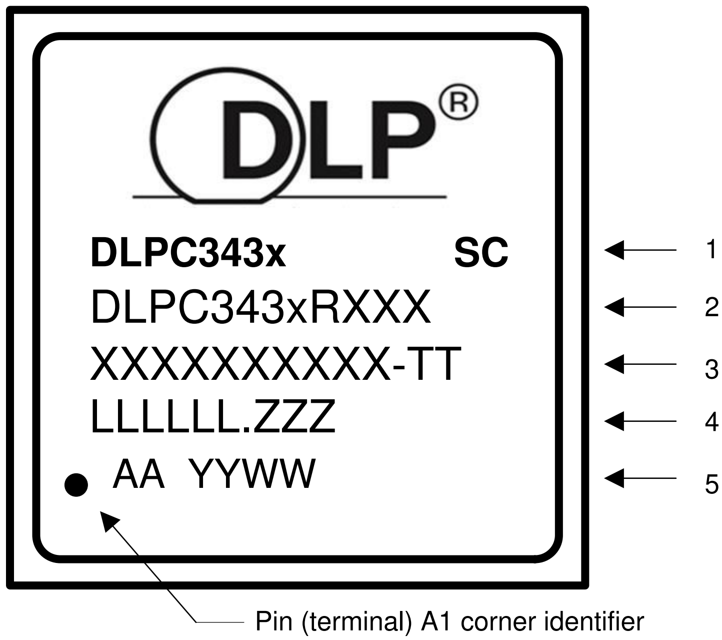
11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Device Nomenclature

11.1.2.1 Device Markings



Marking Definitions:

Line 1:	DLP® Device Name: DLPC343x where**x** is a "7" for this device. SC: Solder ball composition e1: Indicates lead-free solder balls consisting of SnAgCu G8: Indicates lead-free solder balls consisting of tin-silver-copper (SnAgCu) with silver content less than or equal to 1.5% and that the mold compound meets TI's definition of green.
Line 2:	TI Part Number DLP® Device Name: DLPC343x = **x** is a "7" for this device. **R** corresponds to the TI device revision letter for example A, B or C **XXX** corresponds to the device package designator.
Line 3:	XXXXXXXXXX-TT Manufacturer Part Number
Line 4:	LLLLLL.ZZZ Foundry lot code for semiconductor wafers LLLLLL: Fab lot number ZZZ: Lot split number
Line 5:	AA YYWW ES : Package assembly information **AA** corresponds to the manufacturing site YYWW: Date code (YY = Year :: WW = Week)

Note

1. Engineering prototype samples are marked with an **X** suffix appended to the TI part number. For example, 2512737-0001X.
2. See , for DLPC3437 resolutions on the DMD supported per part number.

11.1.2.2 Video Timing Parameter Definitions

See Figure 11-1 for a visual description.

Active Lines Per Frame (ALPF) Defines the number of lines in a frame containing displayable data. ALPF is a subset of the TLPF.

Active Pixels Per Line (APPL) Defines the number of pixel clocks in a line containing displayable data. APPL is a subset of the TPPL.

Horizontal Back Porch (HBP) Blanking Defines the number of blank pixel clocks after the active edge of horizontal sync but before the first active pixel.

Horizontal Front Porch (HFP) Blanking Defines the number of blank pixel clocks after the last active pixel but before horizontal sync.

Horizontal Sync (HS or Hsync) Timing reference point that defines the start of each horizontal interval (line). The active edge of the HS signal defines the absolute reference point. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.

Total Lines Per Frame (TLPF) Total number of active and inactive lines per frame; defines the vertical period (or frame time).

Total Pixel Per Line (TPPL) Total number of active and inactive pixel clocks per line; defines the horizontal line period in pixel clocks.

Vertical Sync (VS or Vsync) Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.

Vertical Back Porch (VBP) Blanking Defines the number of blank lines after the active edge of vertical sync but before the first active line.

Vertical Front Porch (VFP) Blanking Defines the number of blank lines after the last active line but before the active edge of vertical sync.

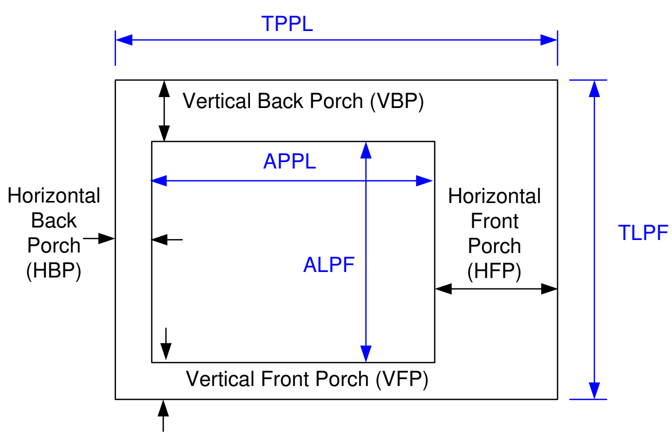


Figure 11-1. Parameter Definitions

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

IntelliBright™ and Link™ are trademarks of Texas Instruments.
Pico™ and TI E2E™ are trademarks of Texas Instruments.
DLP® is a registered trademark of Texas Instruments.
IntelliBright® is a registered trademark of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]	Op Temp (°C)	Device Marking[(4)] [(5)]
DLPC3437CZEZ	ACTIVE	NFBGA	ZEZ	201	160	TBD	Call TI	Level-3-260C-168 HRS	–30 to 85°C	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

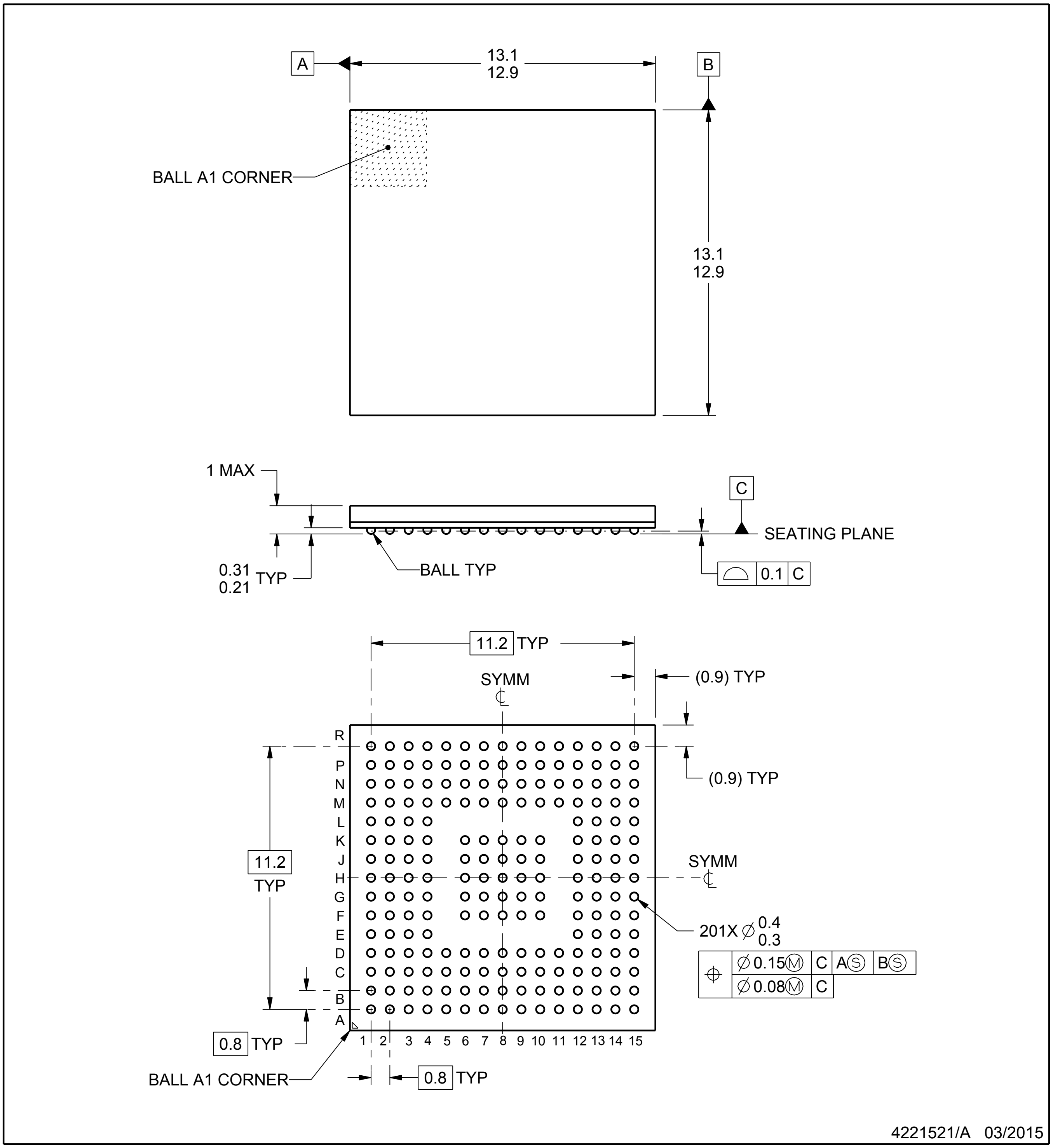
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

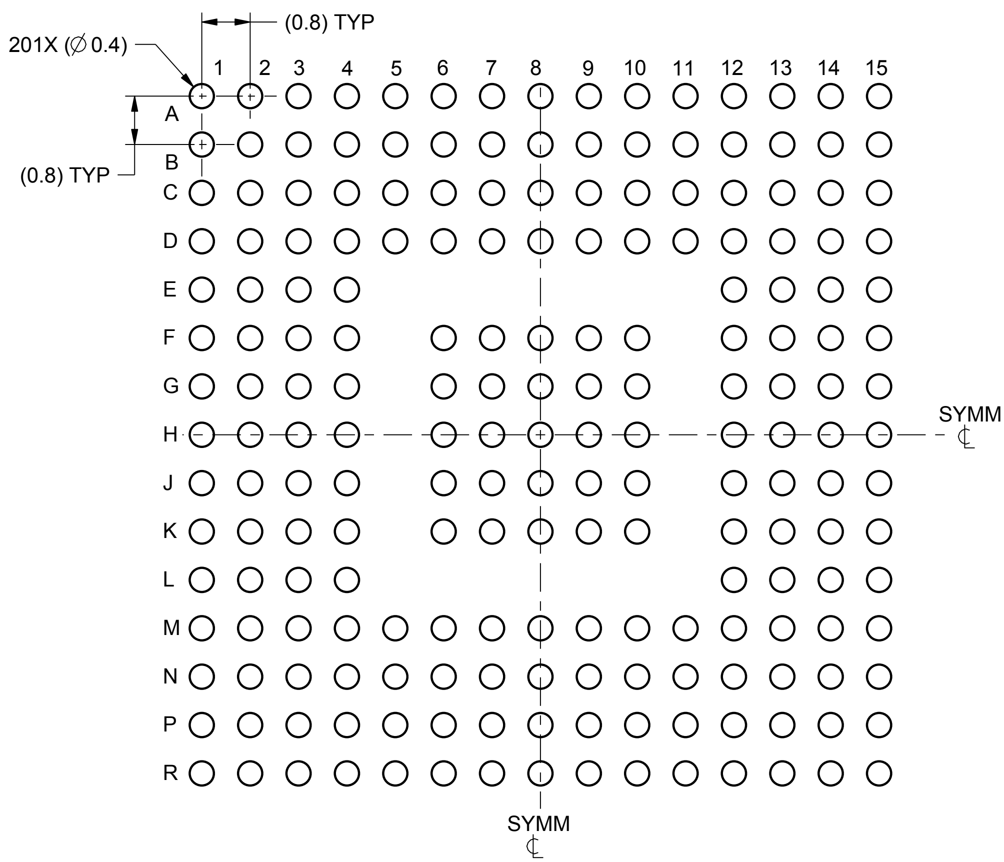
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

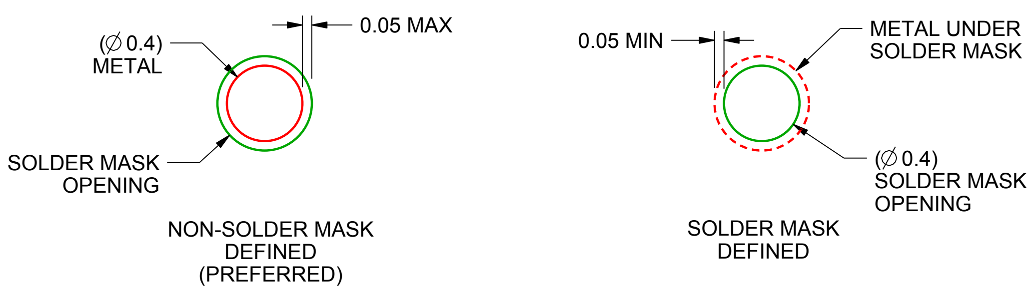


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X

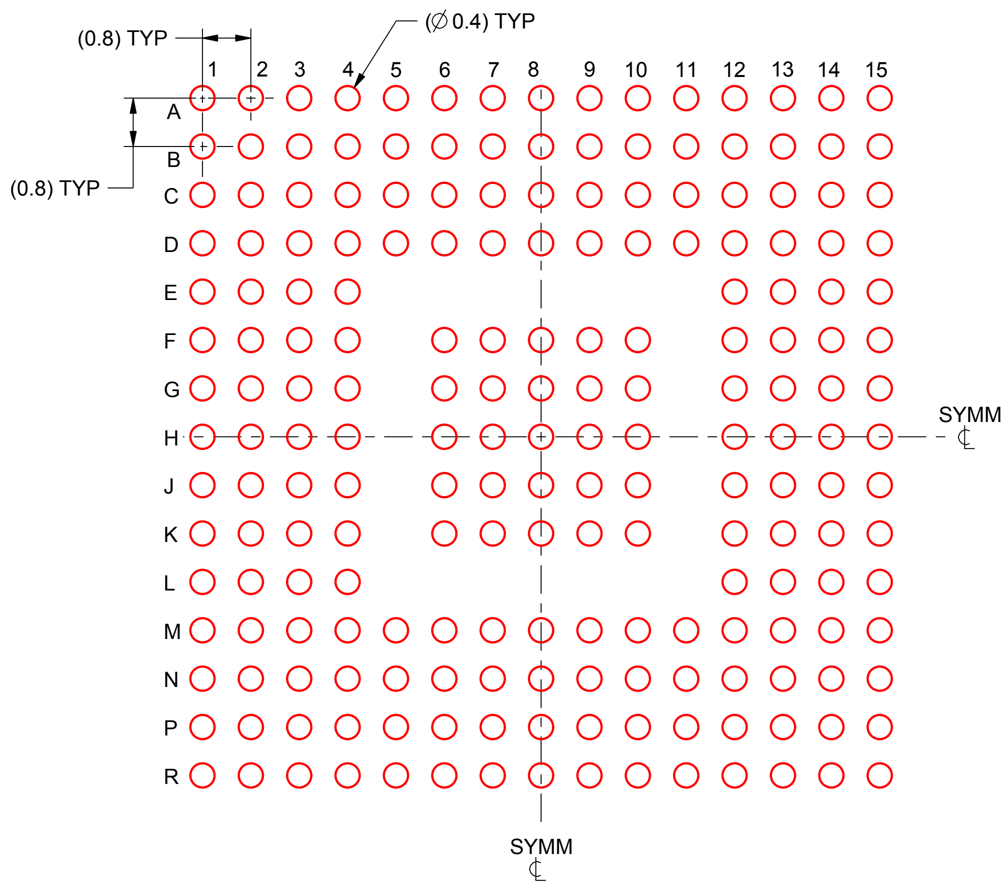


SOLDER MASK DETAILS
NOT TO SCALE

4221521/A 03/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4221521/A 03/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265