EVALUATION KIT AVAILABLE

MAX14595

Low-Power Dual-Channel Logic-Level Translator

General Description

The MAX14595 is a dual-channel, bidirectional logic-level translator designed specifically for low power consumption making it suitable for portable and battery-powered equipment. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. A logic signal present on the V_L side of the device appears as the same logic signal on the V_{CC} side of the device, and vice-versa.

The device is optimized for the I²C bus as well as the management data input/output (MDIO) bus where often high-speed, open-drain operation is required. When $\overline{TS}$ is high, the device allows the pullup to be connected to the I/O port that has the power. This allows continuous I²C operation on the powered side without any disruption while the level translation function is off.

The part is specified over the extended -40°C to +85°C temperature range, and is available in 8-bump WLP and 8-pin TDFN packages.

Applications

Portable and Battery-Powered Electronics

Devices with I²C Communication

Devices with MDIO Communication

General Logic-Level Translation

Benefits and Features

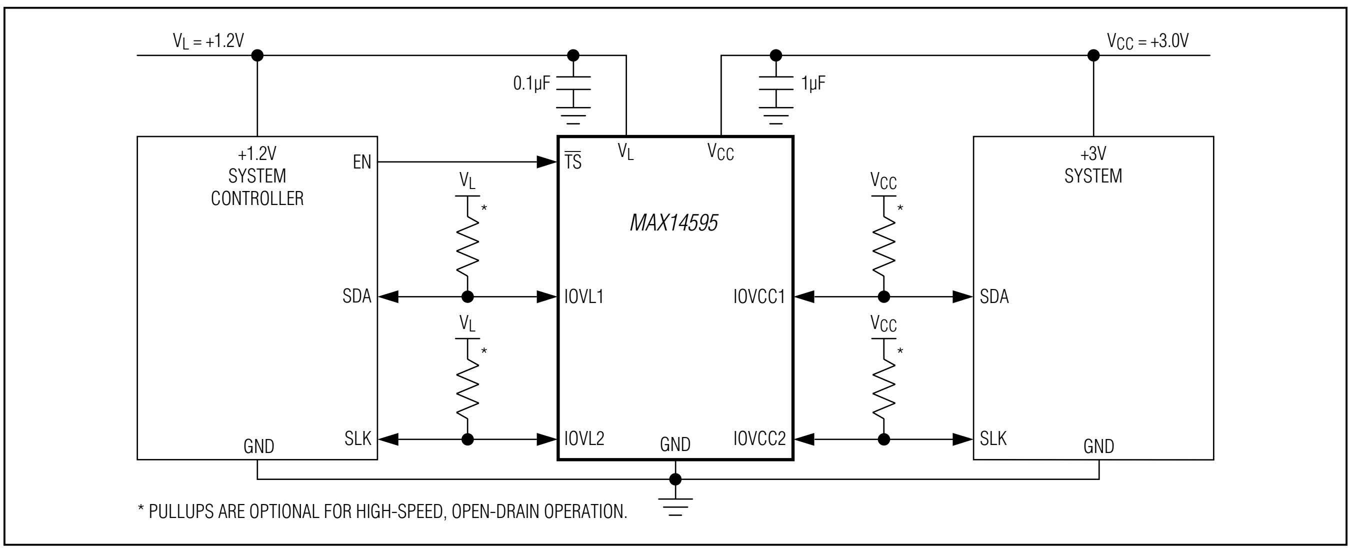
- Meets Industry Standards
  - I²C Requirements for Standard, Fast, and High* Speeds
  - MDIO Open Drain Above 4MHz*
- Allows Greater Design Flexibility
  - Down to 0.9V Operation on V_L Side
  - Supports Above 8MHz Push-Pull Operation
- Ultra-Low Power Consumption
  - 7µA V_{CC} Supply Current
  - 3µA V_L Supply Current
- Provides High Level of Integration
  - Pullup Resistor Enabled with One Side Power Supply when $\overline{TS}$ Is High
  - 12kΩ (max) Internal Pullup
  - Low Transmission Gate R_{ON}: 17Ω (max)
- Saves Space
  - 8-Bump, 0.4mm Pitch, 0.8mm x 1.6mm WLP Package
  - 8-Pin, 2mm x 2mm TDFN Package

*Requires external pullups.

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX14595.related.

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to GND.
V_{CC}, V_L, $\overline{TS}$ ....-0.5V to +6V
IOVCC1, IOVCC2 .... -0.5V to +(V_{CC} + 0.5V)
IOVL1, IOVL2 .... -0.5V to +(V_L + 0.5V)
Short-Circuit Duration IOVCC1, IOVCC2,
IOVL1, IOVL2 to GND ....Continuous
V_{CC}, IOVCC_ Maximum Continuous Current at +110°C 100mA
V_L IOVL_ Maximum Continuous Current at +110°C 40mA
$\overline{TS}$ Maximum Continuous Current at +110°C....................70mA
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 6.2mW/°C above +70°C)....................496mW
WLP (derate 11.8mW/°C above +70°C)....................944mW
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range.................... -65°C to +150°C
Lead Temperature (TDFN only, soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....162°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....20°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....85°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +0.9V to min(V_{CC} + 0.3V, +3.6V), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3V, V_L = +1.2V, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power Supply Range	V_L		0.9		5.5	V
	V_{CC}		1.65		5.5	
V_{CC} Supply Current	I_{CC}	IOVCC_ = V_{CC}, IOVL_ = V_L, $\overline{TS}$ = V_{CC}		7	15	µA
V_L Supply Current	I_L	IOVCC_ = V_{CC}, IOVL_ = V_L, $\overline{TS}$ = V_{CC}		3	6	µA
V_{CC} Shutdown Supply Current	$I_{CC-SHDN}$	$\overline{TS}$ = GND		0.4	1	µA
		$\overline{TS}$ = V_{CC}, V_L = GND, IOVCC_ = unconnected		0.4	1	
V_L Shutdown Supply Current	I_{L-SHDN}	$\overline{TS}$ = GND		0.1	1	µA
		$\overline{TS}$ = V_L, V_{CC} = GND, IOVL_ = unconnected		0.1	1	
IOVCC_, IOVL_ Three-State Leakage Current	I_{LEAK}	T_A = +25°C, $\overline{TS}$ = GND		0.1	1	µA
$\overline{TS}$ Input Leakage Current	I_{LEAK_TS}	T_A = +25°C			1	µA
V_{CC} Shutdown Threshold	V_{TH_VCC}	$\overline{TS}$ = V_L, V_{CC} falling		0.8	1.35	V
V_L Shutdown Threshold	V_{TH_VL}	$\overline{TS}$ = V_{CC}, V_L falling, V_{L} = 0.9V	0.25	0.6	0.86	V
V_L Above V_{CC} Shutdown Threshold	V_{TH_VL-VCC}	V_L rising above V_{CC}, V_{CC} = +1.65V	0.4	0.73	1.1	V
IOVL_ Pullup Resistor	R_{VL_PU}	Inferred from V_{OHL} measurements	3	7.6	12	kΩ
IOVCC_ Pullup Resistor	R_{VCC_PU}	Inferred from V_{OHC} measurements	3	7.6	12	kΩ
IOVL_ to IOVCC_ DC Resistance	$R_{IOVL-IOVCC}$	Inferred from V_{OLx} measurements		6	17	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +0.9V to min(V_{CC} + 0.3V, +3.6V), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3V, V_L = +1.2V, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVELS						
IOVL_ Input-Voltage High	V_{IHL}	IOVL_ rising, V_L = +0.9V, V_{CC} = +1.65V (Note 4)	V_L - 0.2			V
IOVL_ Input-Voltage Low	V_{ILL}	IOVL_ falling, V_L = +0.9V, V_{CC} = +1.65V (Note 4)			0.15	V
IOVCC_ Input-Voltage High	V_{IHC}	IOVCC_ rising, V_L = +0.9V, V_{CC} = +1.65V (Note 4)	V_{CC} - 0.4			V
IOVCC_ Input-Voltage Low	V_{ILC}	IOVCC_ falling, V_L = +0.9V, V_{CC} = +1.65V (Note 4)			0.2	V
$\overline{TS}$ Input-Voltage High	V_{IH}	$\overline{TS}$ rising, V_L = +0.9V or +3.6V, V_{CC} > V_L	V_L - 0.15			V
$\overline{TS}$ Input-Voltage Low	V_{IL}	$\overline{TS}$ falling, V_L = +0.9V or +3.6V, V_{CC} > V_L			0.2	V
IOVL_ Output-Voltage High	V_{OHL}	IOVL_ source current 20µA, $V_{IOVCC\_}$ = V_L to V_{CC} ($V_{CC} \geq V_L$)	0.7 x V_L			V
IOVL_ Output-Voltage Low	V_{OLL}	IOVL_ sink current 5mA, $V_{IOVCC\_} \leq$ 0.05V			0.2	V
IOVCC_ Output-Voltage High	V_{OHC}	IOVCC_ source current 20µA, $V_{IOVL\_}$ = V_L	0.7 x V_{CC}			V
IOVCC_ Output-Voltage Low	V_{OLC}	IOVCC_ sink current 5mA, $V_{IOVL\_} \leq$ 0.05V			0.25	V
RISE/FALL TIME ACCELERATOR STAGE						
Accelerator Pulse Duration		V_L = +0.9V, V_{CC} = +1.65V	9	22	48	ns
IOVL_ Output Accelerator Source Impedance		V_L = +0.9V, IOVL_ = GND, V_{CC} = +1.65V		26		Ω
		V_L = +3.3V, IOVL_ = GND, V_{CC} = +5V		6.8		
IOVCC_ Output Accelerator Source Impedance		V_{CC} = +1.65V, IOVCC_ = GND		26		Ω
		V_{CC} = +5V, IOVCC_ = GND		6.5		
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			+150		°C
Thermal Hysteresis	T_{HYST}			10		°C

TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +0.9V to +3.6V, $V_{CC} \geq V_L$, $\overline{TS}$ = V_L, C_{VCC} = 1µF, C_{VL} = 0.1µF, $C_{IOVL\_} \leq$ 100pF, $C_{IOVCC\_} \leq$ 100pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3V, V_L = +1.2V and T_A = +25°C. All timing is 10% to 90% for rise time and 90% to 10% for fall time.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-On Time for Q1	t_{ON}	$V_{\overline{TS}}$ = 0V to V_L (see the *Block Diagram*)			160	400	µs
IOVCC_ Rise Time	t_{RCC}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 1)			8	22	ns
		Open-drain driving, V_L = +1.2V, V_{CC} = +3V (Figure 2)			11		
IOVCC_ Fall Time	t_{FCC}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 1)			5	15	ns
		Open-drain driving, V_L = +1.2V, V_{CC} = +3V (Figure 2)			6		
IOVL_ Rise Time	t_{RL}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 3)			4	13	ns
		Open-drain driving, V_L = +1.2V, V_{CC} = +3V (Figure 4)			16		
IOVL_ Fall Time	t_{FL}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 3)			2.8	12	ns
		Open-drain driving, V_L = +1.2V, V_{CC} = +3V (Figure 4)			3.3		
Propagation Delay (Driving IOVL_)	t_{PD_LCC}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 1)	Rising		7.6	19	ns
			Falling		3	9	
Propagation Delay (Driving IOVCC_)	t_{PD_CCL}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 3)	Rising		3	5	ns
			Falling		1.5	7	
Channel-to-Channel Skew	t_{SKEW}	Input rise time/fall time < 6ns				1.5	ns
Maximum Data Rate		Push-pull operation		8			MHz
		Open-drain operation (Note 6)		4			

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.
Note 3: V_L must be less than or equal to V_{CC} during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions.
Note 4: V_{IHL}, V_{ILL}, V_{IHC}, and V_{ILC} are intended to define the range where the accelerator triggers.
Note 5: Guaranteed by design.
Note 6: External pullup resistors are required.

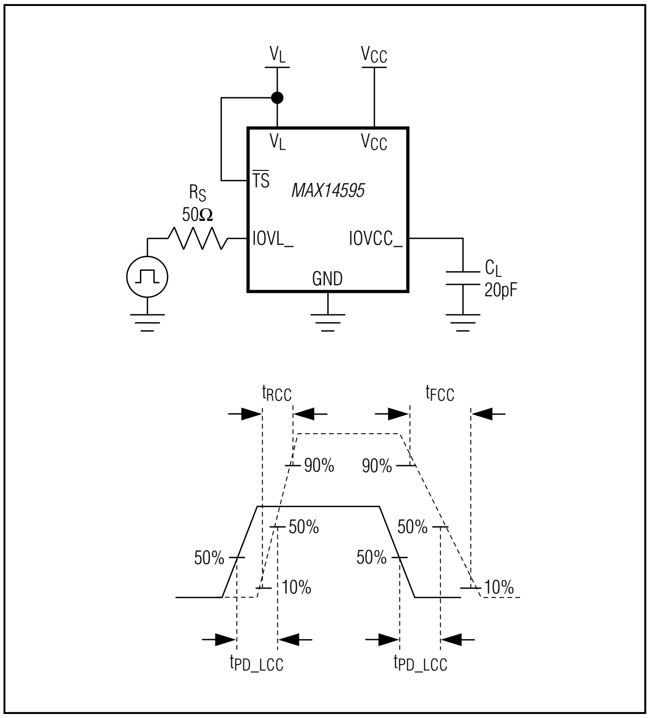


*Figure 1. Push-Pull Driving IOVL_*

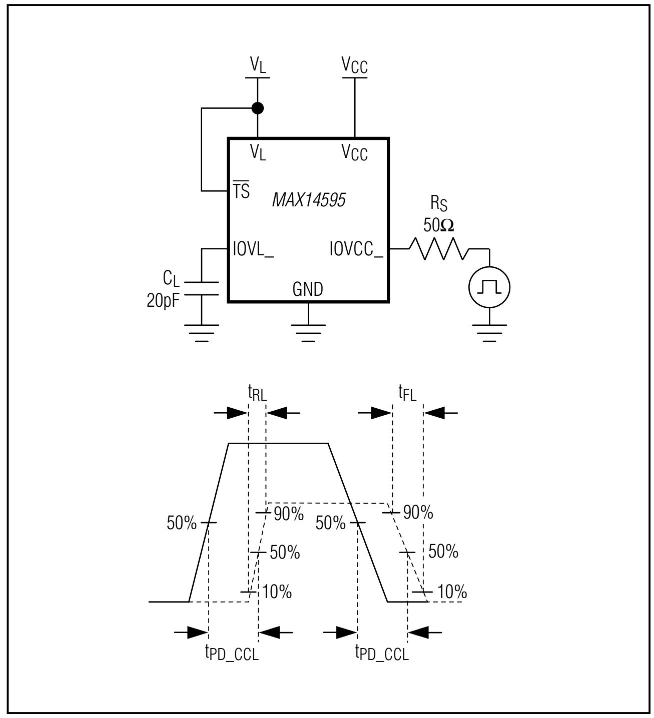


*Figure 3. Push-Pull Driving IOVCC_*

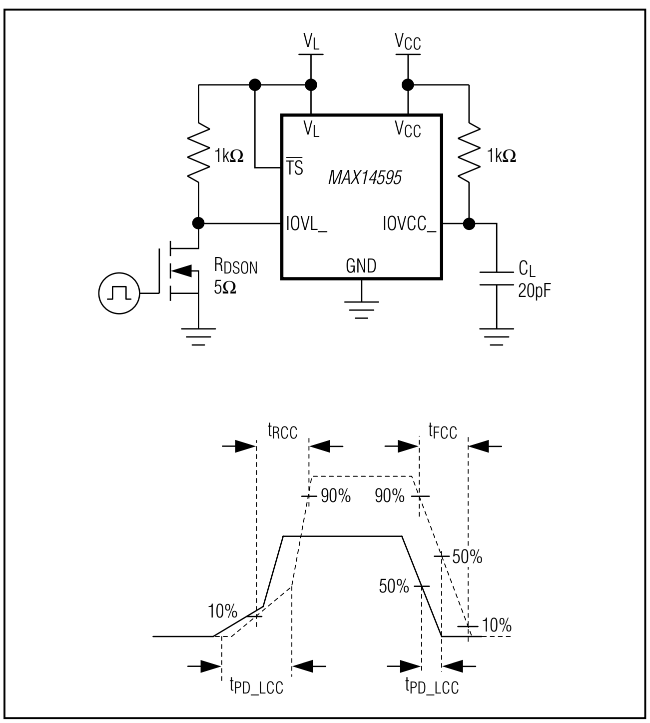


*Figure 2. Open-Drain Driving IOVL_*

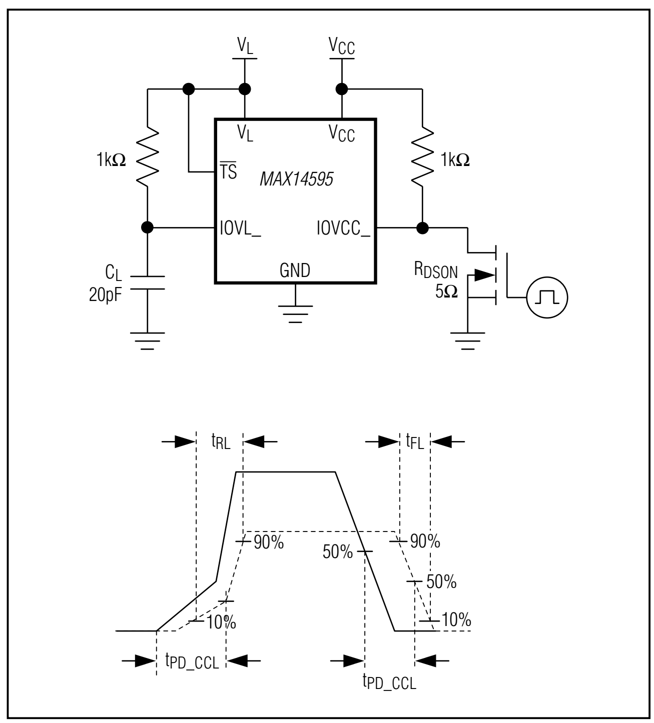
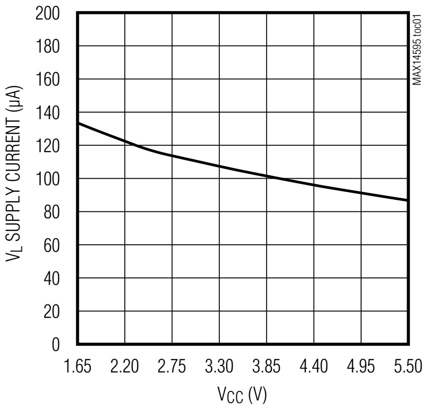


*Figure 4. Open-Drain Driving IOVCC_*

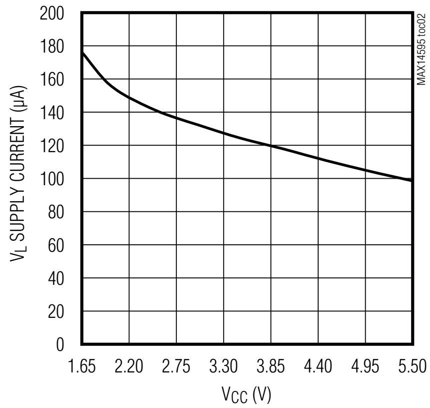
Typical Operating Characteristics

(V_{CC} = +3V, V_L = +1.5V, R_L = 1MΩ, C_L = 15pF, push-pull driving data rate = 8Mbps, T_A = +25°C, unless otherwise noted.)

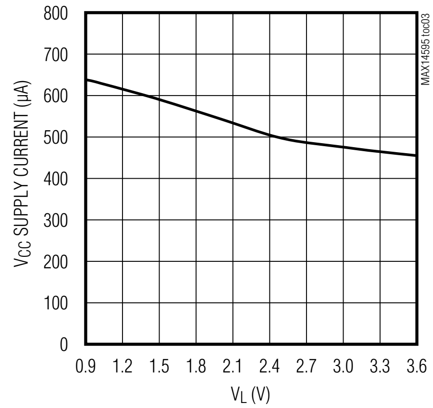
V_L DYNAMIC SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (OPEN-DRAIN DRIVING ONE IOVL_)



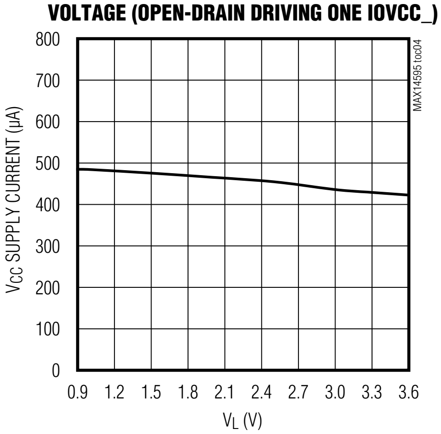
V_L DYNAMIC SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (PUSH-PULL DRIVING ONE IOVCC_)



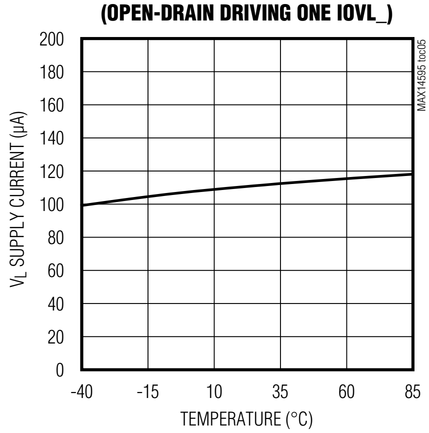
V_{CC} DYNAMIC SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (PUSH-PULL DRIVING ONE IOVL_)



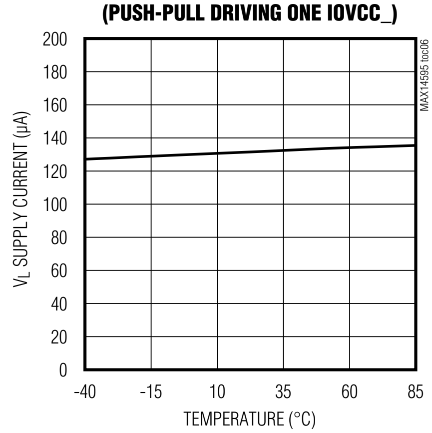
V_{CC} DYNAMIC SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (OPEN-DRAIN DRIVING ONE IOVCC_)



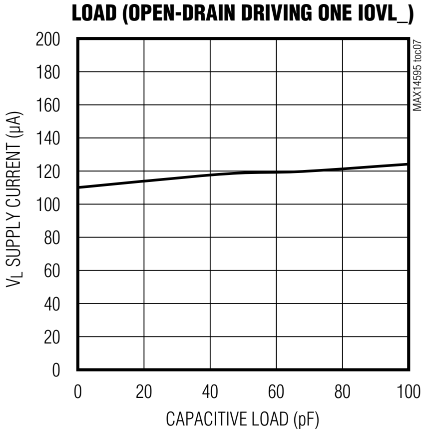
V_L DYNAMIC SUPPLY CURRENT vs. TEMPERATURE (OPEN-DRAIN DRIVING ONE IOVL_)



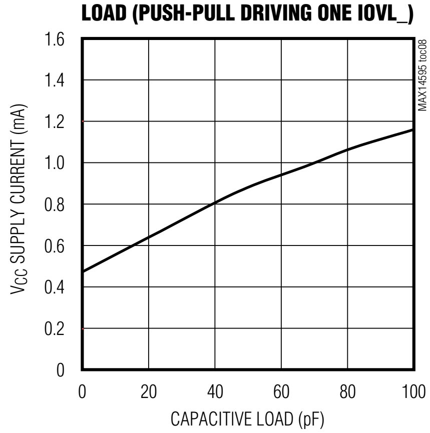
V_L DYNAMIC SUPPLY CURRENT vs. TEMPERATURE (PUSH-PULL DRIVING ONE IOVCC_)



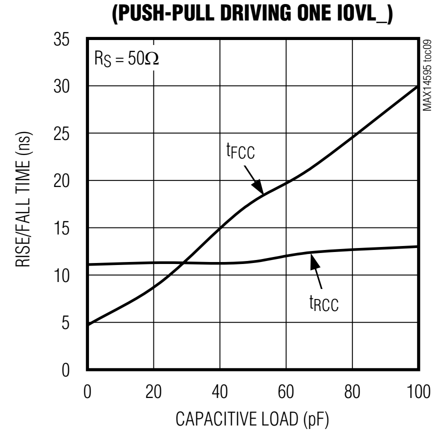
V_L DYNAMIC SUPPLY CURRENT vs. CAPACITIVE LOAD (OPEN-DRAIN DRIVING ONE IOVL_)



V_{CC} DYNAMIC SUPPLY CURRENT vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVL_)



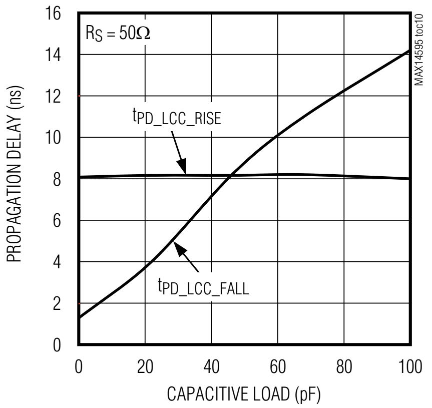
RISE/FALL TIME vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVL_)



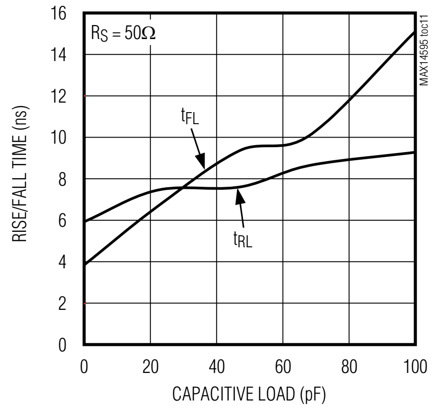
Typical Operating Characteristics (continued)

(V_{CC} = +3V, V_L = +1.5V, R_L = 1MΩ, C_L = 15pF, push-pull driving data rate = 8Mbps, T_A = +25°C, unless otherwise noted.)

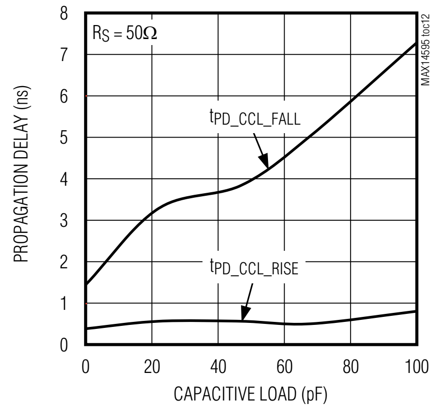
PROPAGATION DELAY vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVL_)



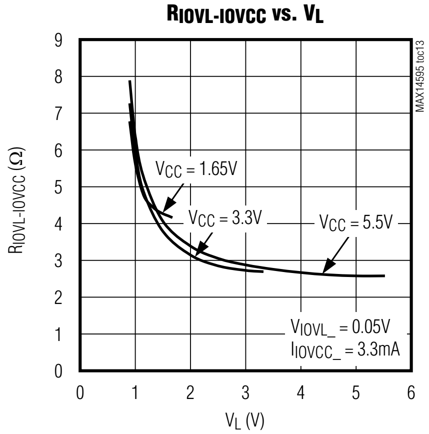
RISE/FALL TIME vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVCC_)



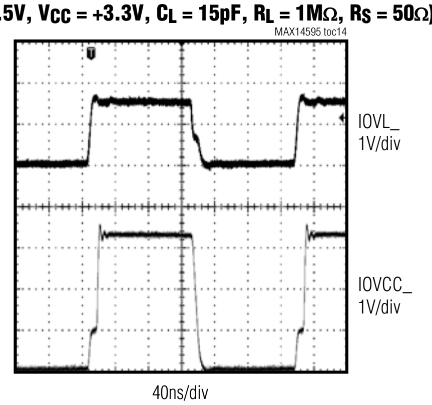
PROPAGATION DELAY vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVCC_)



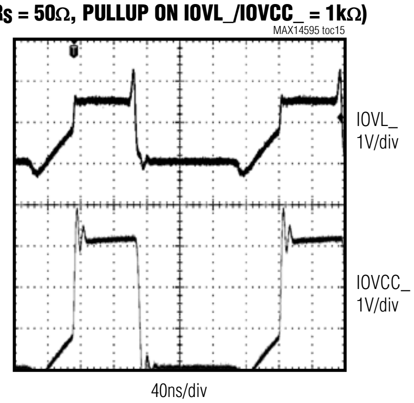
$R_{IOVL-IOVCC}$ vs. V_L



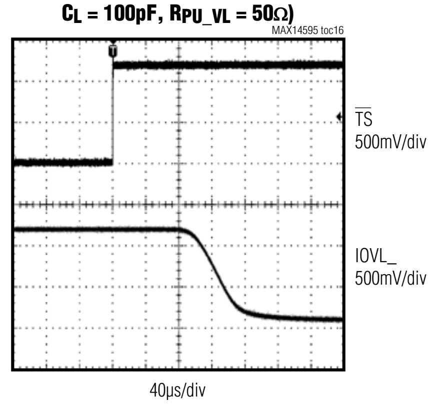
RAIL-TO-RAIL DRIVING (PUSH-PULL DRIVING ONE IOVL_) (V_L = +1.5V, V_{CC} = +3.3V, C_L = 15pF, R_L = 1MΩ, R_S = 50Ω)



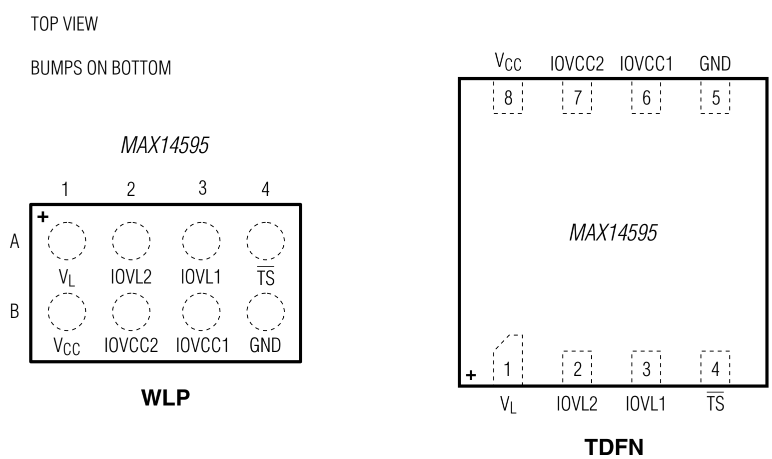
RAIL-TO-RAIL DRIVING (OPEN-DRAIN DRIVING ONE IOVL_) (V_L = +1.5V, V_{CC} = +3.3V, C_L = 100pF, R_L = 50Ω, R_S = 50Ω, PULLUP ON IOVL_/IOVCC_ = 1kΩ)



EXITING SHUTDOWN MODE (V_L = 1.2V, V_{CC} = 3.0V, IOVCC_ = 0V, C_L = 100pF, R_{PU_VL} = 50Ω)



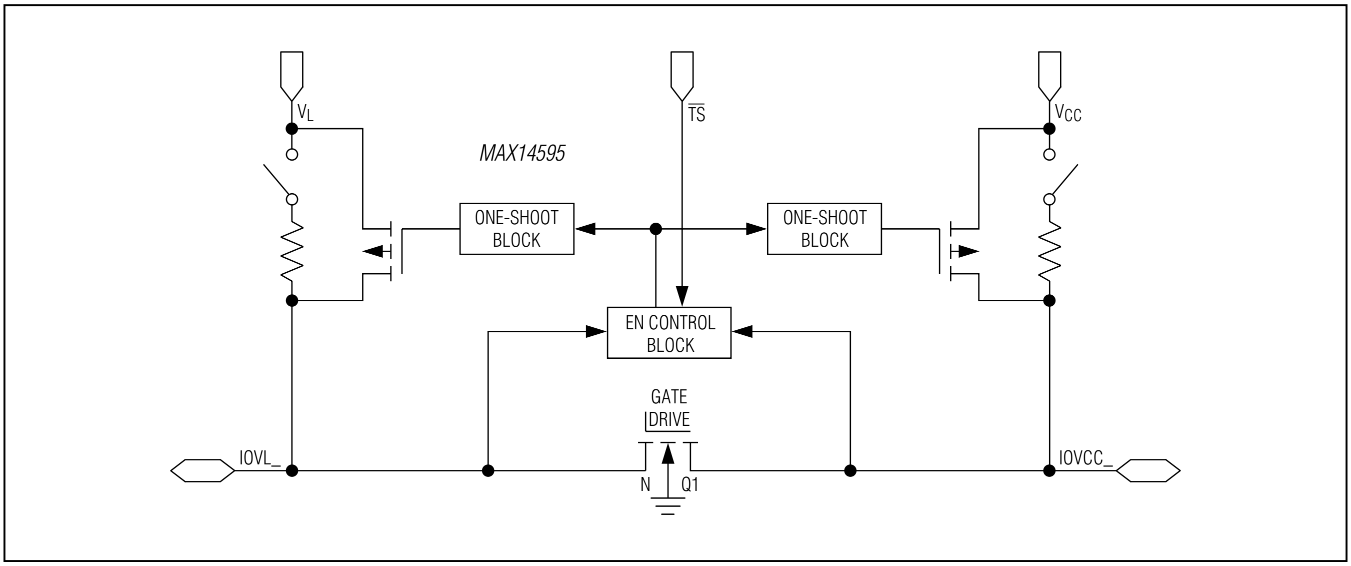
Pin Configurations



Pin Description

BUMP/PIN		NAME	FUNCTION
WLP	TDFN		
A1	1	V_L	Logic Supply Voltage, +0.9V to min(V_{CC} + 0.3V, +3.6V). Bypass V_L to GND with a 0.1µF ceramic capacitor as close as possible to the device.
A2	2	IOVL2	Input/Output 2. Reference to V_L.
A3	3	IOVL1	Input/Output 1. Reference to V_L.
A4	4	$\overline{TS}$	Active Low Three-State Input. Drive $\overline{TS}$ low to place the device in shutdown mode with high-impedance output and internal pullup resistors disconnected. Drive $\overline{TS}$ high for normal operation.
B1	8	V_{CC}	Power-Supply Voltage, +1.65V to +5.5V. Bypass V_{CC} to GND with a 1µF ceramic capacitor as close as possible to the device.
B2	7	IOVCC2	Input/Output 2. Reference to V_{CC}.
B3	6	IOVCC1	Input/Output 1. Reference to V_{CC}.
B4	5	GND	Ground

Block Diagram



Detailed Description

The MAX14595 is a dual-channel, bidirectional level translator. The device translates low voltage down to +0.9V on the V_L side to high voltage on the V_{CC} side and vice-versa. The device is optimized for open-drain and high-speed operation, such as I^2C bus and MDIO bus.

The device has low on-resistance (17Ω max), which is important for high-speed, open-drain operation. The device also features internal pullup resistors that are active when the corresponding power is on and $\overline{TS}$ is high.

Level Translation

For proper operation, ensure that $+1.65V \leq V_{CC} \leq +5.5V$, and $+0.9V \leq V_L \leq V_{CC}$. When power is supplied to V_L while V_{CC} is less than V_L, the device automatically disables logic-level translation function. Also, the device enters shutdown mode when $\overline{TS}$ = GND.

High-Speed Operation

The device meets the requirements of high-speed I^2C and MDIO open-drain operation. The maximum data rate is at least 4MHz for open-drain operation with the total bus capacitance equal to or less than 100pF.

Three-State Input $\overline{TS}$

The device features a three-state input that can put the device into high-impedance mode. When $\overline{TS}$ is low, IOVCC_ and IOVL_ are all high impedance and the internal pullup resistors are disconnected. When $\overline{TS}$ is high, the internal pullup resistors are connected when the corresponding power is in regulation, and the resistors are disconnected at the side that has no power on. In many portable applications, one supply is turned off but the other side is still operating and requires the pullup resistors to be present. This feature eliminates the need for external pullup resistors. The level translation function is off until both power supplies are in range.

Thermal-Shutdown Protection

The device features thermal-shutdown protection to protect the part from overheating. The device enters thermal shutdown when the junction temperature exceeds +150°C (typ), and the device is back to normal operation again after the temperature drops by approximately 10°C (typ). When the device is in thermal shutdown, the level translator is disabled.

Low-Power Dual-Channel Logic-Level Translator

Ordering Information

PART	TOP MARK	PIN-PACKAGE
MAX14595ETA+T	BNT	8 TDFN
MAX14595EWA+T	AAE	8 WLP

Note: *All devices are specified over -40°C to +85°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN	T822CN+1	**21-0487**	**90-0349**
8 WLP	W80A1+1	**21-0555**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—