

# MJF44H11 (NPN), MJF45H11 (PNP)

Preferred Devices

## Complementary Power Transistors

### For Isolated Package Applications

Complementary power transistors are for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

#### Features

- Low Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 1.0 \text{ V (Max) @ } 8.0 \text{ A}$
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs
- Pb–Free Packages are Available\*

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
Collector Current – Continuous – Peak	$I_C$	10 20	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	36 0.288	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–55 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	3.5	$^\circ\text{C/W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

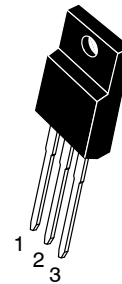
\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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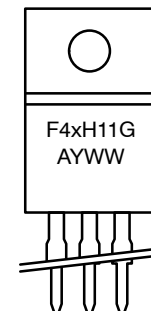
<http://onsemi.com>

## SILICON POWER TRANSISTORS 10 AMPERES 80 VOLTS, 36 WATTS



ISOLATED TO–220  
CASE 221D  
STYLE 2

#### MARKING DIAGRAM



F4xH11 = Specific Device Code  
x = 4 or 5  
G = Pb–Free Package  
A = Assembly Location  
Y = Year  
WW = Work Week

#### ORDERING INFORMATION

Device	Package	Shipping
MJF44H11	TO–220 FULLPACK	50 Units/Rail
MJF44H11G	TO–220 FULLPACK (Pb–Free)	50 Units/Rail
MJF45H11	TO–220 FULLPACK	50 Units/Rail
MJF45H11G	TO–220 FULLPACK (Pb–Free)	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

# MJF44H11 (NPN), MJF45H11 (PNP)

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Emitter Sustaining Voltage (I <sub>C</sub> = 30 mA, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	80	-	-	Vdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , V <sub>BE</sub> = 0)	I <sub>CES</sub>	-	-	1.0	μA
Emitter Cutoff Current (V <sub>EB</sub> = 5 Vdc)	I <sub>EBO</sub>	-	-	10	μA

## ON CHARACTERISTICS

Collector-Emitter Saturation Voltage (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 0.4 Adc)	V <sub>CE(sat)</sub>	-	-	1.0	Vdc
Base-Emitter Saturation Voltage (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 0.8 Adc)	V <sub>BE(sat)</sub>	-	-	1.5	Vdc
DC Current Gain (V <sub>CE</sub> = 1 Vdc, I <sub>C</sub> = 2 Adc)	h <sub>FE</sub>	60	-	-	-
DC Current Gain (V <sub>CE</sub> = 1 Vdc, I <sub>C</sub> = 4 Adc)		40	-	-	-

## DYNAMIC CHARACTERISTICS

Collector Capacitance (V <sub>CB</sub> = 10 Vdc, f <sub>test</sub> = 1 MHz)	MJF44H11 MJF45H11	C <sub>cb</sub>	-	130 230	-	μF
Gain Bandwidth Product (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 20 MHz)	MJF44H11 MJF45H11	f <sub>T</sub>	-	50 40	-	MHz

## SWITCHING TIMES

Delay and Rise Times (I <sub>C</sub> = 5 Adc, I <sub>B1</sub> = 0.5 Adc)	MJF44H11 MJF45H11	t <sub>d</sub> + t <sub>r</sub>	-	300 135	-	ns
Storage Time (I <sub>C</sub> = 5 Adc, I <sub>B1</sub> = I <sub>B2</sub> = 0.5 Adc)	MJF44H11 MJF45H11	t <sub>s</sub>	-	500 500	-	ns
Fall Time (I <sub>C</sub> = 5 Adc, I <sub>B1</sub> = I <sub>B2</sub> = 0.5 Adc)	MJF44H11 MJF45H11	t <sub>f</sub>	-	140 100	-	ns

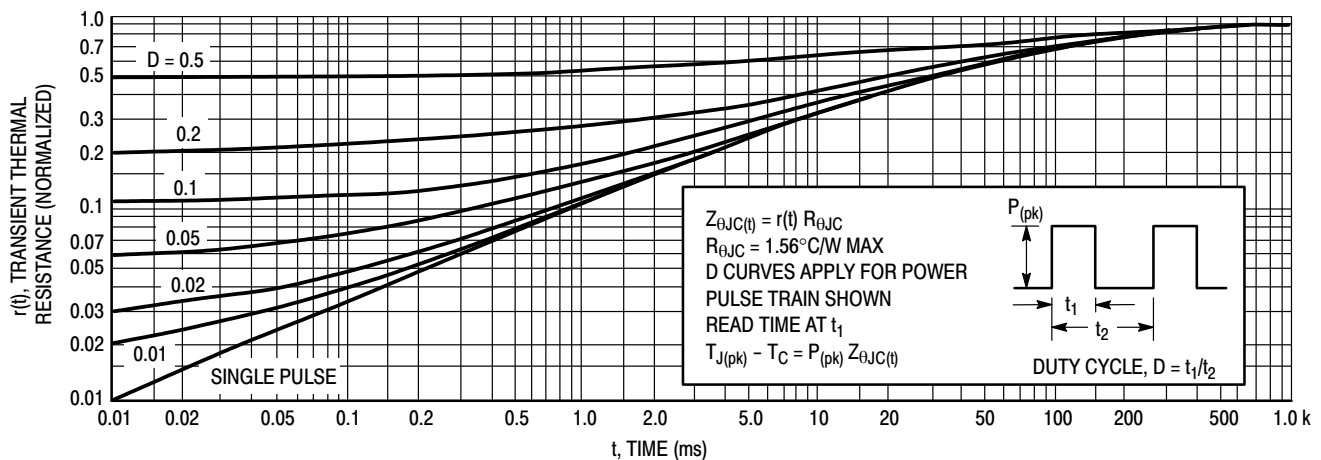
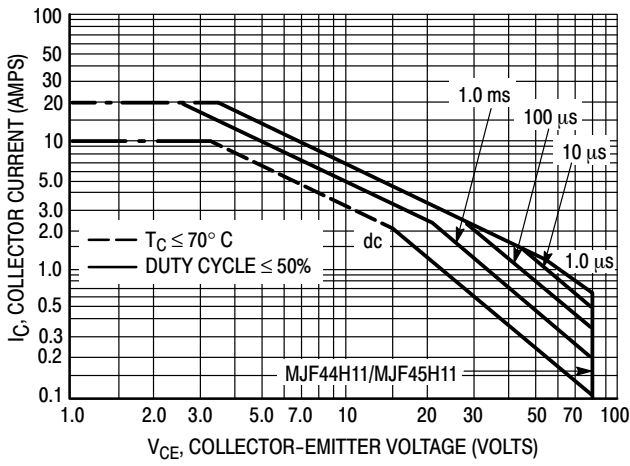


Figure 1. Thermal Response

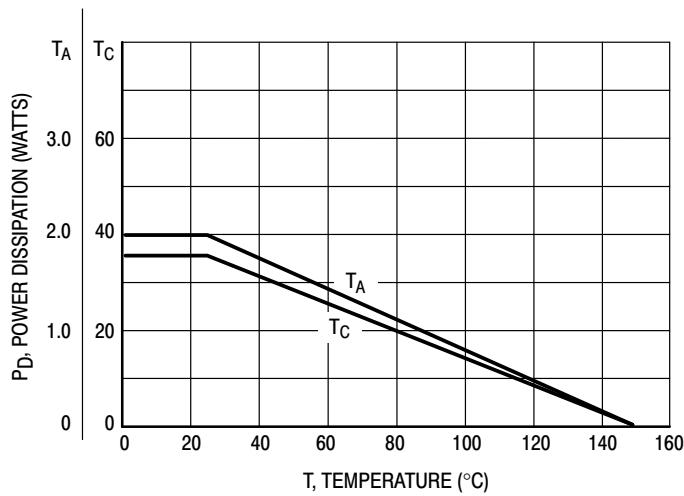
## MJF44H11 (NPN), MJF45H11 (PNP)



**Figure 2. Maximum Rated Forward Bias Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 3. Power Derating**

# MJF44H11 (NPN), MJF45H11 (PNP)

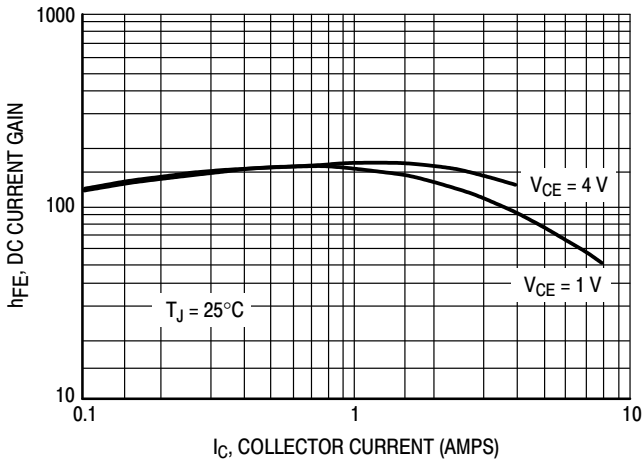


Figure 4. MJF44H11 DC Current Gain

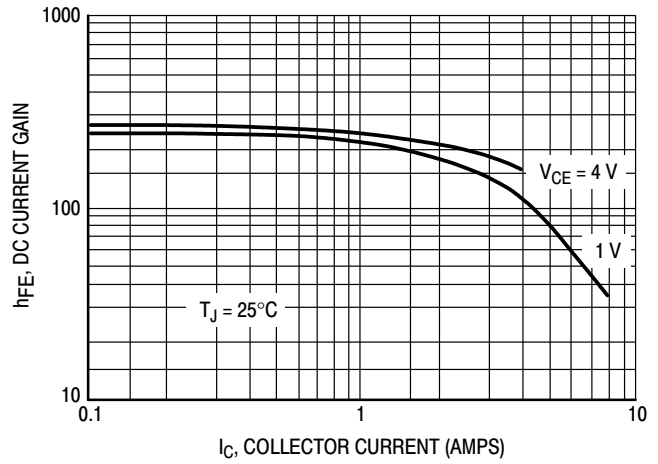


Figure 5. MJF45H11 DC Current Gain

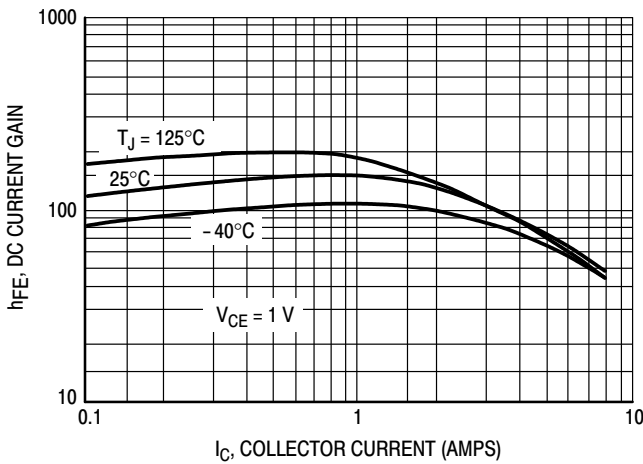


Figure 6. MJF44H11 Current Gain versus Temperature

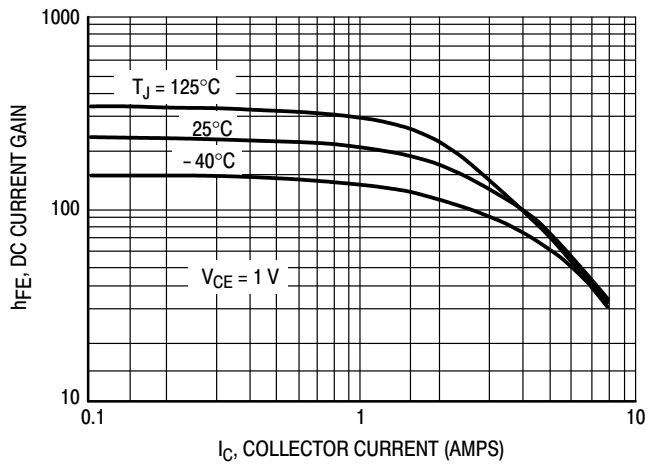


Figure 7. MJF45H11 Current Gain versus Temperature

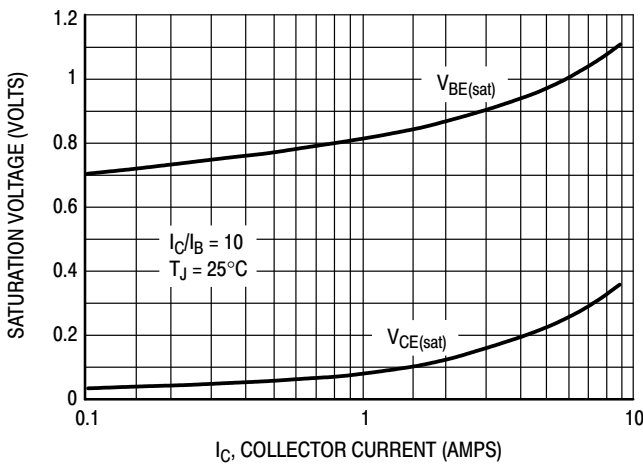


Figure 8. MJF44H11 On-Voltages

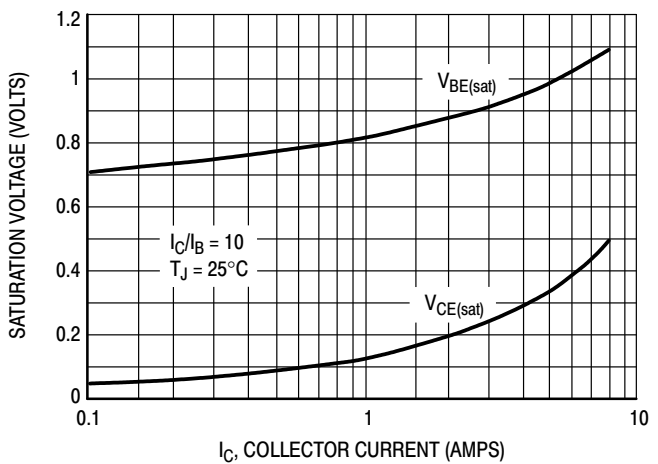
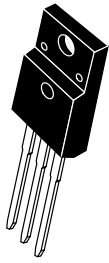


Figure 9. MJF45H11 On-Voltages

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

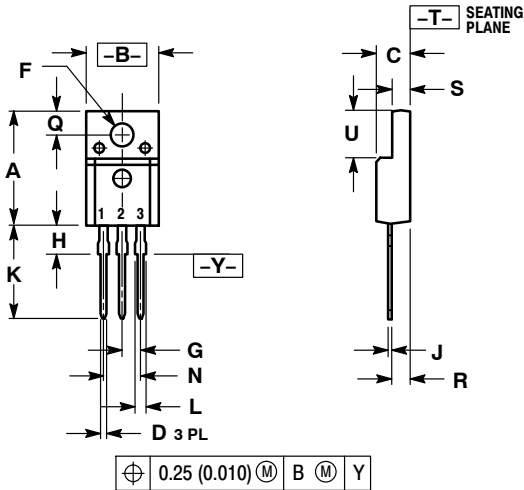
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SCALE 1:1

## TO-220 FULLPAK CASE 221D-03 ISSUE K

DATE 27 FEB 2009



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH
  - 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

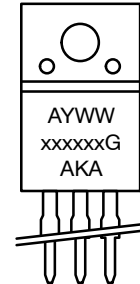
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

### MARKING DIAGRAMS

- |  |   |  |
|--|---|--|
| STYLE 1:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE     | STYLE 2:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER | STYLE 3:<br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE |
| STYLE 4:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE | STYLE 5:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE     | STYLE 6:<br>PIN 1. MT 1<br>2. MT 2<br>3. GATE      |



**Bipolar**



**Rectifier**

- |                               |                           |
|-------------------------------|---------------------------|
| xxxxxx = Specific Device Code | A = Assembly Location     |
| G = Pb-Free Package           | Y = Year                  |
| A = Assembly Location         | WW = Work Week            |
| Y = Year                      | xxxxxx = Device Code      |
| WW = Work Week                | G = Pb-Free Package       |
|                               | AKA = Polarity Designator |

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