

# FDM3300NZ

## Monolithic Common Drain N-Channel 2.5V Specified PowerTrench® MOSFET

### Features

- Max  $r_{DS(on)}$  = 23m $\Omega$  at  $V_{GS} = 4.5V$ ,  $I_D = 10A$
- Max  $r_{DS(on)}$  = 28m $\Omega$  at  $V_{GS} = 2.5V$ ,  $I_D = 9A$
- >2000V ESD protection
- Low Profile - 1mm maximum - in the new package MLP 3.3x3.3 mm
- RoHS Compliant

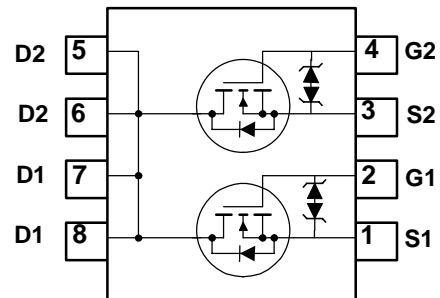
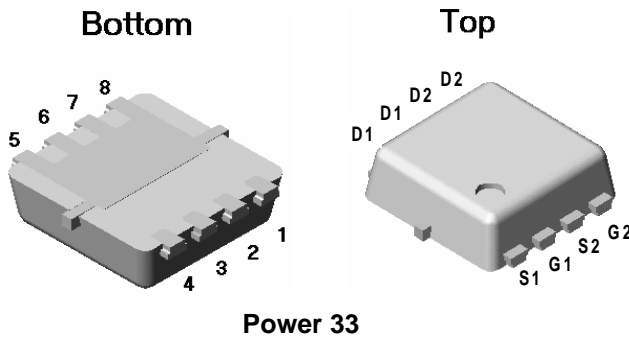


### General Description

This dual N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced PowerTrench® process to optimize the  $r_{DS(on)}$  @  $V_{GS} = 2.5V$  on special MLP lead frame with all the drains on one side of the package.

### Application

- Li-Ion Battery Pack



### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain to Source Voltage	20	V
$V_{GS}$	Gate to Source Voltage	$\pm 12$	V
$I_D$	Drain Current -Continuous	10	A
	-Pulsed	40	
$P_D$	Power Dissipation (Steady State)	(Note 1a)	W
		(Note 1b)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	135	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
3300N	FDM3300NZ	Power 33	7"	8mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		10.7		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	0.6	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\text{V}, I_D = 10\text{A}$		16	23	m $\Omega$
		$V_{GS} = 2.5\text{V}, I_D = 9\text{A}$		20	28	
		$V_{GS} = 4.5\text{V}, I_D = 10\text{A}, T_J = 125^\circ\text{C}$		22	31	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 10\text{A}$		35		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1210	1610	pF
$C_{oss}$	Output Capacitance			330	440	pF
$C_{rss}$	Reverse Transfer Capacitance			180	270	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$		2.3		$\Omega$

### Switching Characteristics

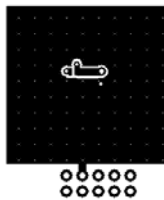
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{V}, I_D = 1.0\text{A}$ $V_{GS} = 4.5\text{V}, R_{GEN} = 6.0\Omega$		10	20	ns
$t_r$	Rise Time			14	25	ns
$t_{d(off)}$	Turn-Off Delay Time			26	42	ns
$t_f$	Fall Time			13	23	ns
$Q_g$	Total Gate Charge		$V_{GS} = 4.5\text{V}$		12	17
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 10\text{V}$ $I_D = 10\text{A}$		2		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			4		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 2.0\text{A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 10\text{A}, di/dt = 100\text{A}/\mu\text{s}$		20		ns
$Q_{rr}$	Reverse Recovery Charge			6		nC

#### Notes:

- 1:  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.  
 (a)  $R_{\theta JA} = 60^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5"x1.5"x0.062" thick PCB.  
 (b)  $R_{\theta JA} = 135^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.



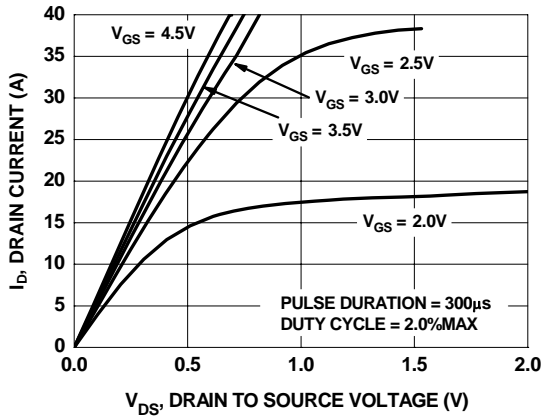
a.  $60^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



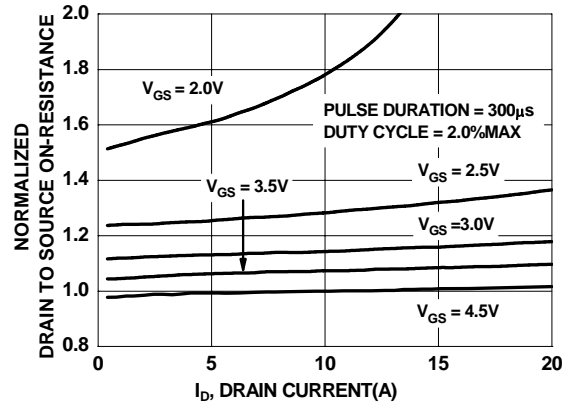
b.  $135^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty cycle < 2.0%.

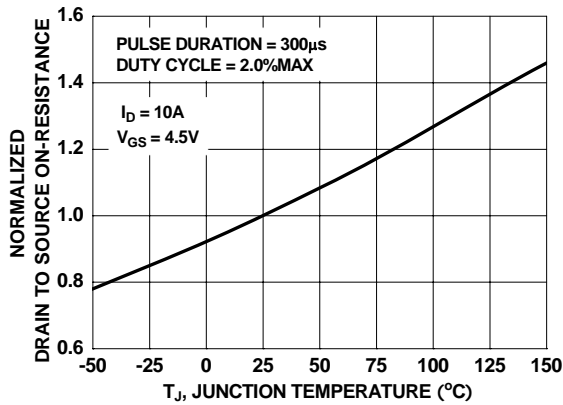
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



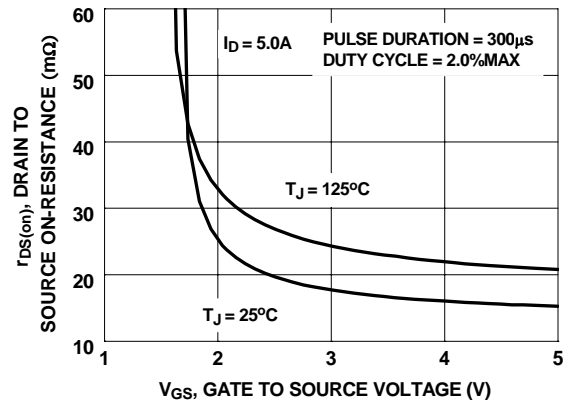
**Figure 1. On Region Characteristics**



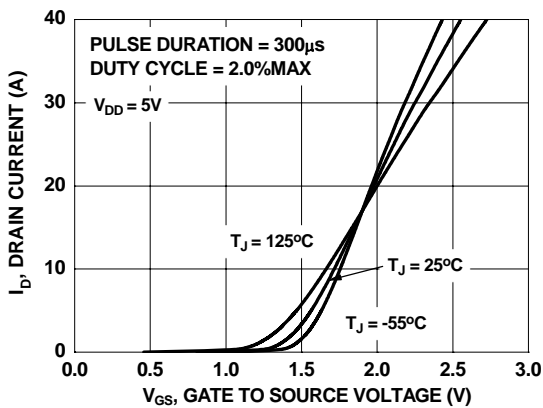
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



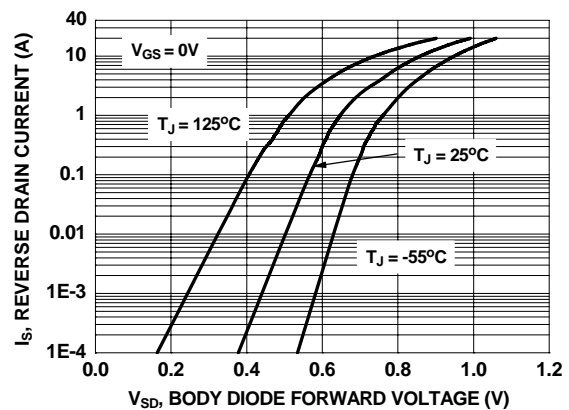
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**



**Figure 5. Transfer Characteristics**



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

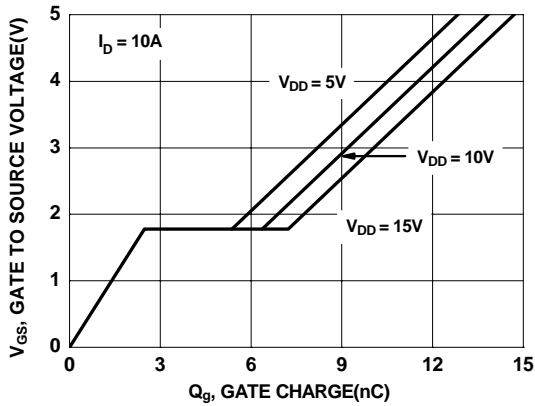


Figure 7. Gate Charge Characteristics

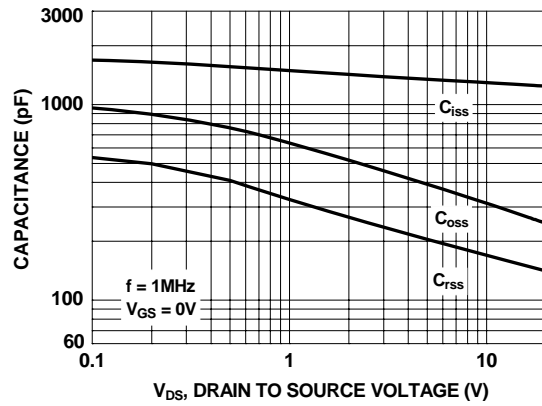


Figure 8. Capacitance vs Drain to Source Voltage

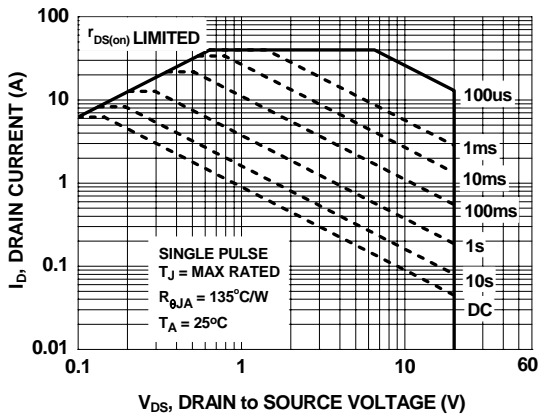


Figure 9. Forward Bias Safe Operating Area

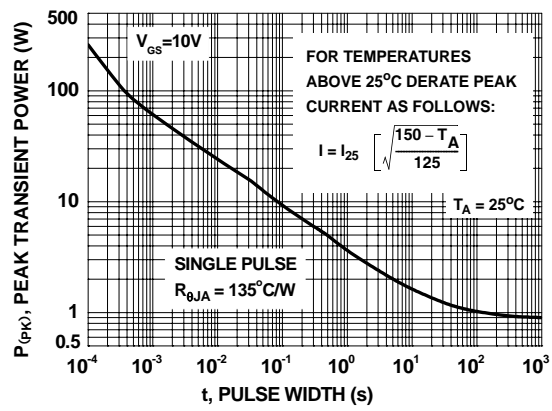


Figure 10. Single Pulse Maximum Power Dissipation

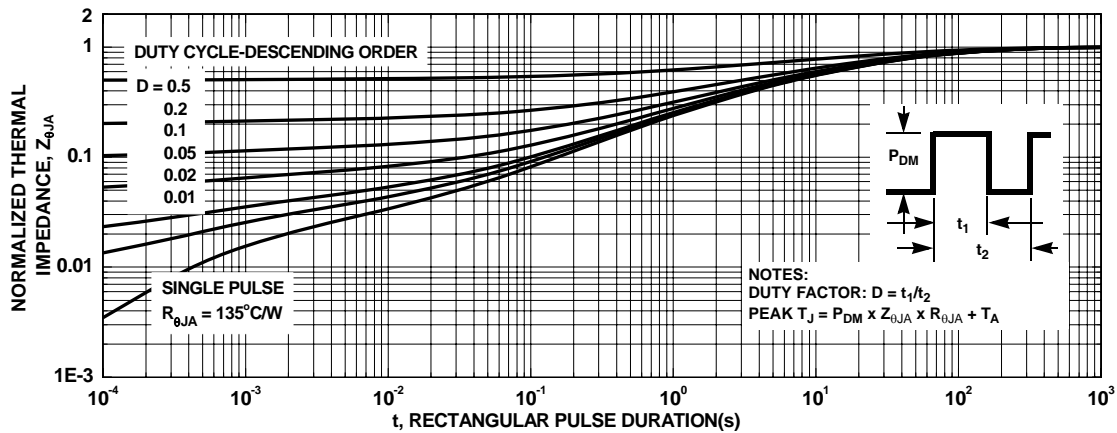
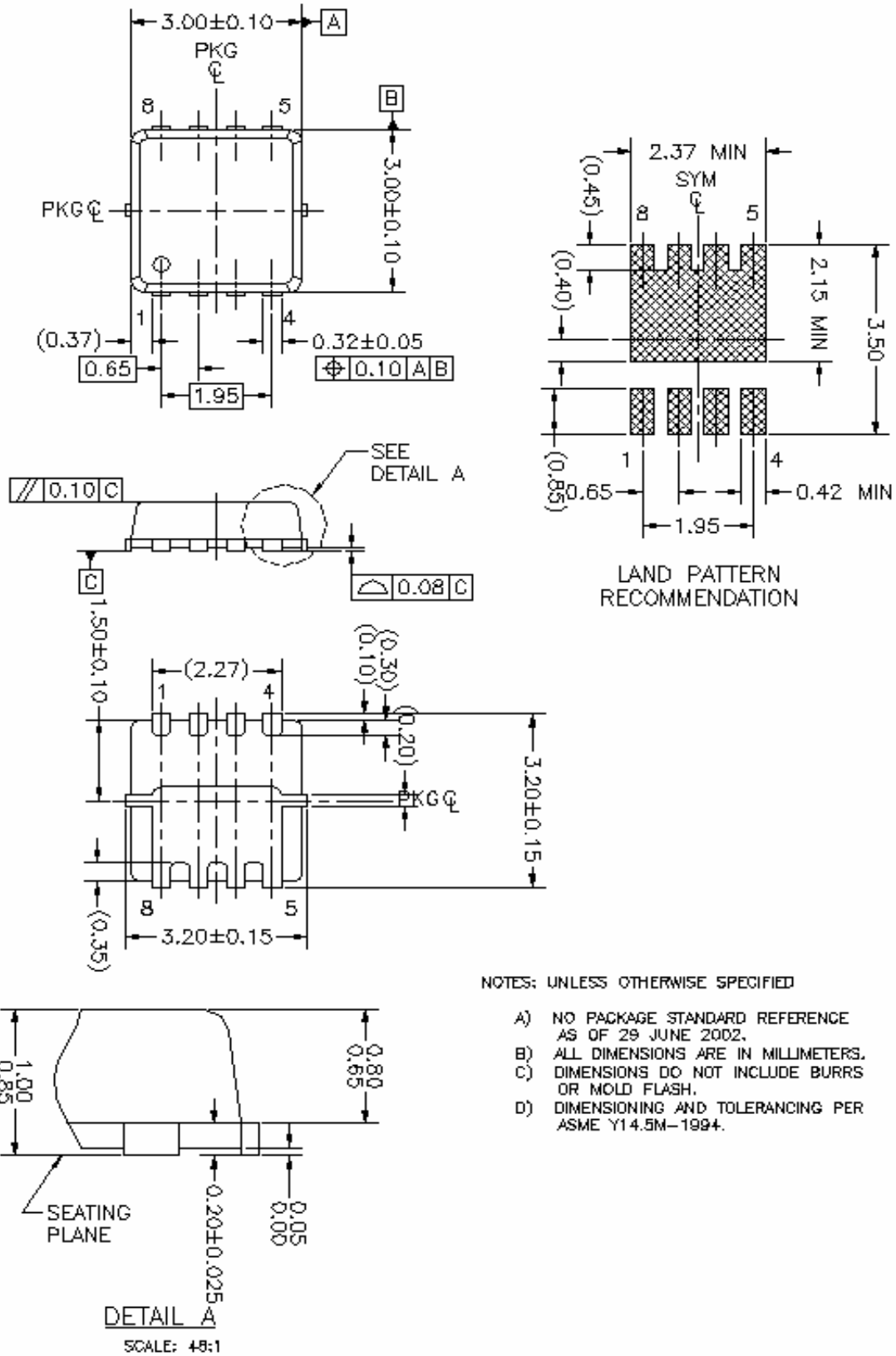


Figure 11. Transient Thermal Response Curve



NOTES: UNLESS OTHERWISE SPECIFIED

- A) NO PACKAGE STANDARD REFERENCE AS OF 29 JUNE 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

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Rev. 122