CHANGE NOTIFICATION

LINEAR TECHNOLOGY

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October 6, 2016

Dear Sir/Madam: PCN#100616

Subject: Notification of Change to LTC2440, LTC2442, LTC2444, LTC2445, LTC2446, LTC2447, LTC2448, LTC2449 Datasheets

Please be advised that Linear Technology Corporation has made a change to the datasheet specifications of subject devices in order to improve device manufacturability. The changes are mentioned below.

The Maximum External Oscillator Frequency (f_{EOSC}) in the Timing Characteristics is being reduced from 20MHz to 12MHz. There are many applications that are using the part at 20MHz and the performance is perfectly adequate. But at 20MHz, performance is reduced from the limits guaranteed in the specification table. This change is intended to apply to future customer designs. No changes are being made to the circuit or the test methodology, so customers who are using these devices with F0 frequencies between 12MHz and 20MHz and are satisfied with the performance will continue to receive the same product.

An error in the Conversion Time calculation using the External Oscillator was corrected to display 178 in the calculation (incorrectly shown as 170). No changes are being made to all devices or test program, this is just a change to the datasheet. The changes are shown on the attached pages of the marked up datasheet. There was no change in form, fit, function, test programs, quality or reliability of the product; this is just a change to the datasheet. New customer designs after December 6, 2014 should adhere to the new datasheet limit.

Should you have any further questions, please feel free to contact your local Linear Technology sales person or you may contact me at 408-432-1900 ext. 2077, or by E-mail JASON.HU@LINEAR.COM. If I do not hear from you by December 06, 2016, we will consider this change approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

POWER REQUIREMENTS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	4.5		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	$\overline{CS}$ = 0V (Note 7) $\overline{CS}$ = V_{CC} (Note 7)	● ●		8 8	11 30	mA μA

TIMING CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	0.1	12 ~~20~~		MHz
t_{HEO}	External Oscillator High Period		●	25		10000	ns
t_{LEO}	External Oscillator Low Period		●	25		10000	ns
t_{CONV}	Conversion Time	OSR = 256 (SDI = 0) OSR = 32768 (SDI = 1) External Oscillator (Note 10, 13)	● ● ●	0.99 126	1.13 145 $\dfrac{40 \cdot OSR + \text{~~170~~} 178}{f_{EOSC}(kHz)}$	1.33 170	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 9) External Oscillator (Notes 9, 10)	●	0.8	0.9 $f_{EOSC}/10$	1	MHz Hz
D_{ISCK}	Internal SCK Duty Cycle	(Note 9)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 8)	●			20	MHz
t_{LESCK}	External SCK Low Period	(Note 8)	●	25			ns
t_{HESCK}	External SCK High Period	(Note 8)	●	25			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 9, 11) External Oscillator (Notes 9, 10)	●	30.9	35.3 $320/f_{EOSC}$	41.6	μs s
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 8)	●		$32/f_{ESCK}$		s
t_1	$\overline{CS}$ ↓ to SDO Low Z	(Note 12)	●	0		25	ns
t_2	$\overline{CS}$ ↑ to SDO High Z	(Note 12)	●	0		25	ns
t_3	$\overline{CS}$ ↓ to SCK ↓	(Note 9)	●		5		μs
t_4	$\overline{CS}$ ↓ to SCK ↑	(Notes 8, 12)	●	25			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			25	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_7	SDI Setup Before SCK ↑	(Note 5)	●	10			ns
t_8	SDI Hold After SCK ↑	(Note 5)	●	10			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 4.5 to 5.5V unless otherwise specified.
V_{REF} = REF$^+$ − REF$^-$; V_{REFCM} = (REF$^+$ + REF$^-$)/2;
V_{IN} = IN$^+$ − IN$^-$; V_{INCM} = (IN$^+$ + IN$^-$)/2.

Note 4: f_O pin tied to GND or to external conversion clock source with f_{EOSC} = 10MHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: The converter uses the internal oscillator.

Note 8: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 9: The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output. In this mode of operation, the SCK pin has a total equivalent load capacitance of C_{LOAD} = 20pF.

Note 10: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses the internal oscillator. f_O = 0V.

Note 12: Guaranteed by design and test correlation.

Note 13: There is an internal reset that adds an additional ~~1μs (typical) to~~ 5 to 15 f_O cycle to the conversion time.

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APPLICATIONS INFORMATION

The sample rate f_S and NULL f_N, my also be adjusted by driving the f_O pin with an external oscillator. The sample rate is $f_S = f_{EOSC}/5$, where f_{EOSC} is the frequency of the clock applied to f_O. Combining a large OSR with a reduced sample rate leads to notch frequencies f_N near DC while maintaining simple antialiasing requirements. A 100kHz clock applied to f_O results in a NULL at 0.6Hz plus all harmonics up to 20kHz, see Figure 14. This is useful in applications requiring digitalization of the DC component of a noisy input signal and eliminates the need of placing a 0.6Hz filter in front of the ADC.

An external oscillator operating from 100kHz to ~~20MHz~~ 12MHz can be implemented using the LTC1799 (resistor set SOT-23 oscillator), see Figure 22. By floating pin 4 (DIV) of the LTC1799, the output oscillator frequency is:

$$f_{OSC} = 10MHz \cdot \left(\frac{10k}{10 \cdot R_{SET}} \right)$$

The normal mode rejection characteristic shown in Figure 14 is achieved by applying the output of the LTC1799 (with $R_{SET} = 100k$) to the f_O pin on the LTC2440 with SDI tied HIGH (OSR = 32768).

Reduced Power Operation

In addition to adjusting the speed/resolution of the LTC2440, the speed/resolution/power dissipation may also be adjusted using the automatic sleep mode. During the conversion cycle, the LTC2440 draws 8mA supply current independent of the programmed speed. Once the conversion cycle is completed, the device automatically enters a low power sleep state drawing 8µA. The device remains in this state as long as $\overline{CS}$ is HIGH and data is not shifted out. By adjusting the duration of the sleep state (hold $\overline{CS}$ HIGH longer) and the duration of the conversion cycle (programming OSR) the DC power dissipation can be reduced, see Figure 16.

For example, if the OSR is programmed at the fastest rate (OSR = 64, $t_{CONV} = 0.285ms$) and the sleep state is 10ms, the effective output rate is approximately 100Hz while the average supply current is reduced to 240µA. By further extending the sleep state to 100ms, the effective output rate of 10Hz draws on average 30µA. Noise, power, and speed can be optimized by adjusting the OSR (Noise/Speed) and sleep mode duration (Power).
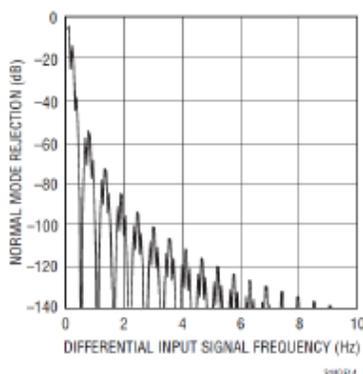

Figure 14. LTC2440 Normal Mode Rejection (External Oscillator at 90kHz)

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	0.1		12 ~~20~~	MHz
t_{HEO}	External Oscillator High Period		●	25		10000	ns
t_{LEO}	External Oscillator Low Period		●	25		10000	ns
t_{CONV}	Conversion Time	OSR = 256 (SDI = 0)	●	0.99	1.13	1.33	ms
		OSR = 32768 (SDI = 1)	●	126	145	170	ms
		External Oscillator (Notes 10, 13) 1x Mode	●		$\frac{40 \cdot OSR + \text{~~170~~} 178}{f_{EOSC} (KHz)}$		ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 9)	●	0.8	0.9	1	MHz
		External Oscillator (Notes 9, 10)			$f_{EOSC}/10$		Hz
D_{ISCK}	Internal SCK Duty Cycle	(Note 9)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 8)	●			20	MHz
f_{LESCK}	External SCK Low Period	(Note 8)	●	25			ns
t_{HESCK}	External SCK High Period	(Note 8)	●	25			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 9, 11)	●	30.9	35.3	41.6	μs
		External Oscillator (Notes 9, 10)	●		$320/f_{EOSC}$		s
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 8)	●		$32/f_{ESCK}$		s
t_1	$\overline{CS} \downarrow$ to SDO Low Z	(Note 12)	●	0		25	ns
t_2	$\overline{CS} \uparrow$ to SDO High Z	(Note 12)	●	0		25	ns
t_3	$\overline{CS} \downarrow$ to SCK $\downarrow$	(Note 9)			5		μs
t_4	$\overline{CS} \downarrow$ to SCK $\uparrow$	(Note 8, 12)	●	25			ns
t_{KQMAX}	SCK $\downarrow$ to SDO Valid		●			25	ns
t_{KQMIN}	SDO Hold After SCK $\downarrow$	(Note 5)	●	15			ns
t_5	SCK Setup Before $\overline{CS} \downarrow$		●	50			ns
t_6	SCK Hold After $\overline{CS} \downarrow$		●			50	ns
t_7	SDI Setup Before SCK $\uparrow$	(Note 5)	●	10			ns
t_8	SDI Hold After SCK $\uparrow$	(Note 5)	●	10			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 4.5V to 5.5V unless otherwise specified.
V_{REF} = REF$^+$ – REF$^-$, V_{REFCM} = (REF$^+$ + REF$^-$)/2;
V_{IN} = SEL$^+$ – SEL$^-$, V_{INCM} = (SEL$^+$ + SEL$^-$)/2.

Note 4: F_O pin tied to GND or to external conversion clock source with f_{EOSC} = 10MHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: The converter uses the internal oscillator.

Note 8: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 9: The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output. In this mode of operation, the SCK pin has a total equivalent load capacitance of C_{LOAD} = 20pF.

Note 10: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in Hz.

Note 11: The converter uses the internal oscillator. F_O = 0V.

Note 12: Guaranteed by design and test correlation.

Note 13: There is an internal reset that adds an additional ~~1μs (typ) to the~~ conversion time. 5 to 15 f_0 cycle to the

Note 14: In order to achieve optimum linearity, the amplifier power positive supply input (V$^+$) must exceed the maximum input voltage level by 2V or greater. The negative amplifier power supply input (V$^-$) must be at least 200mV below the minimum input voltage level.

Note 15: Amplifiers are externally compensated with 0.1μF.

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	0.1		12 ~~20~~	MHz
t_{HEO}	External Oscillator High Period		●	25		10000	ns
t_{LEO}	External Oscillator Low Period		●	25		10000	ns
t_{CONV}	Conversion Time	OSR = 256 (SDI = 0)	●	0.99	1.13	1.33	ms
		OSR = 32768 (SDI = 1)	●	126	145	170	ms
		External Oscillator (Notes 10, 13) 1x Mode	●		$\frac{40 \cdot OSR + \text{~~170~~} 178}{f_{EOSC} \text{ (KHz)}}$		ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 9)	●	0.8	0.9	1	MHz
		External Oscillator (Notes 9, 10)			$f_{EOSC}/10$		Hz
D_{ISCK}	Internal SCK Duty Cycle	(Note 9)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 8)	●			20	MHz
f_{LESCK}	External SCK Low Period	(Note 8)	●	25			ns
t_{HESCK}	External SCK High Period	(Note 8)	●	25			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 9, 11)	●	30.9	35.3	41.6	µs
		External Oscillator (Notes 9, 10)	●		$320/f_{EOSC}$		s
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 8)	●		$32/f_{ESCK}$		s
t_1	$\overline{CS} \downarrow$ to SDO Low Z	(Note 12)	●	0		25	ns
t_2	$\overline{CS} \uparrow$ to SDO High Z	(Note 12)	●	0		25	ns
t_3	$\overline{CS} \downarrow$ to SCK $\downarrow$	(Note 9)			5		µs
t_4	$\overline{CS} \downarrow$ to SCK $\uparrow$	(Note 8, 12)	●	25			ns
t_{KQMAX}	SCK $\downarrow$ to SDO Valid		●			25	ns
t_{KQMIN}	SDO Hold After SCK $\downarrow$	(Note 5)	●	15			ns
t_5	SCK Setup Before $\overline{CS} \downarrow$		●	50			ns
t_6	SCK Hold After $\overline{CS} \downarrow$		●			50	ns
t_7	SDI Setup Before SCK $\uparrow$	(Note 5)	●	10			ns
t_8	SDI Hold After SCK $\uparrow$	(Note 5)	●	10			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: $V_{CC} = 4.5V$ to $5.5V$ unless otherwise specified. $V_{REF} = REF^+ - REF^-$, $V_{REFCM} = (REF^+ + REF^-)/2$; $V_{IN} = SEL^+ - SEL^-$, $V_{INCM} = (SEL^+ + SEL^-)/2$.

Note 4: F_O pin tied to GND or to external conversion clock source with $f_{EOSC} = 10MHz$ unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: The converter uses the internal oscillator.

Note 8: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 9: The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output. In this mode of operation, the SCK pin has a total equivalent load capacitance of $C_{LOAD} = 20pF$.

Note 10: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in Hz.

Note 11: The converter uses the internal oscillator. $F_O = 0V$.

Note 12: Guaranteed by design and test correlation.

Note 13: There is an internal reset that adds an additional ~~1µs (typ) to the~~ conversion time. 5 to 15 f_0 cycle to the

Note 14: In order to achieve optimum linearity, the amplifier power positive supply input (V^+) must exceed the maximum input voltage level by 2V or greater. The negative amplifier power supply input (V^-) must be at least 200mV below the minimum input voltage level.

Note 15: Amplifiers are externally compensated with $0.1µF$.

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APPLICATIONS INFORMATION

If F_O is grounded, f_S is set by the on-chip oscillator at 1.8MHz ±5% (over supply and temperature variations). At an OSR of 32,768, the first NULL is at f_N = 55Hz and the no latency output rate is $f_N/8$ = 6.9Hz. At the maximum OSR, the noise performance of the device is 220nV$_{RMS}$ with better than 80dB rejection of 50Hz ±2% and 60Hz ±2%. Since the OSR is large (32,768) the wide band rejection is extremely large and the antialiasing requirements are simple. The first multiple of f_S occurs at 55Hz • 32,768 = 1.8MHz, see Figure 12.

The first NULL becomes f_N = 7.03kHz with an OSR of 256 (an output rate of 879Hz) and F_O grounded. While the NULL has shifted, the sample rate remains constant. As a result of constant modulator sampling rate, the linearity, offset and full-scale performance remains unchanged as does the first multiple of f_S.

The sample rate f_S and NULL f_N, may also be adjusted by driving the F_O pin with an external oscillator. The sample rate is f_S = $f_{EOSC}/5$, where f_{EOSC} is the frequency of the clock applied to F_O. Combining a large OSR with a reduced sample rate leads to notch frequencies f_N near DC while maintaining simple antialiasing requirements. A 100kHz clock applied to F_O results in a NULL at 0.6Hz plus all harmonics up to 20kHz, see Figure 13. This is useful in applications requiring digitalization of the DC component of a noisy input signal and eliminates the need of placing a 0.6Hz filter in front of the ADC.

An external oscillator operating from 100kHz to 12MHz can be implemented using the LTC1799 (resistor set SOT-23 oscillator), see Figure 14. By floating pin 4 (DIV) of the LTC1799, the output oscillator frequency is:

$$f_{OSC} = 10MHz \cdot \left(\frac{10k}{10 \cdot R_{SET}} \right)$$

The normal mode rejection characteristic shown in Figure 13 is achieved by applying the output of the LTC1799 (with R_{SET} = 100k) to the F_O pin on the LTC2442 with OSR = 32,768.

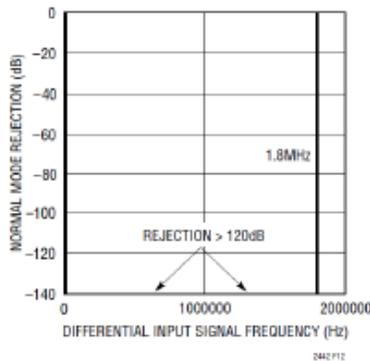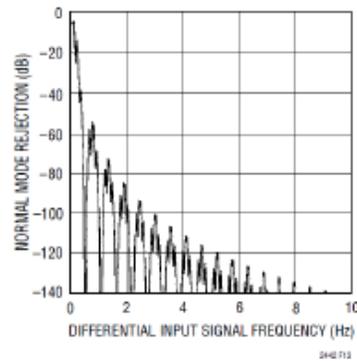Figure 12. Normal Mode Rejection (Internal Oscillator)

Figure 13. Normal Mode Rejection (Internal Oscillator at 90kHz)

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LTC2444/LTC2445/
LTC2448/LTC2449

DIGITAL INPUTS AND DIGITAL OUTPUTS
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O, SDI	$4.5V \leq V_{CC} \leq 5.5V$	●	2.5			V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O, SDI	$4.5V \leq V_{CC} \leq 5.5V$	●			0.8	V
V_{IH}	High Level Input Voltage SCK	$4.5V \leq V_{CC} \leq 5.5V$ (Note 8)	●	2.5			V
V_{IL}	Low Level Input Voltage SCK	$4.5V \leq V_{CC} \leq 5.5V$ (Note 8)	●			0.8	V
I_{IN}	Digital Input Current $\overline{CS}$, F_O, EXT, SDI, SDI	$0V \leq V_{IN} \leq V_{CC}$	●	–10		10	μA
I_{IN}	Digital Input Current SCK	$0V \leq V_{IN} \leq V_{CC}$ (Note 8)	●	–10		10	μA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O, SDI				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 8)			10		pF
V_{OH}	High Level Output Voltage SDO, BUSY	$I_O = –800μA$	●	$V_{CC} – 0.5V$			V
V_{OL}	Low Level Output Voltage SDO, BUSY	$I_O = 1.6mA$	●			0.4V	V
V_{OH}	High Level Output Voltage SCK	$I_O = –800μA$ (Note 9)	●	$V_{CC} – 0.5V$			V
V_{OL}	Low Level Output Voltage SCK	$I_O = 1.6mA$ (Note 9)	●			0.4V	V
I_{OZ}	Hi-Z Output Leakage SDO		●	–10		10	μA

POWER REQUIREMENTS
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	4.5		5.5	V
I_{CC}	Supply Current						
	Conversion Mode	$\overline{CS} = 0V$ (Note 7)	●		8	11	mA
	Sleep Mode	$\overline{CS} = V_{CC}$ (Note 7)	●		8	30	μA

TIMING CHARACTERISTICS
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	0.1	12 ~~20~~		MHz
t_{HEO}	External Oscillator High Period		●	25		10000	ns
t_{LEO}	External Oscillator Low Period		●	25		10000	ns
t_{CONV}	Conversion Time	OSR = 256 (SDI = 0)	●	0.99	1.13	1.33	ms
		OSR = 32768 (SDI = 1)	●	126	145	170	ms
		External Oscillator (Notes 10, 13) 1x Mode	●		$\frac{40 \cdot OSR}{f_{EOSC} (kHz)}$ ~~170~~ 178		ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 9)	●	0.8	0.9	1	MHz
		External Oscillator (Notes 9, 10)			$f_{EOSC}/10$		Hz

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TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
D_{ISCK}	Internal SCK Duty Cycle	(Note 9)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 8)	●			20	MHz
t_{LESCK}	External SCK Low Period	(Note 8)	●	25			ns
t_{HESCK}	External SCK High Period	(Note 8)	●	25			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 9, 11)	●	41.6	35.3	30.9	μs
		External Oscillator (Notes 9, 10)	●		$320/f_{EOSC}$		s
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 8)	●		$32/f_{ESCK}$		s
t_1	$\overline{CS} \downarrow$ to SDO Low Z	(Note 12)	●	0		25	ns
t_2	$\overline{CS} \uparrow$ to SDO High Z	(Note 12)	●	0		25	ns
t_3	$\overline{CS} \downarrow$ to SCK $\downarrow$	(Note 9)			5		μs
t_4	$\overline{CS} \downarrow$ to SCK $\uparrow$	(Notes 8, 12)	●	25			ns
t_{KQMAX}	SCK $\downarrow$ to SDO Valid		●			25	ns
t_{KQMIN}	SDO Hold After SCK $\downarrow$	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS} \downarrow$		●	50			ns
t_6	SCK Hold After $\overline{CS} \downarrow$		●			50	ns
t_7	SDI Set-Up Before SCK $\uparrow$	(Note 5)	●	10			ns
t_8	SDI Hold After SCK $\uparrow$	(Note 5)	●	10			ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: $V_{CC} = 4.5V$ to $5.5V$ unless otherwise specified.
$V_{REF} = REF^+ - REF^-$, $V_{REFCM} = (REF^+ + REF^-)/2$;
$V_{IN} = IN^+ - IN^-$, $V_{INCM} = (IN^+ + IN^-)/2$.

Note 4: F_O pin tied to GND or to external conversion clock source with $f_{EOSC} = 10MHz$ unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: The converter uses the internal oscillator.

Note 8: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 9: The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output. In this mode of operation, the SCK pin has a total equivalent load capacitance of $C_{LOAD} = 20pF$.

Note 10: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in Hz.

Note 11: The converter uses the internal oscillator. $F_O = 0V$.

Note 12: Guaranteed by design and test correlation.

Note 13: There is an internal reset that adds an additional ~~1μs (typ) to the~~ 5 to 15 f_0 cycle to the conversion time.

PIN FUNCTIONS

GND (Pins 1, 4, 5, 6, 31, 32, 33): Ground. Multiple ground pins internally connected for optimum ground current flow and V_{CC} decoupling. Connect each one of these pins to a common ground plane through a low impedance connection. All 7 pins must be connected to ground for proper operation.

BUSY (Pin 2): Conversion in Progress Indicator. This pin is HIGH while the conversion is in progress and goes LOW indicating the conversion is complete and data is ready. It remains LOW during the sleep and data output states. At the conclusion of the data output state, it goes HIGH indicating a new conversion has begun.

EXT (Pin 3): Internal/External SCK Selection Pin. This pin is used to select internal or external SCK for outputting/inputting data. If $\overline{EXT}$ is tied low, the device is in the external SCK mode and data is shifted out of the device under the control of a user applied serial clock. If $\overline{EXT}$ is tied high, the internal serial clock mode is selected. The device generates its own SCK signal and outputs this on the SCK pin. A framing signal BUSY (Pin 2) goes low indicating data is being output.

COM (Pin 7): The common negative input (IN⁻) for all single ended multiplexer configurations. The voltage on CH0-CH15 and COM pins can have any value between

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APPLICATIONS INFORMATION

If F_O is grounded, f_S is set by the on-chip oscillator at 1.8MHz ±5% (over supply and temperature variations). At an OSR of 32,768, the first NULL is at f_N = 55Hz and the no latency output rate is $f_N/8$ = 6.9Hz. At the maximum OSR, the noise performance of the device is 280nV$_{RMS}$ (LTC2444/LTC2448) and 200nV$_{RMS}$ (LTC2445/LTC2449) with better than 80dB rejection of 50Hz±2% and 60Hz±2%. Since the OSR is large (32,768) the wide band rejection is extremely large and the antialiasing requirements are simple. The first multiple of f_S occurs at 55Hz • 32,768 = 1.8MHz, see Figure 12.

The first NULL becomes f_N = 7.04kHz with an OSR of 256 (an output rate of 880Hz) and F_O grounded. While the NULL has shifted, the sample rate remains constant. As a result of constant modulator sampling rate, the linearity, offset and full-scale performance remains unchanged as does the first multiple of f_S.

The sample rate f_S and NULL f_N, may also be adjusted by driving the F_O pin with an external oscillator. The sample rate is f_S = $f_{EOSC}/5$, where f_{EOSC} is the frequency of the clock applied to F_O. Combining a large OSR with a reduced sample rate leads to notch frequencies f_N near DC while maintaining simple antialiasing requirements. A 100kHz clock applied to F_O results in a NULL at 0.6Hz plus all harmonics up to 20kHz, see Figure 13. This is useful in applications requiring digitalization of the DC component of a noisy input signal and eliminates the need of placing a 0.6Hz filter in front of the ADC.

An external oscillator operating from 100kHz to 12MHz can be implemented using the LTC1799 (resistor set SOT-23 oscillator), see Figure 16. By floating pin 4 (DIV) of the LTC1799, the output oscillator frequency is:

$$f_{OSC} = 10MHz \cdot \left(\frac{10k}{10 \cdot R_{SET}}\right)$$

The normal mode rejection characteristic shown in Figure 13 is achieved by applying the output of the LTC1799 (with R_{SET} = 100k) to the F_O pin on the LTC2444/LTC2445/LTC2448/LTC2449 with SDI tied HIGH (OSR = 32768).
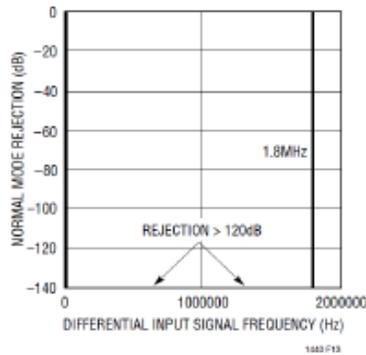

Figure 12. LTC2444/LTC2445/LTC2448/LTC2449 Normal Mode Rejection (Internal Oscillator)
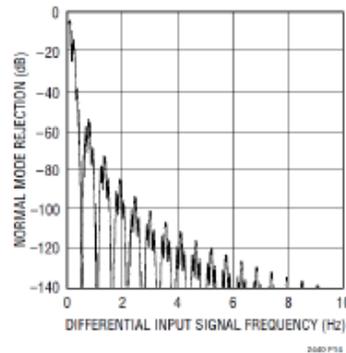

Figure 13. LTC2444/LTC2445/LTC2448/LTC2449 Normal Mode Rejection (External Oscillator at 90kHz)

LTC2446/LTC2447

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O, SDI	$4.5V \leq V_{CC} \leq 5.5V$	●	2.5			V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O, SDI	$4.5V \leq V_{CC} \leq 5.5V$	●			0.8	V
V_{IH}	High Level Input Voltage SCK	$4.5V \leq V_{CC} \leq 5.5V$ (Note 8)	●	2.5			V
V_{IL}	Low Level Input Voltage SCK	$4.5V \leq V_{CC} \leq 5.5V$ (Note 8)	●			0.8	V
I_{IN}	Digital Input Current CS, F_O, EXT, ~~SDI~~ SDI	$0V \leq V_{IN} \leq V_{CC}$	●	−10		10	μA
I_{IN}	Digital Input Current SCK	$0V \leq V_{IN} \leq V_{CC}$ (Note 8)	●	−10		10	μA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O, SDI				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 8)			10		pF
V_{OH}	High Level Output Voltage SDO, BUSY	$I_O = -800μA$	●	$V_{CC} - 0.5V$			V
V_{OL}	Low Level Output Voltage SDO, BUSY	$I_O = 1.6mA$	●			0.4~~V~~	V
V_{OH}	High Level Output Voltage SCK	$I_O = -800μA$ (Note 9)	●	$V_{CC} - 0.5V$			V
V_{OL}	Low Level Output Voltage SCK	$I_O = 1.6mA$ (Note 9)	●			0.4~~V~~	V
I_{OZ}	Hi-Z Output Leakage SDO		●	−10		10	μA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	4.5		5.5	V
I_{CC}	Supply Current						
	Conversion Mode	$\overline{CS} = 0V$ (Note 7)	●		8	11	mA
	Sleep Mode	$\overline{CS} = V_{CC}$ (Note 7)	●		8	30	μA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	0.1	12 ~~20~~		MHz
t_{HEO}	External Oscillator High Period		●	25		10000	ns
t_{LEO}	External Oscillator Low Period		●	25		10000	ns
t_{CONV}	Conversion Time	OSR = 256	●	0.99	1.13	1.33	ms
		OSR = 32768	●	126	145	170	ms
		External Oscillator (Notes 10, 13) 1x Mode	●		$\frac{40 \cdot OSR}{f_{EOSC} (kHz)}$ ~~170~~ 178		ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 9)	●	0.8	0.9	1	MHz
		External Oscillator (Notes 9, 10)			$f_{EOSC}/10$		Hz

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TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
D_{ISCK}	Internal SCK Duty Cycle	(Note 9)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 8)	●			20	MHz
t_{LESCK}	External SCK Low Period	(Note 8)	●	25			ns
t_{HESCK}	External SCK High Period	(Note 8)	●	25			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 9, 11) External Oscillator (Notes 9, 10)	● ●	41.6	35.3 $320/f_{EOSC}$	30.9	µs s
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 8)	●		$32/f_{ESCK}$		s
t_1	$\overline{CS}$ ↓ to SDO Low Z	(Note 12)	●	0		25	ns
t_2	$\overline{CS}$ ↑ to SDO High Z	(Note 12)	●	0		25	ns
t_3	$\overline{CS}$ ↓ to SCK ↓	(Note 9)	●		5		µs
t_4	$\overline{CS}$ ↓ to SCK ↑	(Notes 8, 12)	●	25			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			25	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Setup Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns
t_7	SDI Setup Before SCK ↑	(Note 5)	●	10			ns
t_8	SDI Hold After SCK ↑	(Note 5)	●	10			ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: $V_{CC} = 4.5V$ to $5.5V$ unless otherwise specified. $V_{REF} = REF^+ - REF^-$, $V_{REFCM} = (REF^+ + REF^-)/2$; REF^+ is the positive reference input, REF^- is the negative reference input; $V_{IN} = IN^+ - IN^-$, $V_{INCM} = (IN^+ + IN^-)/2$.

Note 4: F_O pin tied to GND or to external conversion clock source with $f_{EOSC} = 10MHz$ unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: The converter uses the internal oscillator.

Note 8: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 9: The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output. In this mode of operation, the SCK pin has a total equivalent load capacitance of $C_{LOAD} = 20pF$.

Note 10: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in Hz.

Note 11: The converter uses the internal oscillator. $F_O = 0V$.

Note 12: Guaranteed by design and test correlation.

Note 13: There is an internal reset that adds an additional 1µs (typ) to the 5 to 15 f_O cycle to the conversion time.

PIN FUNCTIONS

GND (Pins 1, 4, 5, 6, 31, 32, 33): Ground. Multiple ground pins internally connected for optimum ground current flow and V_{CC} decoupling. Connect each one of these pins to a common ground plane through a low impedance connection. All seven pins must be connected to ground for proper operation.

BUSY (Pin 2): Conversion in Progress Indicator. This pin is HIGH while the conversion is in progress and goes LOW indicating the conversion is complete and data is ready. It remains LOW during the sleep and data output states. At the conclusion of the data output state, it goes HIGH indicating a new conversion has begun.

EXT (Pin 3): Internal/External SCK Selection Pin. This pin is used to select internal or external SCK for outputting/inputting data. If $\overline{EXT}$ is tied low, the device is in the external SCK mode and data is shifted out of the device under the control of a user applied serial clock. If $\overline{EXT}$ is tied high, the internal serial clock mode is selected. The device generates its own SCK signal and outputs this on the SCK pin. A framing signal BUSY (Pin 2) goes low indicating data is being output.

COM (Pin 7): The common negative input (IN^-) for all single ended multiplexer configurations. The voltage on CH0-CH7 and COM pins can have any value between GND

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LTC2446/LTC2447

APPLICATIONS INFORMATION

offset and full-scale performance remain unchanged as does the first multiple of f_S.

The sample rate f_S and NULL f_N, may also be adjusted by driving the F_O pin with an external oscillator. The sample rate is $f_S = f_{EOSC}/5$, where f_{EOSC} is the frequency of the clock applied to F_O. Combining a large OSR with a reduced sample rate leads to notch frequencies f_N near DC while maintaining simple antialiasing requirements. A 100kHz clock applied to F_O results in a NULL at 0.6Hz plus all harmonics up to 20kHz, see Figure 13. This is useful in applications requiring digitalization of the DC component of a noisy input signal and eliminates the need of placing a 0.6Hz filter in front of the ADC.
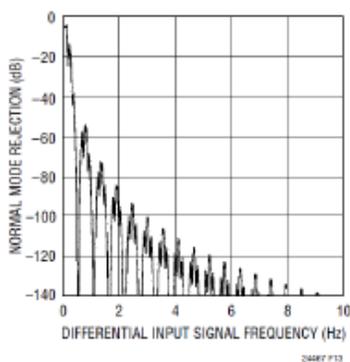

Figure 13. LTC2446/LTC2447 Normal
Mode Rejection (External Oscillator at 90kHz)

An external oscillator operating from 100kHz to ~~20MHz~~ 12MHz can be implemented using the LTC1799 (resistor set SOT-23 oscillator), see Figure 14. By floating pin 4 (DIV) of the LTC1799, the output oscillator frequency is:

$$f_{OSC} = 10MHz \cdot \left(\frac{10k}{10 \cdot R_{SET}} \right)$$

The normal mode rejection characteristic shown in Figure 13 is achieved by applying the output of the LTC1799 (with $R_{SET} = 100k$) to the F_O pin on the LTC2446/LTC2447 with SDI tied HIGH (OSR = 32768).

Multiple Ratiometric and Absolute Measurements

The LTC2446/LTC2447 combine a high precision, high speed delta-sigma converter with a versatile front-end
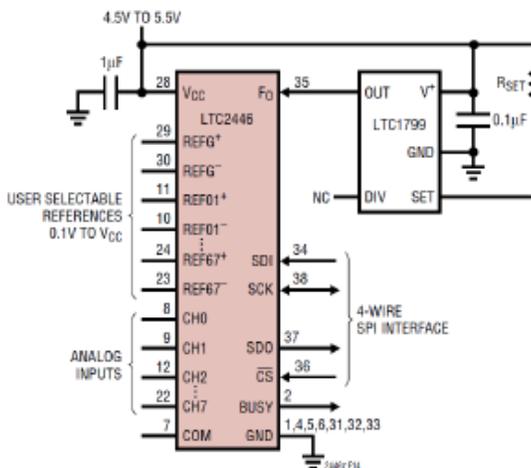

Figure 14. Simple External Clock Source

multiplexer. The unique no latency architecture allows seamless changes in both input channel and reference while the absolute accuracy ensures excellent matching between both analog input channels and reference channels. Any set of inputs (differential or single-ended) can perform a conversion with one of two references. For Bridges, RTDs and other ratiometric devices, each set of channels can perform a conversion with respect to a unique reference voltage. For Thermocouples, voltage sense, current sense and other absolute sensors, each set of channels can perform a conversion with respect to a single global reference voltage (see Figure 15). This allows users to measure both multiple absolute and multiple ratio metric sensors with the same device in such applications as flow, gas chromatography, multiple RTDs or bridges, or universal data acquisition.

Average Input Current

The LTC2446 switches the input and reference to a 2pF capacitor at a frequency of 1.8MHz. A simplified equivalent circuit is shown in Figure 16. The sample capacitor for the LTC2447 is 4pF, and its average input current is externally buffered from the input source.

The average input and reference currents can be expressed in terms of the equivalent input resistance of the sample capacitor, where: $Req = 1/(f_{SW} \cdot Ceq)$.

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