KSZ8873

KSZ8873 Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the KSZ8873 family of devices. The silicon errata discussed in this document are for the silicon revisions listed in Table 1. A summary of KSZ8873 silicon errata is provided in Table 2.

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Silicon Revision
KSZ8873FLL, KSZ8873FLLI, KSZ8873MLL, KSZ8873MLLI, KSZ8873MML, KSZ8873MMLI, KSZ8873RLL, KSZ8873RLLI	A2
KSZ8873MLL-AM, KSZ8873RLLU	A3

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary	Affected Silicon Revisions
1.	LinkMD does not work on Port 1	A2
2.	Cannot write certain bits in MIIM Basic Control Register 0	A2
3.	RMII output timing is out of specification (RLL device only)	A2
4.	Port 1 does not respond to received flow control PAUSE frames	A2
5.	The rate for egress port rate limiting is incorrect when tag insertion is enabled	A2, A3
6.	Switch won't start in I2C Master Mode	A2, A3
7.	SMI management interface does not function if SPISN pin is not pulled high	A2, A3
8.	Receiver error in 100BASE-TX mode following Soft Power Down	A2, A3

Silicon Errata Issues

Module 1: LinkMD does not work on Port 1

DESCRIPTION

The LinkMD status result in the register is incorrect for Port 1.

END USER IMPLICATIONS

LinkMD cannot be used for Port 1.

Work around

None.

PLAN

This erratum will not be corrected in a future revision.

Module 2: Cannot write certain bits in MIIM Basic Control Register 0

DESCRIPTION

Bits 8, 12 and 13 in MIIM register 0 (Basic Control Register) cannot be written. These bits control Force 100BASE-TX, Auto-Negotiation and Force Duplex for the PHYs. This applies to both ports 1 and 2.

END USER IMPLICATIONS

These settings can be set at power-up by pin strapping options. However, if using the MIIM interface, these PHY control bits cannot be changed after power-up.

There are copies of these control bits in the 8-bit registers which are accessible via the SMI and SPI interfaces. (See register 0x1C for port 1 and 0x2C for port 2.) There are no problems with writing to these registers.

Work around

Use pin strapping to set the value of these control bits. Use SMI or SPI for register access.

PLAN

This erratum will not be corrected in a future revision.

Module 3: RMII output timing is out of specification (RLL device only)

DESCRIPTION

The maximum output delay (t_{OD}) on the RMII bus is 18ns, which exceeds the specification of 16ns given in the data sheet.

END USER IMPLICATIONS

The increased output delay time reduces the setup time into the connected RMII device. If that setup time is violated, data errors can occur, resulting in errored or dropped packets.

Work around

The following steps can be taken to improve the setup time into the device connected to the RMII port of the KSZ8873RLL:

- Keep the KSZ8873 RMII output data and control signals (RXEN and RXD[1:0]) to the other device as short as possible.
- Do not use an RMII clocking scheme in which the other device sources the RMII 50MHz clock to the KSZ8873. The RMII clock source should be either the KSZ8873 or a separate oscillator.
- If the KSZ8873 is the source of the RMII 50MHz clock, add additional trace delay on the RMII 50MHz clock going into the other RMII device relative to the RXEN and RXD[1:0] traces.
- If an external oscillator is the source of the RMII 50MHz clock, then make the RMII clock trace to the KSZ8873 as short as possible, and add trace delay on the RMII clock going to the other RMII device.

PLAN

This erratum will not be corrected in a future revision.

Module 4: Port 1 does not respond to received flow control PAUSE frames

DESCRIPTION

Port 1 does not respond to received PAUSE control frames. This issue does not affect the generation (transmission) of PAUSE frames by Port 1 in response to congestion within the KSZ8873 switch fabric. Port 2 does not exhibit this issue; it responds properly to received PAUSE frames.

END USER IMPLICATIONS

The switch will not suspend transmission on Port 1 when requested to do so by its link partner sending PAUSE frames. PAUSE frames are received and are counted in the MIB RxPausePkts counter (offset 0xA), but they are not acted upon.

Work around

There is no direct workaround for this issue. However, if Port 1 and Port 2 have different link partners and/or different traffic patterns, it may be possible to assign Ports 1 and 2 with this asymmetry in mind, such that port 1 gets the configuration that is less likely to generate flow control requests into that port.

PLAN

This erratum will not be corrected in a future revision.

Module 5: The rate for egress port rate limiting is incorrect when tag insertion is enabled

DESCRIPTION

When tag insertion is enabled on an egress port and egress port rate limiting is turned on, the egress rate limit will be about twice the programmed value. When tag insertion is disabled, the egress rate limit is as programmed.

END USER IMPLICATIONS

The egress rate may exceed the programmed rate limit if tag insertion is enabled.

Work around

If both features are needed, use an egress rate setting of half the desired rate. However, even with this adjustment, the rate limit control may not be precise.

PLAN

This erratum will not be corrected in a future revision.

Module 6: Switch won't start in I^2C Master Mode

DESCRIPTION

In I^2C master mode, the switch reads register configurations from an attached EEPROM when exiting reset. In this mode, the Start Switch bit in Register 1 is cleared to '0', which disables the switch.

END USER IMPLICATIONS

After configuration from the external EEPROM, the switch is disabled and cannot be used since I^2C master mode implies that there is no other external control of the switch registers.

Work around

When programming the EEPROM, set Register 78 (0x4E) bit 0 = '1'. This corrects the problem.

PLAN

This erratum will not be corrected in a future revision.

Module 7: SMI management interface does not function if SPISN pin is not pulled high

DESCRIPTION

If SPISN (pin 39) is left floating when the MIIM / SMI management mode is selected, the SMI interface will not work. This is due to the internal pull-down resistor on the SPISN pin. The MIIM management mode is unaffected.

END USER IMPLICATIONS

Registers cannot be accessed via SMI management interface if SPISN floats to a low level.

Work around

The problem is solved by pulling SPISN high with an external resistor to VDDIO. Use a resistor value between 1kΩ and 10kΩ.

PLAN

This erratum will not be corrected in a future revision.

Module 8: Receiver error in 100BASE-TX mode following Soft Power Down

DESCRIPTION

Some KSZ8873 devices may exhibit receiver errors after transitioning from Soft Power Down mode to Normal mode, as controlled by register 195 (0xC3) bits [1:0]. When exiting Soft Power Down mode, the receiver blocks may not start up properly, causing the PHY to miss data and exhibit erratic behavior. The problem may appear on either port 1 or port 2, or both ports. The problem occurs only for 100BASE-TX, not 10BASE-T.

END USER IMPLICATIONS

When the failure occurs, the following symptoms are seen on the affected port(s):

- The port is able to link
- LED0 blinks, even when there is no traffic
- The MIB counters indicate receive errors (Rx Fragments, Rx Symbol Errors, Rx CRC Errors, Rx Alignment Errors)
- Only a small fraction of packets is correctly received and forwarded through the switch. Most packets are dropped due to receive errors.

The failing condition cannot be corrected by the following:

- Removing and reconnecting the cable
- Hardware reset
- Software Reset and PCS Reset bits in register 67 (0x43)

Work around

The problem can be corrected by setting and then clearing the Port Power Down bits (registers 29 (0x1D) and 45 (0x2D), bit 3). This must be done separately for each affected port after returning from Soft Power Down Mode to Normal Mode. The following procedure will ensure no further issues due to this erratum.

To enter Soft Power Down Mode, set register 195 (0xC3), bits [1:0] = 10.

To exit Soft Power Down Mode, follow these steps:

1. Set register 195 (0xC3), bits [1:0] = 00 // Exit soft power down mode
2. Wait 1ms minimum
3. Set register 29 (0x1D), bit [3] = 1 // Enter PHY port 1 power down mode
4. Set register 29 (0x1D), bit [3] = 0 // Exit PHY port 1 power down mode
5. Set register 45 (0x2D), bit [3] = 1 // Enter PHY port 2 power down mode
6. Set register 45 (0x2D), bit [3] = 0 // Exit PHY port 2 power down mode

PLAN

This erratum will not be corrected in a future revision.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000830A (04-10-19)	All	Converted to Microchip format.
	Module 2.	"These bits control Force 100," changed to "These bits control Force 100BASE-TX"
	Module 7.	Added new erratum: SMI management interface does not function if SPISN pin is not pulled high
	Module 8.	Added new erratum: Receiver error in 100BASE-TX mode following Soft Power Down

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