



Quality Alert – Kintex UltraScale Potential Lifetime Reduction of I2C_SDA, I2C_SCL and PERSTN0 and PERSTN1 I/O

XCN15040 (v1.0) November 24, 2015

Quality Alert

Overview

The purpose of this notification is to communicate a potential risk to Kintex Ultrascale FPGA product lifetimes affecting the functionality of the System Monitor I2C SDA and SCL and PCI Express® reset I/O in Bank 65 with Xilinx Vivado Tools 2015.3 or earlier with 3.3V I/O signaling levels. I/O signaling levels of 1.8V and lower are not impacted by this issue.

Description

Kintex UltraScale devices include dual-purpose I/O that can provide dedicated connections to the System Monitor I2C interface and the integrated block for PCI Express reset input. These pin names are documented as IO_L23N_T3U_N9_I2C_SDA_65, IO_L23P_T3U_N8_I2C_SCL_65, IO_T3U_N12_PERSTN0_65 and IO_T1U_N12_PERSTN1_65 in the Kintex UltraScale device pinout tables.

When these I/O are used for their dedicated I2C_SDA, I2C_SCL, PERSTN0 or PERSTN1 function, Vivado Tools 2015.3 or earlier will incorrectly enable a circuit path connecting the I/O to internal low voltage circuits. When the I/O is externally connected to 3.3V signaling levels, it will result in the external signal not reaching the full logic high voltage level of 3.3V, increased I/O leakage levels and reduced lifetime of the internal low-voltage circuits and a loss of functionality for the I/O.

I/O signaling levels of 2.5V will result in a reduction in the logic high-voltage level, but will not result in a lifetime reduction for these I/O. I/O signaling levels of 1.8V and lower are not impacted by this issue.

Products Affected

This alert impacts Kintex Ultrascale devices in Table 1 using bitstreams meeting the application profile described above and created by Vivado Tools 2015.3 or earlier.

Table 1: Affected Devices

Kintex UltraScale Device Names					
XCKU025	XCKU035	XCKU040	XCKU060	XCKU085	XCKU115

Note: XCKU095 is unaffected since it does not support 3.3V signaling in Bank 65.

Corrective Action

This issue has been corrected in Vivado Tools 2015.4 and later.

Required Action

Affected customers using bitstreams created in Vivado Tools 2015.3 or earlier and meeting the application profile outlined in the Description section must regenerate the bitstream using Vivado Tools 2015.4 and upgrade all appropriate systems to ensure lifetime targets are met for their products. Customers using 2.5V signaling are advised to regenerate the bitstream using Vivado Tools 2015.4 and upgrade all appropriate systems to ensure lifetime targets are met for their products. Customers using 1.8V signaling for these pins are not required to take action. For additional recommendations and guidance see [AR65998](#).

Upon request, reliability lifetime modeling data and support can be made available for assessing your specific use model.

For additional information or questions, please contact your Xilinx sales representative.

Important Notice: Xilinx Customer Notifications (XCNs, XDNs, and Quality Alerts) can be delivered via e-mail alerts sent by the Support website (<http://www.xilinx.com/support>). Register today and personalize your “Documentation and Design Advisory Alerts” area to include Customer Notifications. Xilinx Support provides many benefits, including the ability to receive alerts for new and updated information about specific products, as well as alerts for other publications such as data sheets, errata, application notes, etc. For information on how to sign up, refer to Answer Record 18683: <http://www.xilinx.com/support/answers/18683.htm>.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
11/24/2015	1.0	Initial release.

Notice of Disclaimer

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>.