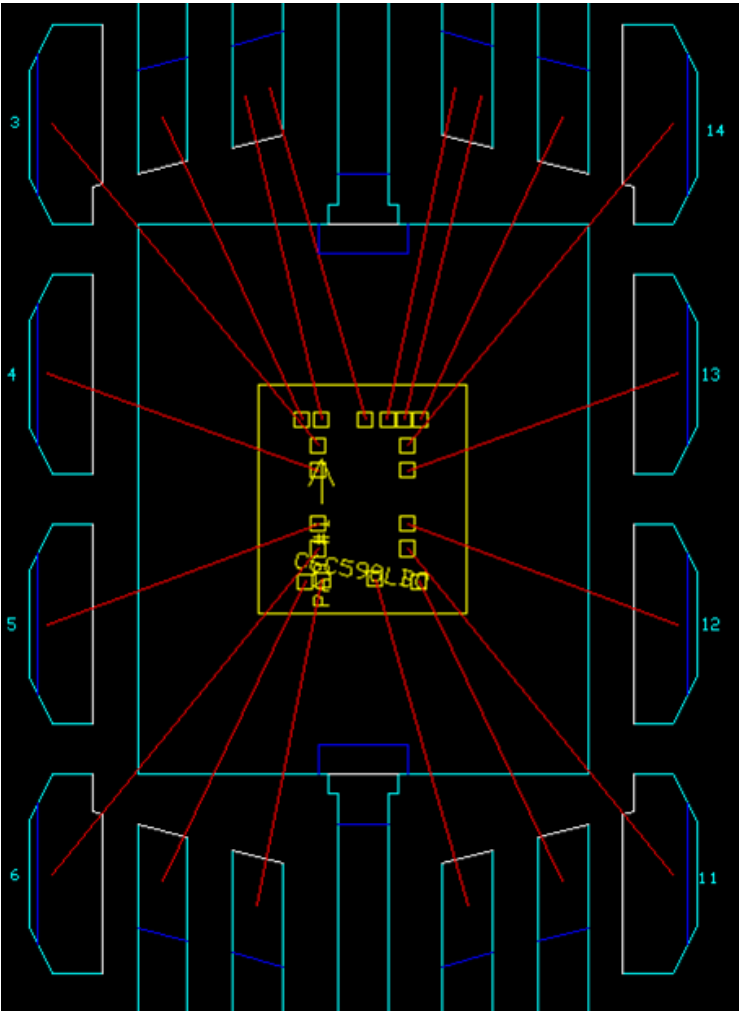
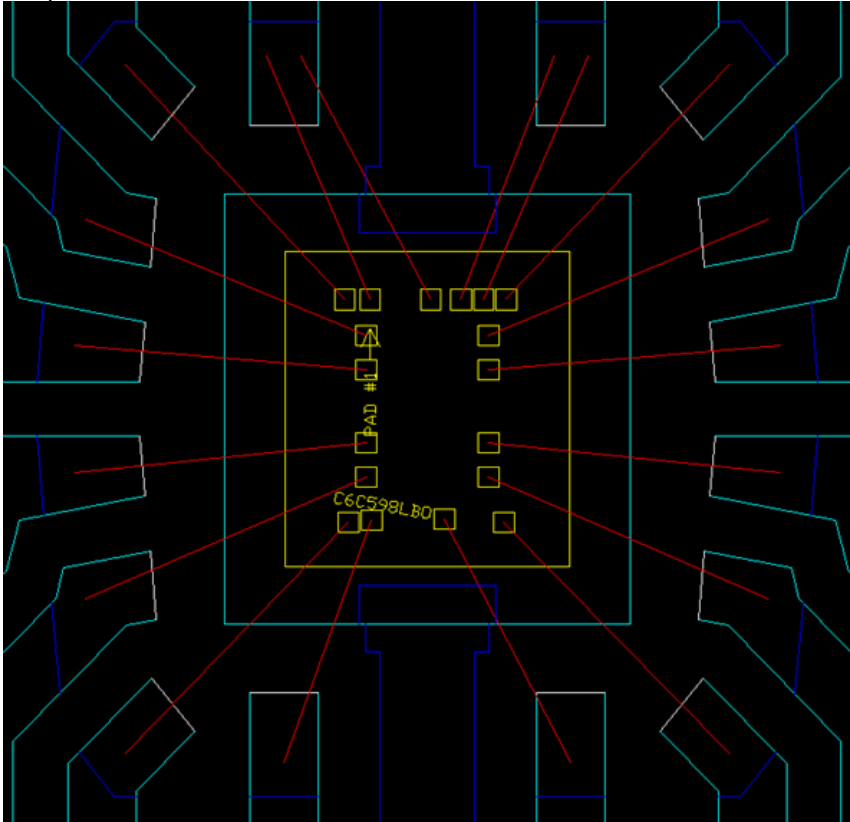


PCN Number:	20140117001		PCN Date:	01/28/2014	
Title:	TLC6C598QDRQ1 leadframe - CMS C1309141				
Customer Contact:	PCN_ww_admin_team@list.ti.com		Phone:	+1(214)480-6037	
Dept:	Quality Services				
Proposed 1st Ship Date:	07/28/2014		Estimated Sample Availability:	Upon request	
Change Type:					
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Assembly Materials
<input type="checkbox"/>	Design	<input type="checkbox"/>	Electrical Specification	<input type="checkbox"/>	Mechanical Specification
<input type="checkbox"/>	Test Site	<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>	Wafer Bump Site	<input type="checkbox"/>	Wafer Bump Material	<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>	Wafer Fab Site	<input type="checkbox"/>	Wafer Fab Materials	<input type="checkbox"/>	Wafer Fab Process
<input type="checkbox"/>	Part number change				
PCN Details					
Description of Change:					
Change the internal leadframe configuration.					
Reason for Change:					
The current leadframe configuration allows internal bond wire spacing less than 1 wire diameter. Extracts from the current and proposed bond diagrams are shown below. Please note the improved spacing of the red bond wires in the proposed view.					
Current:					
 <p>The diagram shows a central chip labeled 'TLC6C598L20' with a yellow square highlighting its internal bond wires. Red lines represent bond wires connecting the chip to lead positions 3 through 14. The spacing between these red bond wires is relatively narrow. The leads are numbered 3, 4, 5, 6 on the left and 11, 12, 13, 14 on the right. The chip is mounted on a leadframe with various mechanical features.</p>					

Proposed:



Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

Positive impact. The improved spacing reduces the possibilities of shorted wires.

Changes to product identification resulting from this PCN:

None

Product Affected:

TLC6C598QDRQ1

Qualification Data:

Automotive New Product Qualification Plan/Summary

(As per AEC-Q100 and JEDEC Guidelines)

Supplier Name:	Texas Instruments Inc.	Supplier Wafer Fabrication Site:	TI Dallas - DMOS5
Supplier Code:		Supplier Die Rev.	B
Supplier Part Number:	TLC6C598QDRQ1	Supplier Assembly/Test Site:	TI Malaysia
Customer Name:		Supplier Package/Pin:	D/16
Customer Part Number:		Pb-Free Lead Frame (Y/N):	Y
Device Description:		"Green" Mold Compound (Y/N):	Y
MSL Rating:	Level3-260C	Operating Temp Range:	-40 to +125C
Peak Solder Reflow Temp:	260C	Automotive Grade Level (1):	1
Prepared by:	Larry Ting	Date:	01/16/2014
Supplier Name:	Texas Instruments Inc.	Supplier Wafer Fabrication Site:	TI Dallas - DMOS5

Test	#	Reference	Test Conditions	Min Lots (2)	SS / lot (2)	Min Total (2)	Results Lot/pass /fail	Comments: (N/A =Not Applicable)	Exceptions to AEC - Q100
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TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS (3)

PC	A1	JESD22-113 J-STD-020	Preconditioning: SMD only; Moisture Preconditioning for THB/HAST, AC/UHST, TC, HTSL, and HTOL	Performed on <u>ALL</u> SMD devices prior to THB/HAST, AC/UHST, TC and PTC					
THB or HAST	A2	JESD22-A101 JESD22-A110	Temperature Humidity Bias: 85°C/85%/1000 hours Highly Accelerated Stress Test: 130°C/85%/96 hours or 110°C/85%/264 hours	3	77	231	Pass	QBS to current leadframe	
AC or UHST	A3	JESD22-A102 JESD22-A118	Autoclave: 121°C/15 psig/96 hours Unbiased Highly Accelerated Stress Test: 130°C/85%/96 hours or 110°C/85%/264 hours	3	77	231	Pass	QBS to current leadframe	
TC	A4	JESD22-A104	Temperature Cycle: -65°C/+150°C/500 cycles	3	77	231	Pass	QBS to current leadframe	
PTC	A5	JESD22-A105	Power Temperature Cycling: -40°C/+125°C/1000 cycles	1	45	45	Pass	N/A	
HTSL	A6	JESD22-A103	High Temperature Storage Life: 150°C/1000 hours or 175°C/500 hours	1	45	45	Pass	QBS to current leadframe	

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS (3)

HTOL	B1	JESD22-A108	High Temp Operating Life: 125°C/1000 hours 150°C/408 hours	3	77	231	Pass	QBS to current leadframe	
ELFR	B2	AEC-Q100-008	Early Life Failure Rate:	3	800	2400	Pass	QBS to current leadframe	

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS (3)

WBS	C1	AEC-Q100-001	Wire Bond Shear Test: (Cpk > 1.67)	30 bonds	5 parts min.	30 bonds	Pass		
WBP	C2	Mil-Std-883 Method 2011	Wire Bond Pull: Each bonder used (Cpk > 1.67)	30 bonds	5 parts min.	30 bonds	Pass		
SD	C3	JESD22-B102	Solderability: (>95% coverage) 8 hr steam age (1 hour for Au-plated leads)	1	15	15		N/A	
PD	C4	JESD22-B100 JESD22-B108	Physical Dimensions: (Cpk > 1.67)	1	10	10	Pass		
SBS	C5	AEC-Q100-010	Solder Ball Shear: (Cpk > 1.67)	5 balls	10 parts min.	50	Pass		
LI	C6	JESD22-B105	Lead Integrity:	10 leads	5 parts min.	50		N/A	

TEST GROUP E- ELECTRICAL VERIFICATION

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test:	All	All	All			
HBM	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model: (2kV - H2 or better)	1				N/A	
MM	E2	AEC-Q100-003	Electrostatic Discharge, Machine Model: (200V – M3 or better)	1				N/A	
CDM	E3	AEC-Q100-101	Electrostatic Discharge, Charged Device Model: (750V corner leads, 500V for all other pins)	1				N/A	
LU	E4	AEC-Q100-004	Latch-Up:	1	6	6		N/A	
ED	E5	AEC-Q100-009	Electrical Distributions: (Cpk > 1.67)	1	30	30	1/30/0		

- (1) Grade 0 (or A): -40°C to +150°C ambient operating temperature range
 Grade 1 (or Q): -40°C to +125°C ambient operating temperature range
 Grade 2 (or T): -40°C to +105°C ambient operating temperature range
 Grade 3 (or I): -40°C to +85°C ambient operating temperature range
 Grade 4 (or C): -0°C to +150°C ambient operating temperature range
- (2) These are recommended minimum lot/sample sizes. Lot/sample size may be reduced depending on available data.
- (3) Generic data may be used.

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Reliability data shows characteristic failure mechanisms of the specific environmental stress as documented in the industry standards for each stress condition.

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