RF Power LDMOS Transistor

N–Channel Enhancement–Mode Lateral MOSFET

This 56 W RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1805 to 1880 MHz.

1800 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 1600 mA, P_{out} = 56 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

| Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	18.6	31.9	7.1	−35.1	−11
1840 MHz	19.1	32.1	7.2	−34.4	−21
1880 MHz	19.3	33.1	7.2	−34.4	−15

Features

- Designed for wide instantaneous bandwidth applications
- Greater negative gate–source voltage range for improved Class C operation
- Able to withstand extremely high output VSWR and broadband operating conditions
- Optimized for Doherty applications

✓RoHS

A2T18S262W12NR3

1805–1880 MHz, 56 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR
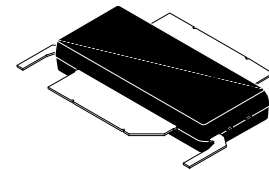
OM-880X-2L2L PLASTIC
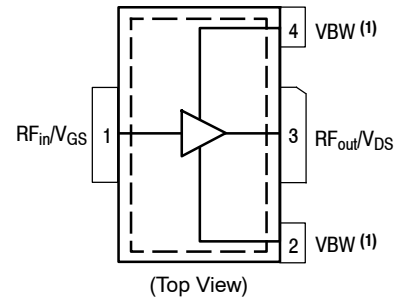
Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

1. Device can operate with V_{DD} current supplied through pin 2 and pin 4.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	−0.5, +65	Vdc
Gate–Source Voltage	V_{GS}	−6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Case Operating Temperature Range	T_C	−40 to +150	°C
Operating Junction Temperature Range [1,2]	T_J	−40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case Case Temperature 72°C, 56 W CW, 28 Vdc, I_{DQ} = 1600 mA, 1840 MHz	$R_{\theta JC}$	0.23	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	2
Charge Device Model (per JESD22–C101)	C3

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 320 μAdc)	$V_{GS(th)}$	1.4	1.8	2.2	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1600 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.6	3.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3.2 Adc)	$V_{DS(on)}$	0.05	0.14	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

(continued)

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Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

| Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1] (In NXP Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1600 mA, P_{out} = 56 W Avg., f = 1880 MHz, Single−Carrier W−CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	18.0	19.3	20.5	dB
Drain Efficiency	η_D	31.5	33.1	—	%
Output Peak−to−Average Ratio @ 0.01% Probability on CCDF	PAR	6.5	7.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	−34.4	−31.5	dBc
Input Return Loss	IRL	—	−15	−8	dB
Load Mismatch (In NXP Test Fixture, 50 ohm system) I_{DQ} = 1600 mA, f = 1840 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 32 Vdc, 347 W Pulsed CW Output Power (3 dB Input Overdrive from 288 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (In NXP Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1600 mA, 1805−1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, Pulsed CW	P1dB	—	231	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805−1880 MHz frequency range.)	Φ	—	−18	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	110	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 56 W Avg.	G_F	—	0.7	—	dB
Gain Variation over Temperature (−30°C to +85°C)	ΔG	—	0.011	—	dB/°C
Output Power Variation over Temperature (−30°C to +85°C)	$\Delta P1dB$	—	0.006	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2T18S262W12NR3	R3 Suffix = 250 Units, 56 mm Tape Width, 13−inch Reel	OM−880X−2L2L

1. Part internally matched both on input and output.
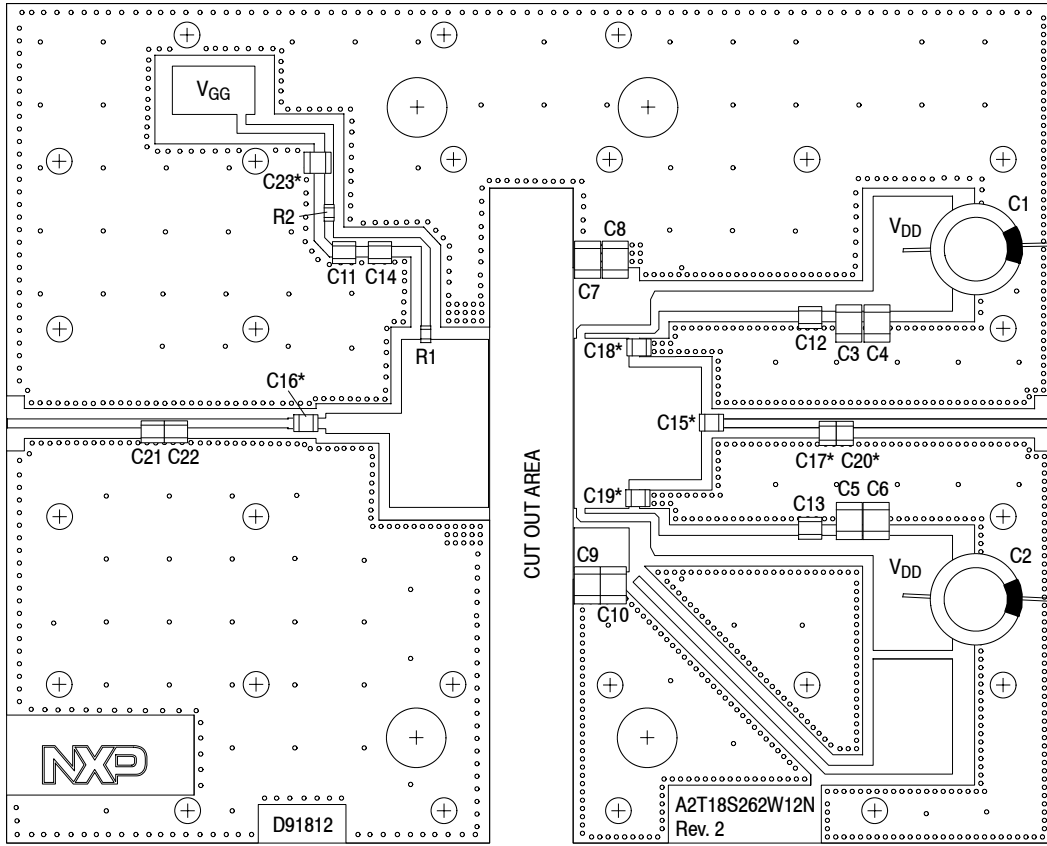
A2T18S262W12NR3

*C15, C16, C17, C18, C19, C20 and C23 are mounted vertically.

Figure 2. A2T18S262W12NR3 Test Circuit Component Layout

Table 7. A2T18S262W12NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
C3, C4, C5, C6, C7, C8, C9, C10	4.7 μF Chip Capacitor	C4532X7S2A475M230KB	TDK
C11	470 pF Chip Capacitor	ATC100B471JT200XT	ATC
C12, C13, C14, C15, C16	10 pF Chip Capacitor	ATC100B100JT500XT	ATC
C17, C18, C19	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C20	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C21	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
C22	0.1 pF Chip Capacitor	ATC100B0R1BT500XT	ATC
C23	10 μF Chip Capacitor	GRM32ER61H106KA12L	Murata
R1	2.2 Ω, 1/8 W Chip Resistor	CRCW08052R20JNEA	Vishay
R2	1 kΩ, 1/10 W Chip Resistor	RR1220P-102-D	Susumu
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D91812	MTL

TYPICAL CHARACTERISTICS — 1805–1880 MHz
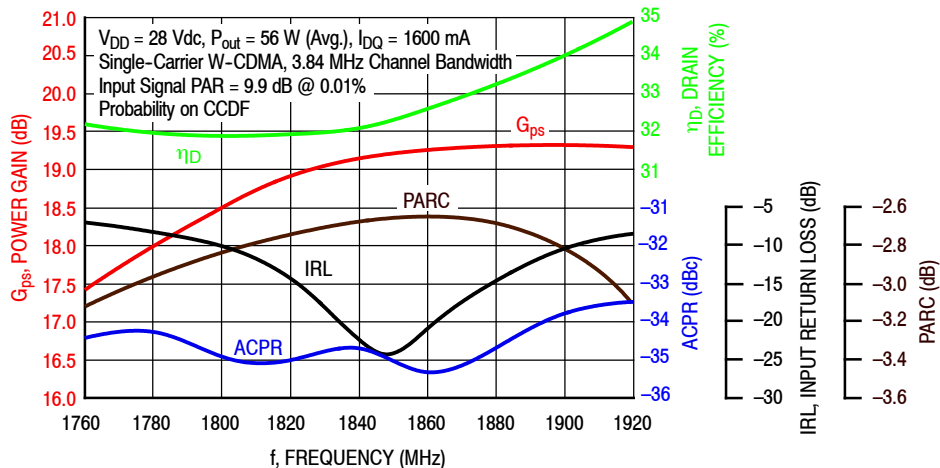
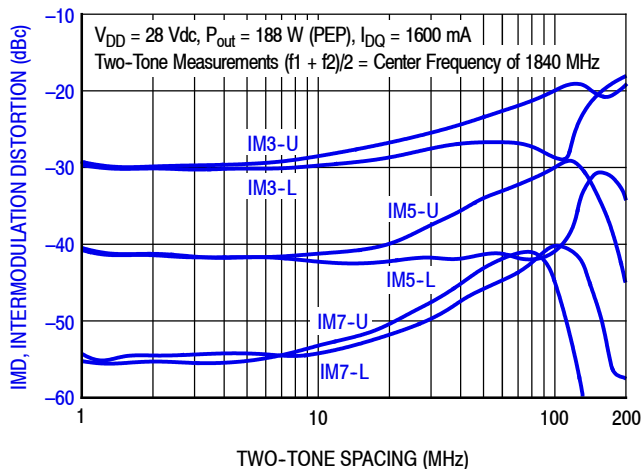**Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_out = 56 Watts Avg.**

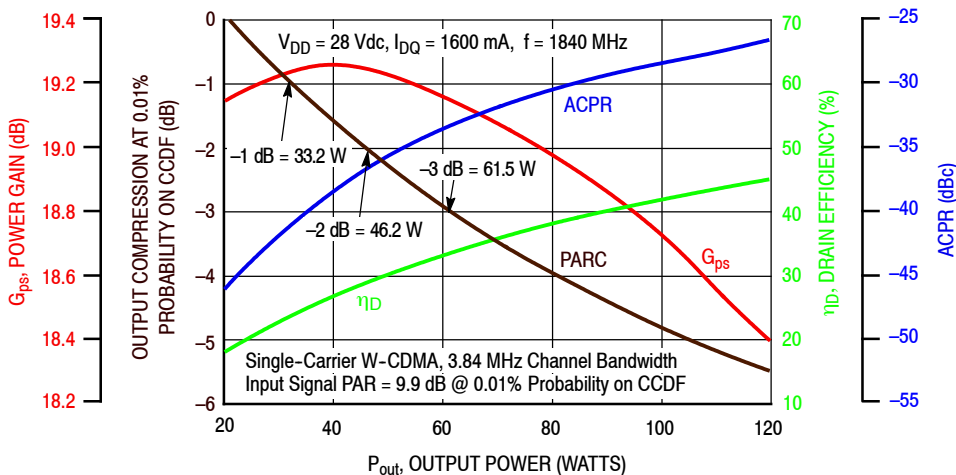**Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing**

Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

A2T18S262W12NR3

TYPICAL CHARACTERISTICS — 1805–1880 MHz
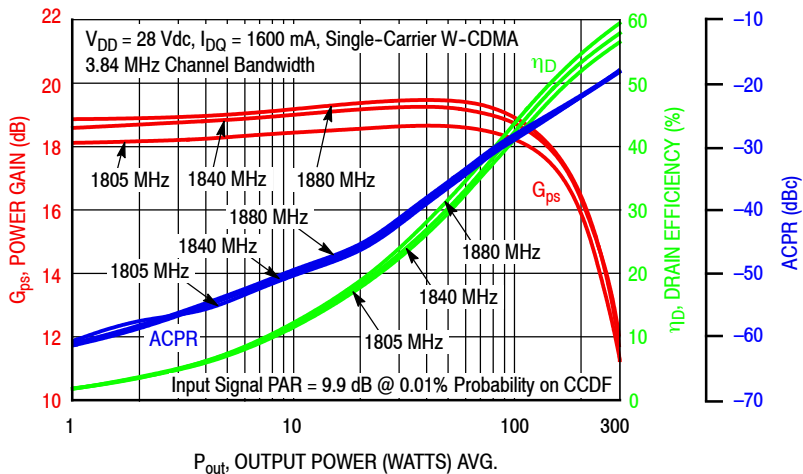
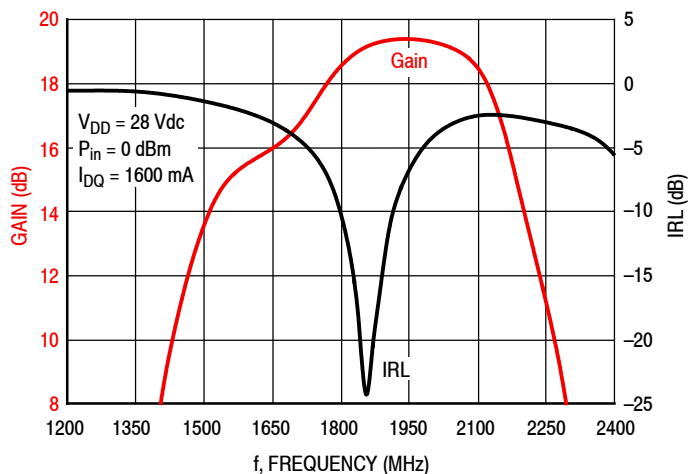Figure 6. Single–Carrier W–CDMA Power Gain, Drain
Efficiency and ACPR versus Output Power

Figure 7. Broadband Frequency Response

Table 8. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1600 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} [1] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.03 − j3.40	1.13 + j3.70	0.65 − j3.47	17.5	55.2	328	58.3	−11
1840	1.15 − j4.27	1.50 + j4.04	0.68 − j3.23	17.8	55.0	318	60.8	−14
1880	1.21 − j4.87	2.03 + j4.55	0.58 − j3.29	17.3	55.1	320	58.3	−16

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} [2] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.03 − j3.40	1.04 + j3.84	0.65 − j3.53	15.4	55.9	388	59.8	−17
1840	1.15 − j4.27	1.36 + j4.24	0.68 − j3.28	15.7	55.7	373	61.5	−20
1880	1.21 − j4.87	1.91 + j4.86	0.59 − j3.36	15.1	55.8	379	58.6	−22

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1600 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} [1] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.03 − j3.40	1.04 + j3.77	1.26 − j2.72	20.2	53.0	198	70.4	−20
1840	1.15 − j4.27	1.36 + j4.16	1.03 − j2.37	20.2	52.7	188	69.2	−25
1880	1.21 − j4.87	1.91 + j4.66	1.03 − j2.60	20.1	52.7	188	67.4	−24

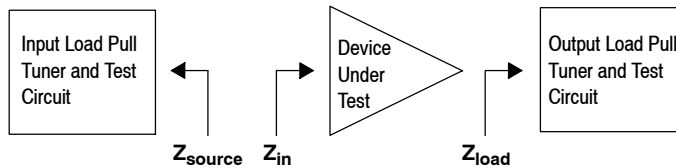| f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} [2] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.03 − j3.40	0.95 + j3.86	0.99 − j2.98	17.5	54.6	287	71.2	−26
1840	1.15 − j4.27	1.24 + j4.30	1.01 − j2.41	18.1	53.3	216	69.2	−34
1880	1.21 − j4.87	1.80 + j4.91	1.01 − j2.71	17.8	53.8	238	67.9	−32

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Input Load Pull Tuner and Test Circuit ← → Device Under Test → Output Load Pull Tuner and Test Circuit

Z_{source} Z_{in} Z_{load}

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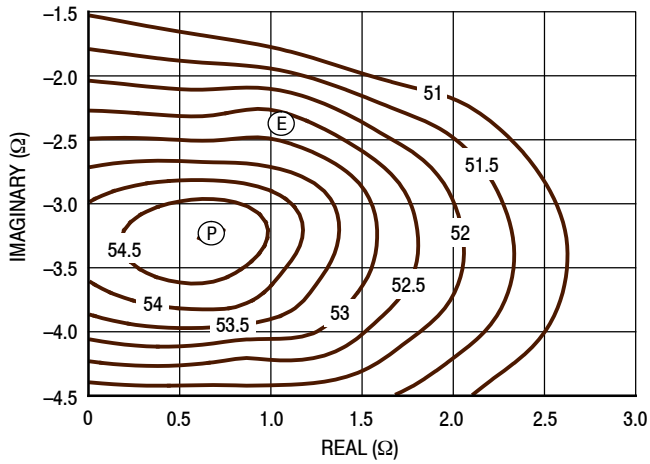## P1dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

Figure 8. P1dB Load Pull Output Power Contours (dBm)
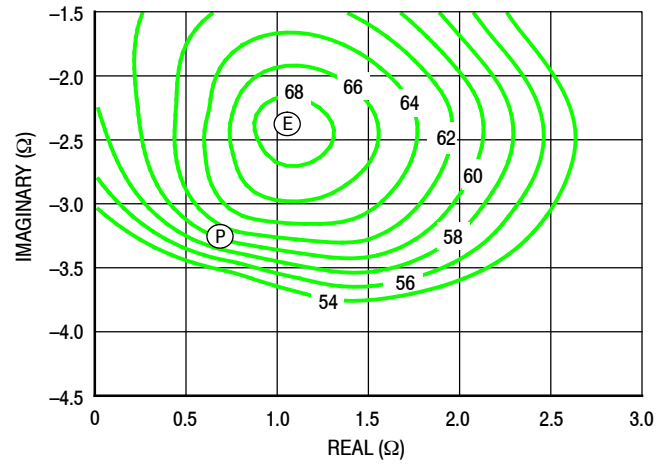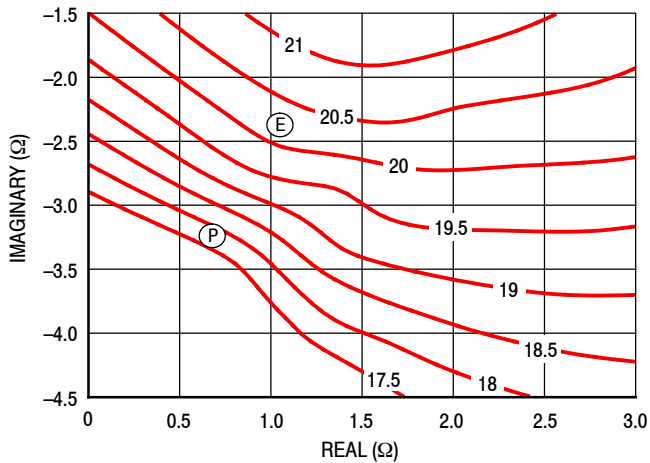

Figure 9. P1dB Load Pull Efficiency Contours (%)
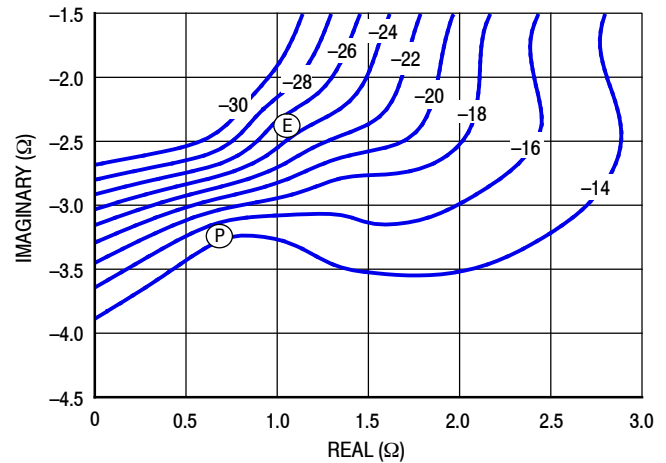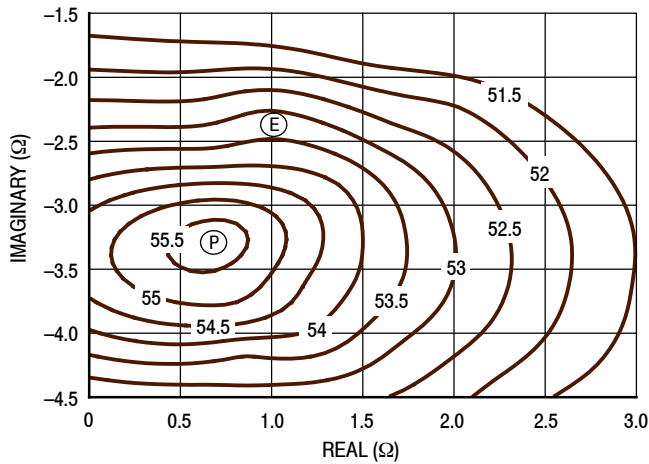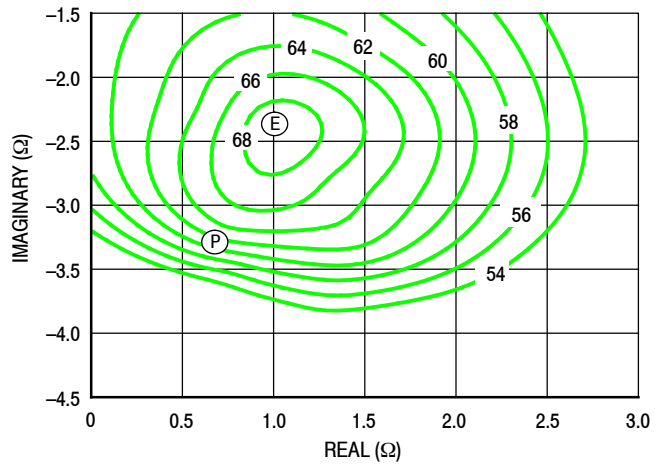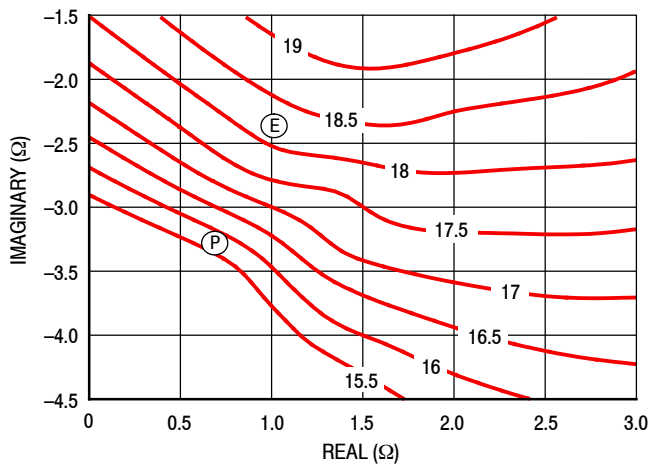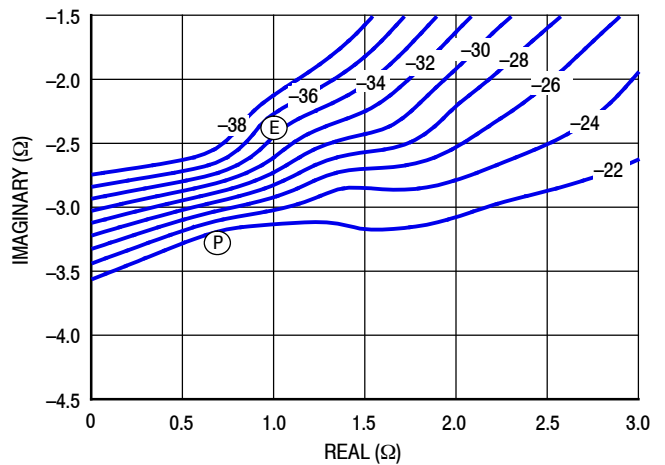

Figure 10. P1dB Load Pull Gain Contours (dB)

Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

— Gain
— Drain Efficiency
— Linearity
— Output Power

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Figure 12. P3dB Load Pull Output Power Contours (dBm)

Figure 13. P3dB Load Pull Efficiency Contours (%)

Figure 14. P3dB Load Pull Gain Contours (dB)
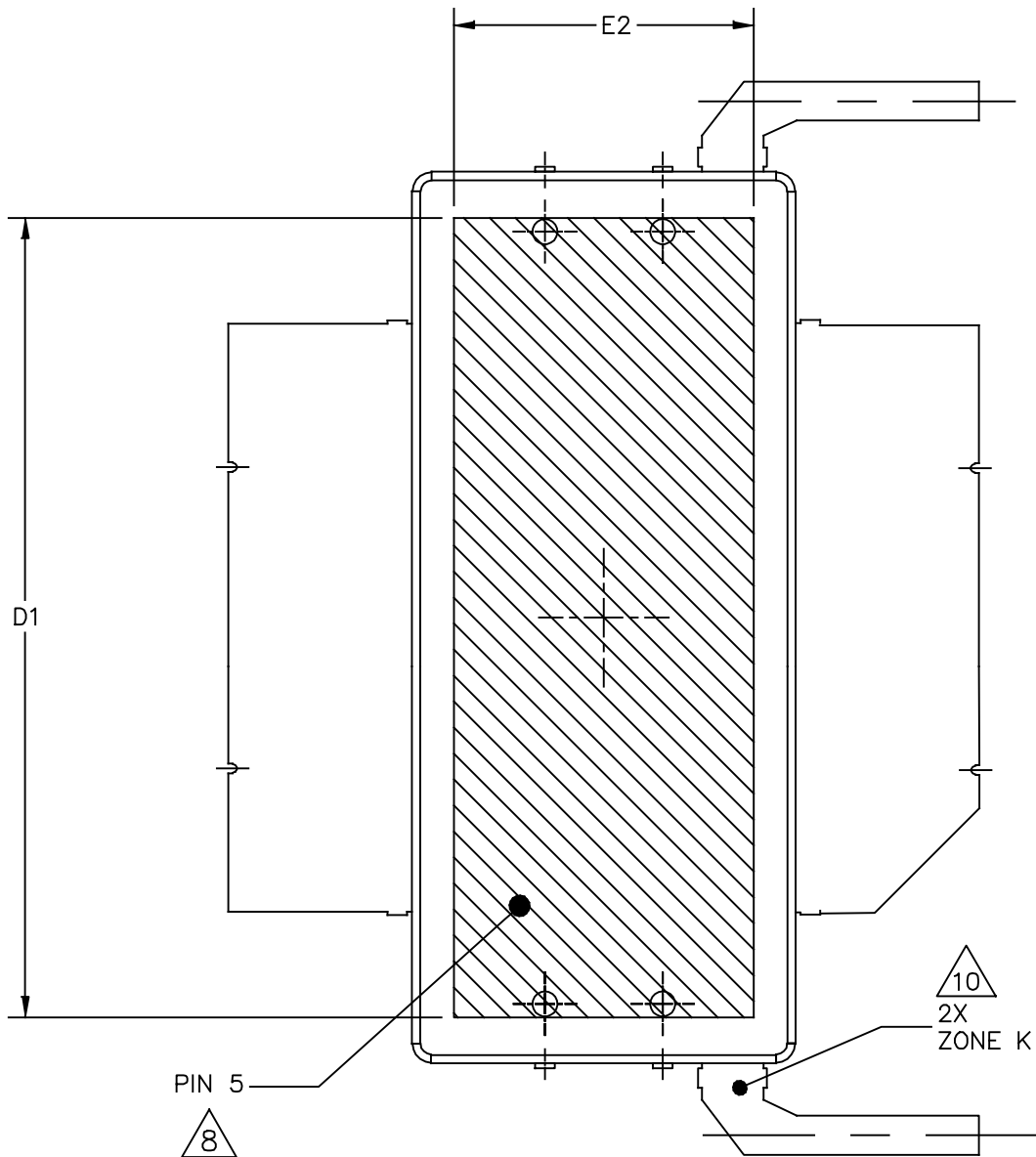
Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS
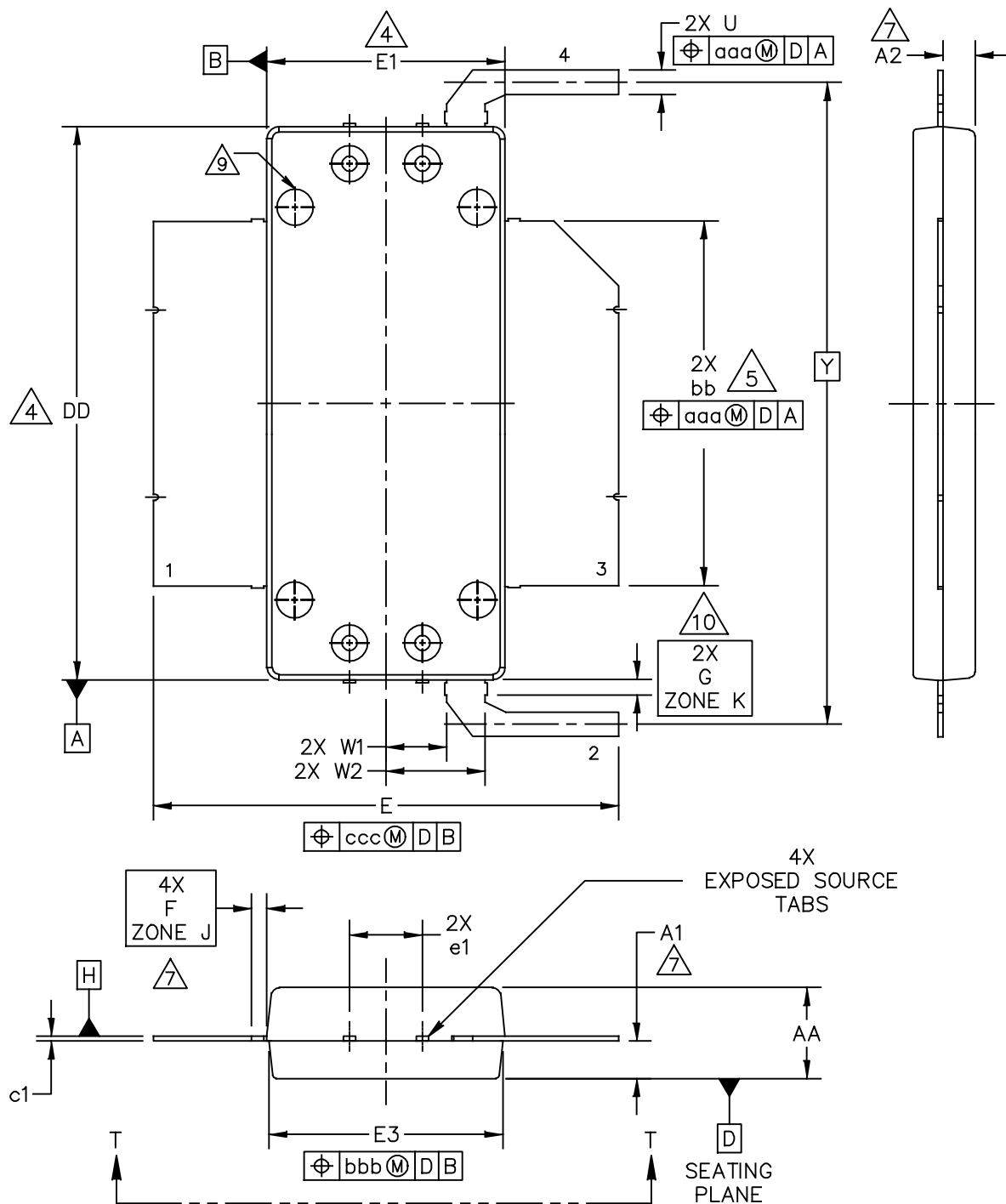
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	STANDARD: NON−JEDEC	
	SOT1817−1	09 FEB 2016

BOTTOM VIEW
VIEW T—T

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	STANDARD: NON—JEDEC		
	SOT1817—1		09 FEB 2016

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD
   WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

△4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION
   IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD
   MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
   PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION
   AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

△7. DIMENSIONS A1 AND A2 APPLIES WITHIN ZONE J ONLY. A1 APPLIES TO PINS 1 AND 3.
   A2 APPLIES TO PINS 2 AND 4.

△8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1
   AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES
   OF EXPOSED AREA OF HEAT SLUG.

△9. DIMPLED HOLE REPRESENTS INPUT SIDE.

△10. ZONE K REPRESENTS NON-SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED
   ARE PERMITTED ON BOTH SIDES OF THE LEADS.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.148	.152	3.76	3.86	W1	.095	.105	2.41	2.67
A1	.059	.065	1.50	1.65	W2	.158	.168	4.01	4.27
A2	.056	.068	1.42	1.73	U	.037	.043	0.94	1.09
DD	.908	.912	23.06	23.16	Y	1.056 BSC		26.82 BSC	
D1	.816	----	20.73	----	bb	.597	.603	15.16	15.32
E	.762	.770	19.35	19.56	c1	.007	.011	0.18	0.28
E1	.390	.394	9.91	10.01	e1	.116	.124	2.95	3.15
E2	.306	----	7.77	----					
E3	.383	.387	9.73	9.83	aaa	.004		0.10	
F	.025 BSC		0.64 BSC		bbb	.006		0.15	
G	.030 BSC		0.76 BSC		ccc	.010		0.25	

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OM-880X-2L2L	STANDARD: NON-JEDEC
	SOT1817-1 09 FEB 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes
- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over–Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins
- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software
- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools
- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:
1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2017	• Initial release of data sheet

A2T18S262W12NR3