CHANGE NOTIFICATION

Linear Technology Corporation
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April 01, 2014

Dear Sir/Madam: PCN# 040114

Subject: Notification of Change to LTC2480 Datasheet

Please be advised that Linear Technology Corporation has made a change to the LTC2480 specification in order to improve device manufacturability. The Maximum External Oscillator Frequency (f_{EOSC}) in the Timing Characteristics is being reduced from 4000kHz to 1000kHz . This is also noted in the text and in the graphs of performance vs. sample rate in Figures 20 to 27 of the attached datasheet. Performance degrades at high sample rates as shown in the figures, and an external oscillator frequency of 1000kHz is a more conservative maximum. No changes are being made to the circuit or the test methodology. Product shipped after June 2, 2014 will be tested to the new limit.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by email at JASON.HU@LINEAR.COM. If I do not hear from you by June 2, 2014, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

ANALOG INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 10)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, f_O, SDI				10		pF
C_{IN}	Digital Input Capacitance SCK				10		pF
V_{OH}	High Level Output Voltage SDO	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SDO	I_O = 1.6mA	●			0.4	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage SDO		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	Conversion Mode (Note 12)	●		160	250	µA
		Sleep Mode (Note 12)	●		1	2	µA
		H-Grade	●			20	µA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 15)	●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode	●	157.2	160.3	163.5	ms
		50Hz Mode (H-Grade)	●	157.2	160.3	165.1	ms
		60Hz Mode	●	131.0	133.6	136.3	ms
		60Hz Mode (H-Grade)	●	131.0	133.6	137.6	ms
		Simultaneous 50Hz/60Hz Mode	●	144.1	146.9	149.9	ms
		Simultaneous 50Hz/60Hz Mode (H-Grade)	●	144.1	146.9	151.0	ms
		External Oscillator	●		41036/f_{EOSC} (in kHz)		ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode	●	78.7	80.3	81.9	ms
		50Hz Mode (H-Grade)	●			82.7	ms
		60Hz Mode	●	65.6	66.9	68.2	ms
		60Hz Mode (H-Grade)	●			68.9	ms
		Simultaneous 50Hz/60Hz Mode	●	72.2	73.6	75.1	ms
		Simultaneous 50Hz/60Hz Mode (H-Grade)	●			75.6	ms
		External Oscillator	●		20556/f_{EOSC} (in kHz)		ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10)			38.4		kHz
		External Oscillator (Notes 10, 11)			f_{EOSC}/8		kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 10)	●			4000	kHz

APPLICATIONS INFORMATION

internal oscillator and 50Hz mode, the extra gain error is 0.061ppm. If an external clock is used, the corresponding extra gain error is 0.24 • 10–6 • f_{EOSC}ppm.

The magnitude of the dynamic reference current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typically better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by V_{REF}^+ and GND, the expected drift of the dynamic current gain error will be insignificant (about 1% of its value over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

In addition to the reference sampling charge, the reference pins ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a small gain error. A 100Ω source resistance will create a 0.05µV typical and 0.5µV maximum full-scale error.

Output Data Rate

When using its internal oscillator, the LTC2480 produces up to 7.5 samples per second (sps) with a notch frequency of 60Hz, 6.25sps with a notch frequency of 50Hz and 6.82sps with the 50Hz/60Hz rejection mode. The actual output data rate will depend upon the length of the sleep and data output phases which are controlled by the user and which can be made insignificantly short. When operated with an external conversion clock (f_O connected to an external oscillator), the LTC2480 output data rate can be increased as desired. The duration of the conversion phase is 41036/f_{EOSC}. If f_{EOSC} = 307.2kHz, the converter behaves as if the internal oscillator is used and the notch is set at 60Hz.

An increase in f_{EOSC} over the nominal 307.2kHz will translate into a proportional increase in the maximum output data rate. The increase in output rate is nevertheless accompanied by three potential effects, which must be carefully considered.

First, a change in f_{EOSC} will result in a proportional change in the internal notch position and in a reduction of the converter differential mode rejection at the power line fre-

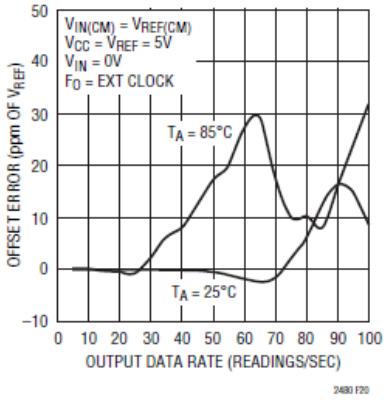

Figure 20. Offset Error vs Output Data Rate and Temperature

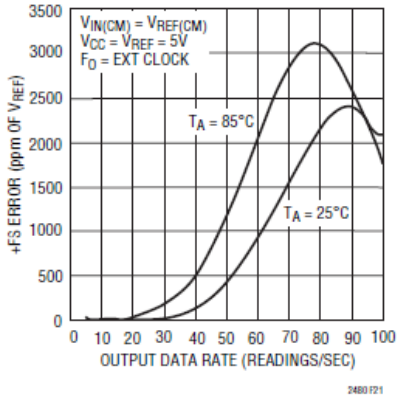

Figure 21. +FS Error vs Output Data Rate and Temperature

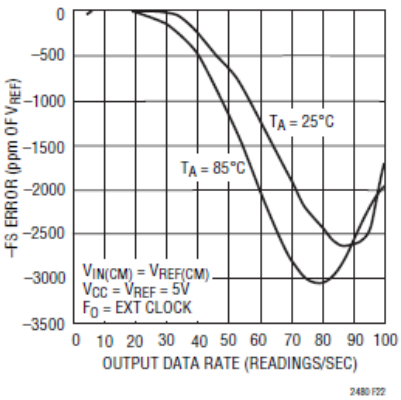

Figure 22. –FS Error vs Output Data Rate and Temperature

APPLICATIONS INFORMATION

quency. In many applications, the subsequent performance degradation can be substantially reduced by relying upon the LTC2480's exceptional common mode rejection and by carefully eliminating common mode to differential mode conversion sources in the input circuit. The user should avoid single-ended input filters and should maintain a very high degree of matching and symmetry in the circuits driving the IN^+ and IN^- pins.

Second, the increase in clock frequency will increase proportionally the amount of sampling charge transferred through the input and the reference pins. If large external input and/or reference capacitors (C_{IN}, C_{REF}) are used, the previous section provides formulae for evaluating the effect of the source resistance upon the converter performance for any value of f_{EOSC}. If small external input and/or reference capacitors (C_{IN}, C_{REF}) are used, the effect of the external source resistance upon the LTC2480 typical performance can be inferred from Figures 13, 14, 15 and 16 in which the horizontal axis is scaled by $307200/f_{EOSC}$.

Third, an increase in the frequency of the external oscillator above 1MHz (a more than 3× increase in the output data rate) will start to decrease the effectiveness of the internal autocalibration circuits. This will result in a progressive degradation in the converter accuracy and linearity. Typical measured performance curves for output data rates up to 100 readings per second are shown in Figures 20 to 27. In order to obtain the highest possible level of accuracy from this converter at output data rates above 20 readings per

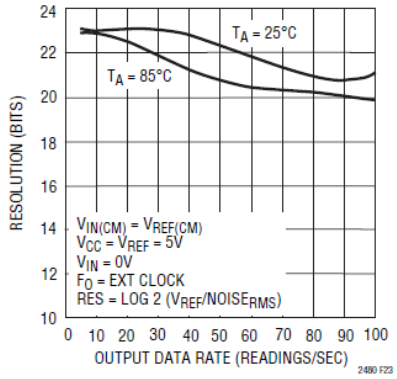

Figure 23. Resolution ($Noise_{RMS}$ ≤ 1LSB) vs Output Data Rate and Temperature

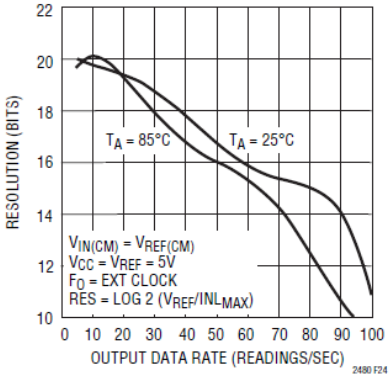

Figure 24. Resolution (INL_{MAX} ≤ 1LSB) vs Output Data Rate and Temperature

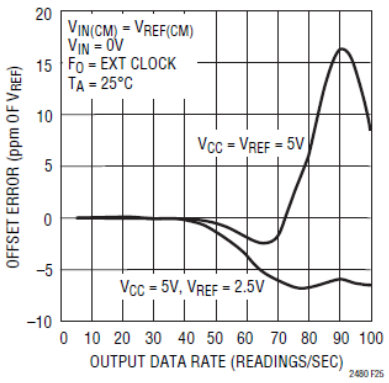

Figure 25. Offset Error vs Output Data Rate and Reference Voltage

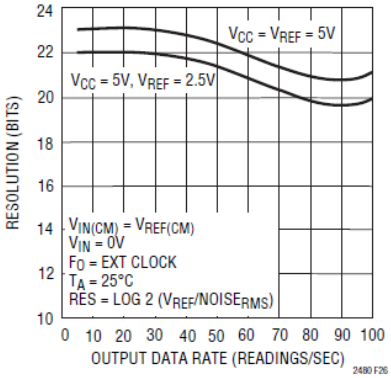

Figure 26. Resolution ($Noise_{RMS}$ ≤ 1LSB) vs Output Data Rate and Reference Voltage

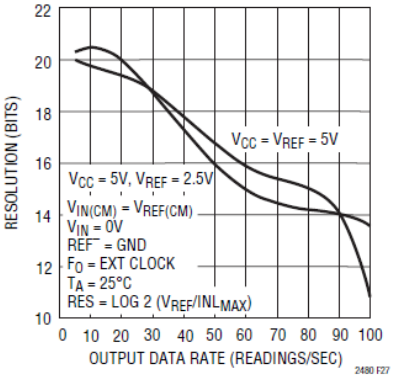

Figure 27. Resolution (INL_{MAX} ≤ 1LSB) vs Output Data Rate and Reference Voltage