TRF37x32 Dual Down Converter Mixer With Integrated IF AMP

1 Features

- Device Family Supports Wide RF Input Range
  - TRF37A32: 400 - 1700 MHz
  - TRF37B32: 700 - 2700 MHz
  - TRF37C32: 1700 - 3800 MHz
- Gain: 10 dB
- Noise Figure: 9.5 dB
- Input IP3: 30 dBm
- 500 mW per Channel Power Dissipation
- Single Ended RF Input
- IF Frequency Range from 30 MHz to 600 MHz
- 45 dB Isolation between Channels
- Low Power Mode Option
- Independent Power Down Control
- Single 3.3V Supply
- No External Matching Required

2 Applications

- Wireless Infrastructure
  - WCDMA, TD-SCDMA
  - LTE, TD-LTE
  - Multicarrier GSM (MC-GSM)
- Point-to-Point Microwave
- Software Defined Radios (SDR)
- Radar Receiver
- Satellite Communications

3 Description

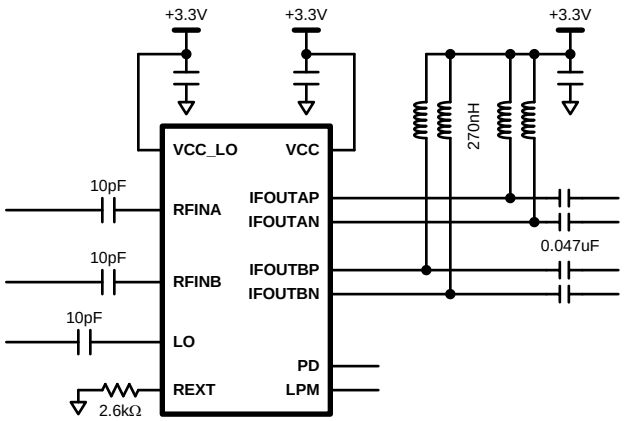
The TRF37x32 is a wideband dual down converter mixer with integrated IF amplifier. The device employs integrated baluns for single ended RF and LO inputs. The IF amplifier operates from 30 MHz to 600 MHz in an open collector topology to support a variety of IF frequencies and bandwidths. The TRF37x32 provides excellent mixer linearity and noise performance and offers good isolation between channels for operation with diversity applications. The device operates with low power dissipation and further provides an option for a low power mode for power sensitive applications. Each channel can be independently powered down with fast response times to allow operation in time domain duplexed (TDD) applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRF37A32	WQFN (32)	5.00mm x 5.00mm
TRF37B32		
TRF37C32		

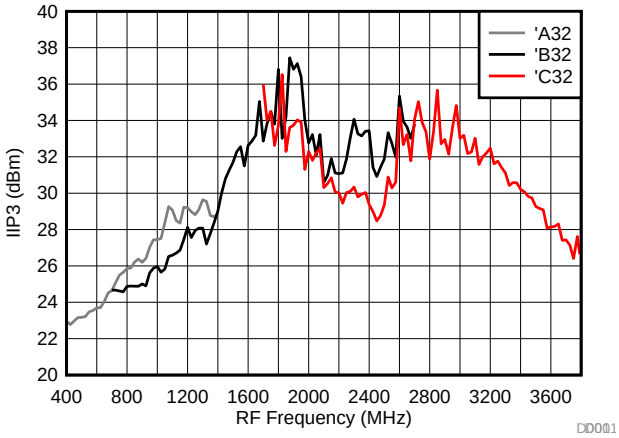
(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



TRF37A/B/C32

IIP3 Performance Across Frequency



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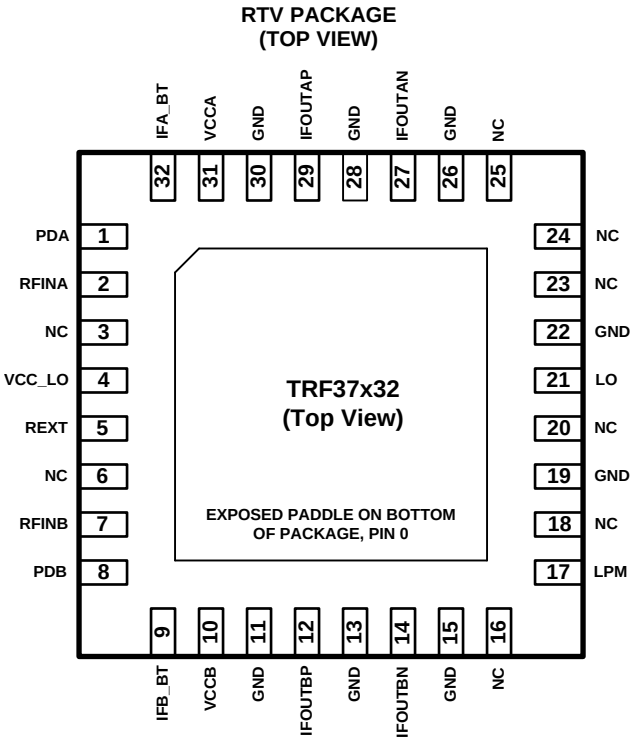
5 Revision History

Changes from Original (May 2014) to Revision A **Page**

- Added Typical Characteristics, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, and Layout section ... 1
- Replaced the *Handling Ratings* table with the *ESD Ratings* table ... 5

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
PDA	1	Digital Input	Power down for channel A (1 = PD; 0 or open = powered)
RFINA	2	Analog Input	RF input for channel A
NC	3	N/A	No connect
VCC_LO	4	Supply	V_{CC} supply for the LO circuitry
REXT	5	Bias	External bias resistor
NC	6	N/A	No connect
RFINB	7	Analog Input	RF input for channel B
PDB	8	Digital Input	Power down for channel B (1 = PD; 0 or open = powered)
IFB_BT	9	N/A	IF channel B bias control; leave unconnected
VCCB	10	Supply	Power supply for channel B
GND	11	Ground	Ground
IFOUTBP	12	Analog Output	IF out channel B: positive
GND	13	Ground	Ground
IFOUTBN	14	Analog Output	IF out channel B: negative
GND	15	Ground	Ground
NC	16	N/A	No connect
LPM	17	Digital Input	Low power mode (0 = normal; 1 = low power)
NC	18	N/A	No connect
GND	19	Ground	Ground
NC	20	N/A	No connect
LO	21	Analog Input	Local oscillator (LO) input

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	22	Ground	Ground
NC	23	N/A	No connect
NC	24	N/A	No connect
NC	25	N/A	No connect
GND	26	Ground	Ground
IFOUTAN	27	Analog Output	IF out channel A: negative
GND	28	Ground	Ground
IFOUTAP	29	Analog Output	IF out channel A: positive
GND	30	Ground	Ground
VCCA	31	Supply	Power supply for channel A
IFA_BT	32	N/A	IF channel A bias control; leave unconnected

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage		–0.3	3.6	V
Storage temperature, T_{STG}		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except XIFOUTAP, IFOUTAN, IFOUTBP, and IFOUTBN	±2500	V
		Pins XIFOUTAP, IFOUTAN, IFOUTBP, and IFOUTBN (2)	±100	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) High Linearity IFOUT pins are susceptible to low voltage HBM damage.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating virtual junction temperature range, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		RTV 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	19.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.9	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	5.9	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics, TRF37A32

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Parameters						
V_{CC}	Supply Voltage		3.15	3.3	3.45	V
I_{CC}	Supply Current	F_{LO} = 750 MHz		280		mA
P_{diss}	Total Power Dissipation	F_{LO} = 750 MHz		0.92		W
	Power Down Current				2	mA
RF Frequency Range						
F_{RF}	Frequency Range		400		1700	MHz
RF Specifications						
G	Gain	F_{RF} = 950 MHz (LSI)		9.6		dB
G_{var}	Gain Variation over Frequency	within any 200 MHz Band		0.5		dB
NF	SSB Noise Figure	F_{RF} = 950 MHz (LSI)		9.6		dB
	SSB Noise Figure with Blocker	5 dBm blocker signal Δf > 50 MHz		17		dB
IIP3	Input 3rd Order Intercept Point	F_{RF} = 950 MHz (LSI), $F_{spacing}$ = 20 MHz		26		dBm
OIP3	Output 3rd Order Intercept Point	F_{RF} = 950 MHz (LSI), $F_{spacing}$ = 20 MHz		35.6		dBm
OIP2	Output 2nd Order Intercept Point	F_{RF} = 950 MHz (LSI)		65		dBm
IP1dB	Input 1 dB Compression Point	F_{RF} = 950 MHz (LSI)		11		dBm
Z_{IN}	Input Impedance			50		Ω
RLi	Input Return Loss	F_{RF} = 800 - 1400 MHz (LSI)		15		dB
LO Input						
P_{LO}	LO Drive Level		–3	0	6	dBm
F_{LO}	LO Frequency Range		600		1400	MHz
Z_{IN}	Input Impedance			50		Ω
RLi	Input Return Loss	F_{RF} = 750 - 1150 MHz		15		dB
Low Power Mode: LPM = 1						
I_{CC}	Supply Current	F_{LO} = 750 MHz		200		mA
P_{diss}	Total Power Dissipation	F_{LO} = 750 MHz		0.66		W
G	Gain	F_{RF} = 950 MHz (LSI)		9.2		dB
NF	SSB Noise Figure	F_{RF} = 950 MHz (LSI)		9.6		dB
IIP3	Input 3rd Order Intercept Point	F_{RF} = 950 MHz (LSI), $F_{spacing}$ = 20 MHz		26		dBm
IP1dB	Input 1 dB Compression Point	F_{RF} = 950 MHz (LSI)		11		dBm
Isolation						
	Channel Isolation	Drive RFinA/B IFoutA/B-IFoutB/A F_{RF} = 950 MHz		50		dB
	RF to IF Isolation	F_{RF} = 950 MHz		20		dB
	LO to RF Leakage	P_{LO} = 0 dBm		–55		dBm
	LO to IF Leakage	P_{LO} = 0 dBm		–45		dBm
Spurious						
	2x2 Spurious Product	2RF - 2LO		65		dBc
	3x3 Spurious Product	3RF - 3LO		70		dBc
IF Output						
Z_L	Differential Output Impedance Load			200		Ω
F_{IF}	Frequency Range	1 dB corner frequency	30		600	MHz
	DC Bias Range	Externally supplied DC bias through RF choke		3.3		V

7.6 Electrical Characteristics, TRF37B32

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Parameters						
V_{CC}	Supply Voltage		3.15	3.3	3.45	V
I_{CC}	Supply Current	F_{LO} = 1750 MHz		305		mA
P_{diss}	Total Power Dissipation	F_{LO} = 1750 MHz		1		W
	Power Down Current				2	mA
RF Frequency Range						
F_{RF}	Frequency Range		700		2700	MHz
RF Specifications						
G	Gain	F_{RF} = 1950 MHz (LSI)		10		dB
G_{var}	Gain Variation over Frequency	within any 200 MHz Band		0.5		dB
NF	SSB Noise Figure	F_{RF} = 1950 MHz (LSI)		9.2		dB
	SSB Noise Figure with Blocker	5 dBm blocker signal Δf > 50 MHz		15.5		dB
IIP3	Input 3rd Order Intercept Point	F_{RF} = 1950 MHz (LSI), $F_{spacing}$ = 20 MHz		32		dBm
OIP3	Output 3rd Order Intercept Point	F_{RF} = 1950 MHz (LSI), $F_{spacing}$ = 20 MHz		42		dBm
OIP2	Output 2nd Order Intercept Point	F_{RF} = 1950 MHz (LSI)		70		dBm
IP1dB	Input 1 dB Compression Point	F_{RF} = 1950 MHz (LSI)		10.8		dBm
Z_{IN}	Input Impedance			50		Ω
RLi	Input Return Loss	F_{RF} = 1700 - 2700 MHz (LSI)		10		dB
LO Input						
P_{LO}	LO Drive Level		–3	0	6	dBm
F_{LO}	LO Frequency Range		500		2900	MHz
Z_{IN}	Input Impedance			50		Ω
RLi	Input Return Loss	F_{RF} = 1500 - 2450 MHz		15		dB
Low Power Mode: LPM = 1						
I_{CC}	Supply Current	F_{LO} = 1750 MHz		220		mA
P_{diss}	Total Power Dissipation	F_{LO} = 1750 MHz		0.73		W
G	Gain	F_{RF} = 1950 MHz (LSI)		9.2		dB
NF	SSB Noise Figure	F_{RF} = 1950 MHz (LSI)		9.2		dB
IIP3	Input 3rd Order Intercept Point	F_{RF} = 1950 MHz (LSI), $F_{spacing}$ = 20 MHz		23		dBm
IP1dB	Input 1 dB Compression Point	F_{RF} = 1950 MHz (LSI)		10.7		dBm
Isolation						
	Channel Isolation	Drive RFinA/B IFoutA/B-IFoutB/A F_{RF} = 1950 MHz		45		dB
	RF to IF Isolation	F_{RF} = 1950 MHz		22		dB
	LO to RF Leakage	P_{LO} = 0 dBm		–50		dBm
	LO to IF Leakage	P_{LO} = 0 dBm		–42		dBm
Spurious						
	2x2 Spurious Product	2RF - 2LO		70		dBc
	3x3 Spurious Product	3RF - 3LO		75		dBc
IF Output						
Z_L	Differential Output Impedance Load			200		Ω
F_{IF}	Frequency Range	1 dB corner frequency	30		600	MHz
	DC Bias Range	Externally supplied DC bias through RF choke		3.3		V

7.7 Electrical Characteristics, TRF37C32

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Parameters						
V_{CC}	Supply Voltage		3.15	3.3	3.45	V
I_{CC}	Supply Current	F_{LO} = 2300 MHz		325		mA
P_{diss}	Total Power Dissipation	F_{LO} = 2300 MHz		1.1		W
	Power Down Current				2	mA
RF Frequency Range						
F_{RF}	Frequency Range		1700		3800	MHz
RF Specifications						
G	Gain	F_{RF} = 2500 MHz (LSI)		9.8		dB
G_{var}	Gain Variation over Frequency	within any 200 MHz Band		0.5		dB
NF	SSB Noise Figure	F_{RF} = 2500 MHz (LSI)		9.9		dB
	SSB Noise Figure with Blocker	5 dBm blocker signal Δf > 50 MHz		17.5		dB
IIP3	Input 3rd Order Intercept Point	F_{RF} = 2500 MHz (LSI) $F_{spacing}$ = 20 MHz		29		dBm
OIP3	Output 3rd Order Intercept Point	F_{RF} = 2500 MHz (LSI) $F_{spacing}$ = 20 MHz		38.8		dBm
OIP2	Output 2nd Order Intercept Point	F_{RF} = 2500 MHz (LSI)		65		dBm
IP1dB	Input 1 dB Compression Point	F_{RF} = 2500 MHz (LSI)		11.5		dBm
Z_{IN}	Input Impedance			50		Ω
RLi	Input Return Loss			8		dB
LO Input						
P_{LO}	LO Drive Level		–3	0	6	dBm
F_{LO}	LO Frequency Range		1500		3600	MHz
Z_{IN}	Input Impedance			50		Ω
RLi	Input Return Loss	F_{RF} = 2800 - 3400 MHz		10		dB
Low Power Mode: LPM = 1						
I_{CC}	Supply Current	F_{LO} = 2300 MHz		230		mA
P_{diss}	Total Power Dissipation	F_{LO} = 2300 MHz		0.76		W
G	Gain	F_{RF} = 2500 MHz (LSI)		9.2		dB
NF	SSB Noise Figure	F_{RF} = 2500 MHz (LSI)		9.9		dB
IIP3	Input 3rd Order Intercept Point	F_{RF} = 2500 MHz (LSI), $F_{spacing}$ = 20 MHz		22		dBm
IP1dB	Input 1 dB Compression Point	F_{RF} = 2500 MHz (LSI)		11.5		dBm
Isolation						
	Channel Isolation	Drive RFinA/B IFoutA/B-IFoutB/A F_{RF} = 2500 MHz		48		dB
	RF to IF Isolation	F_{RF} = 2500 MHz		21		dB
	LO to RF Leakage	P_{LO} = 0 dBm		–55		dBm
	LO to IF Leakage	P_{LO} = 0 dBm		–45		dBm
Spurious						
	2x2 Spurious Product	2RF - 2LO		65		dBc
	3x3 Spurious Product	3RF - 3LO		70		dBc
IF Output						
Z_L	Differential Output Impedance Load			200		Ω
F_{IF}	Frequency Range	1 dB corner frequency	30		600	MHz
	DC Bias Range	Externally supplied DC bias through RF choke		3.3		V

7.8 Timing Requirements

			MIN	TYP	MAX	UNIT
Power Control						
P_D	Turn-on Time	P_D = low to 90% final output power		100		ns
	Turn-off Time	P_D = high to initial output power –30 dB		100		ns

7.9 Typical Characteristics (TRF37A32)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 950 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

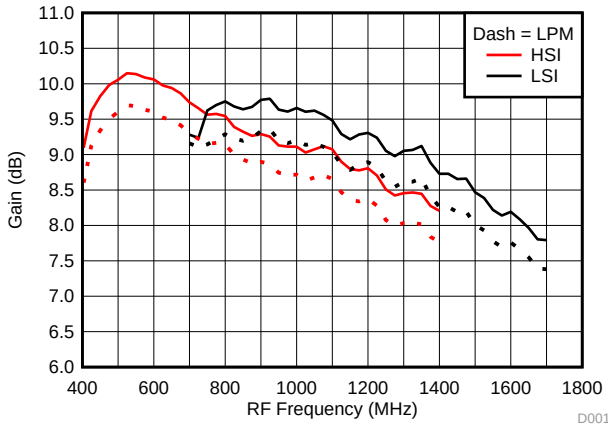


Figure 1. Gain vs Frequency over H/LSI, LPM

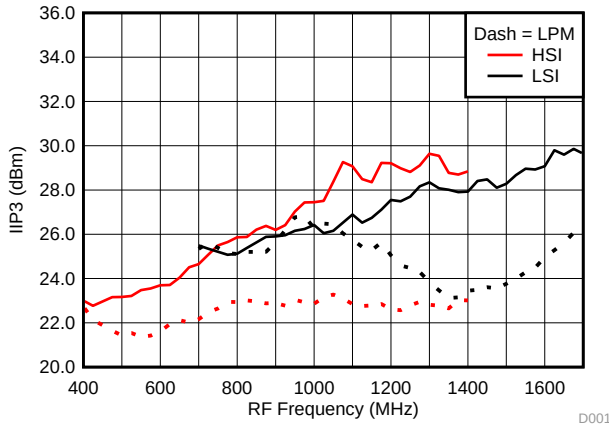


Figure 2. IIP3 vs Frequency over H/LSI, LPM

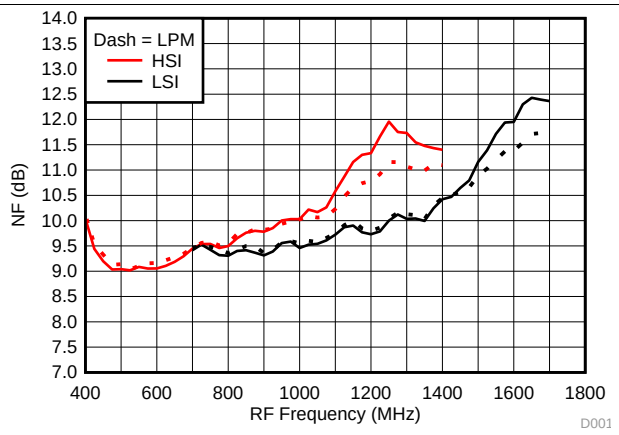


Figure 3. NF vs Frequency over H/LSI, LPM

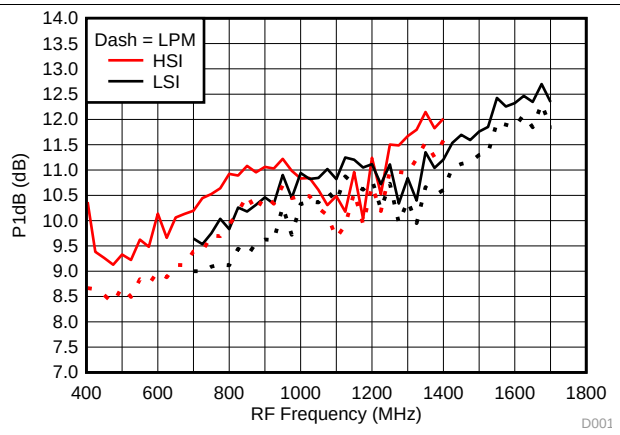


Figure 4. Input P1dB vs Frequency over H/LSI, LPM

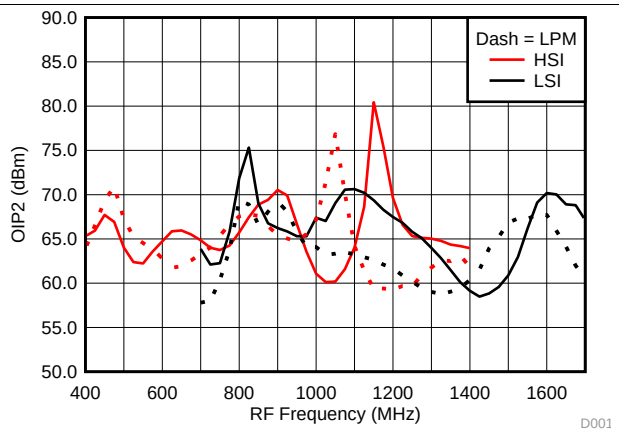


Figure 5. OIP2 vs Frequency over H/LSI, LPM

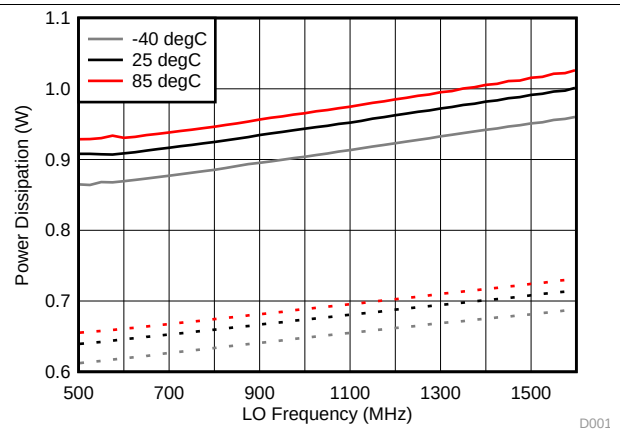


Figure 6. Power Dissipation vs Temperature, LPM

Typical Characteristics (TRF37A32) (continued)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 950 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

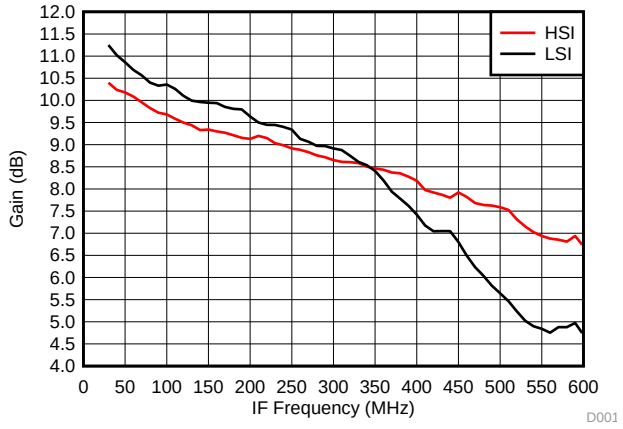


Figure 7. Gain vs IF Frequency over H/LSI

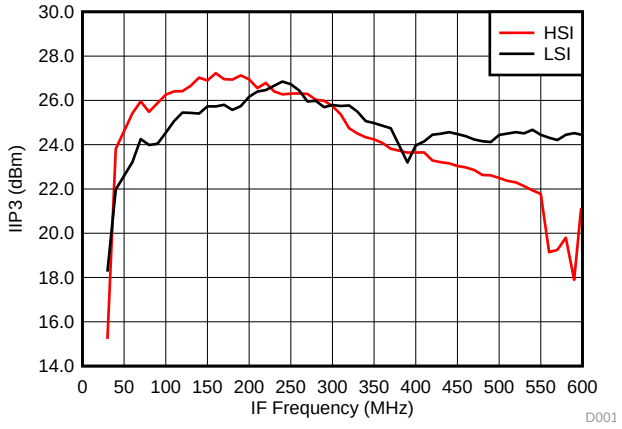


Figure 8. IIP3 vs IF Frequency over H/LSI

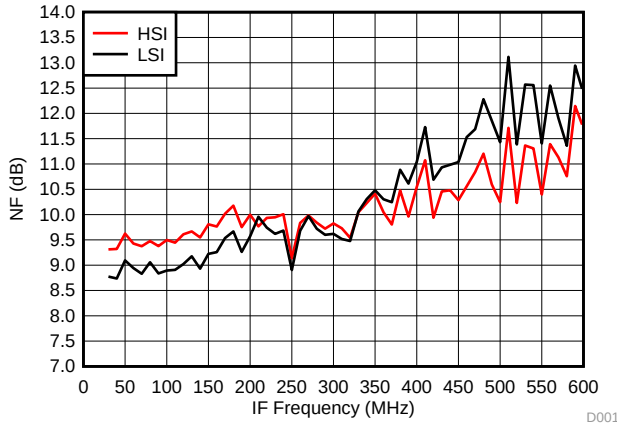


Figure 9. NF vs IF Frequency over H/LSI

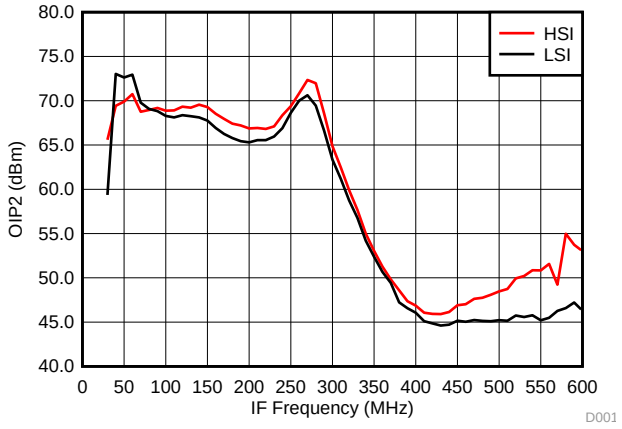


Figure 10. OIP2 vs IF Frequency over H/LSI

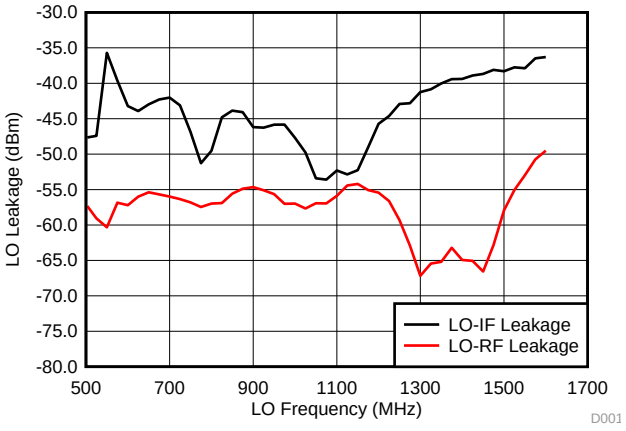


Figure 11. LO-IF/RF Leakage vs Frequency

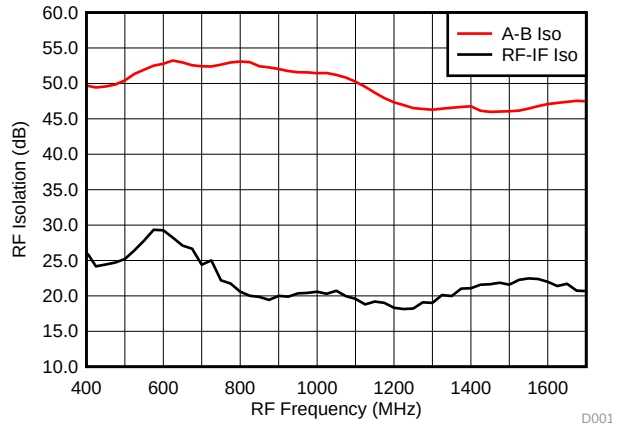


Figure 12. A-B Channel and RF-IF Isolation

Typical Characteristics (TRF37A32) (continued)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 950 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

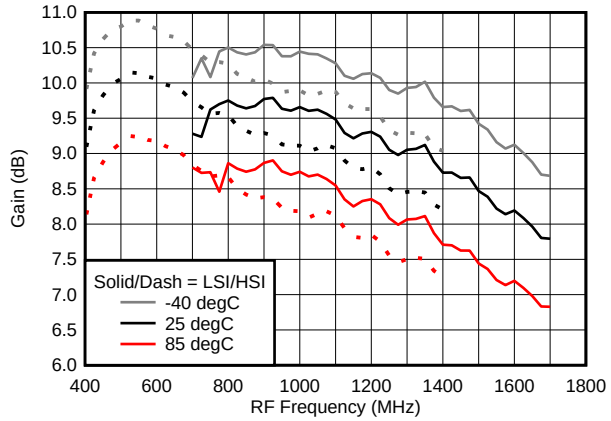


Figure 13. Gain vs Frequency over Temperature (HSI/LSI)

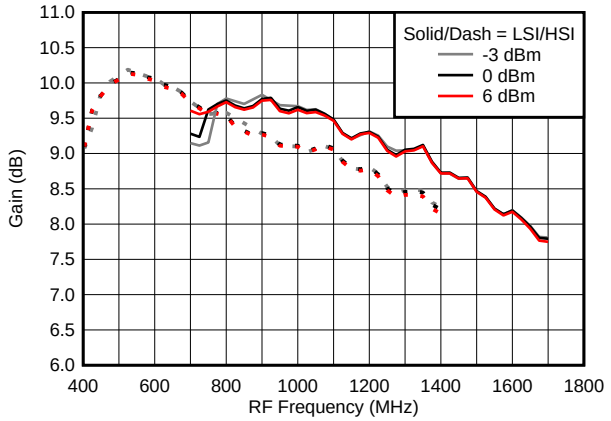


Figure 14. Gain vs Frequency over LO Drive (H/LSI)

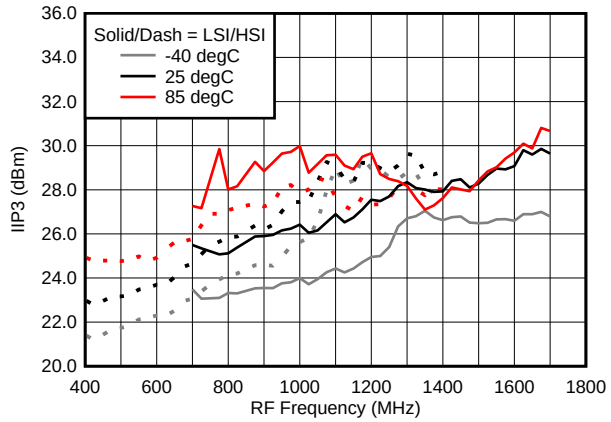


Figure 15. IIP3 vs Frequency over Temperature (HSI/LSI)

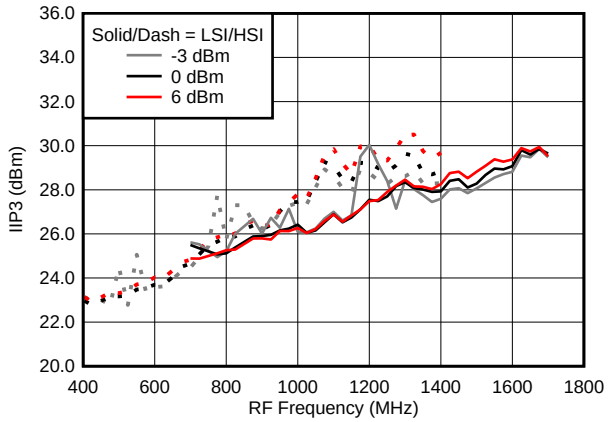


Figure 16. IIP3 vs Frequency over LO Drive (H/LSI)

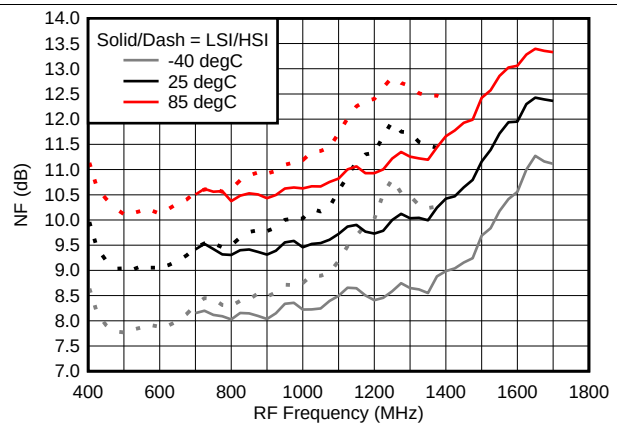


Figure 17. NF vs Frequency over Temperature (HSI/LSI)

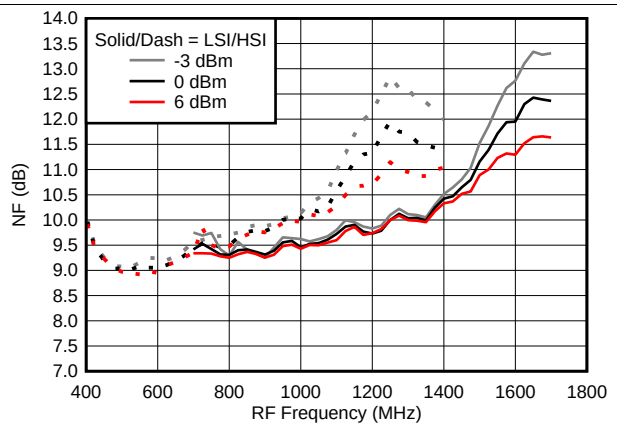


Figure 18. NF vs Frequency over LO Drive (H/LSI)

Typical Characteristics (TRF37A32) (continued)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 950 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

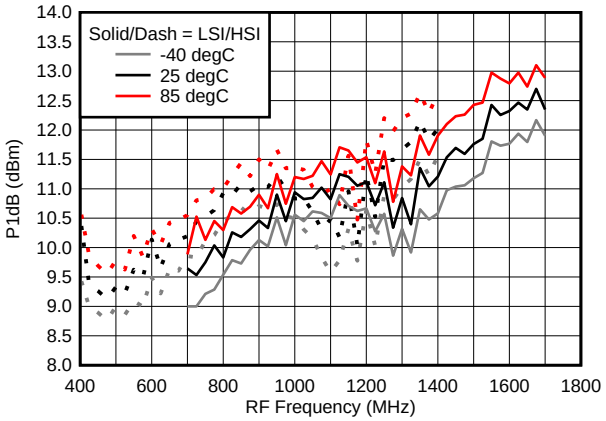


Figure 19. Input P1dB vs Frequency over Temperature (HSI/LSI)

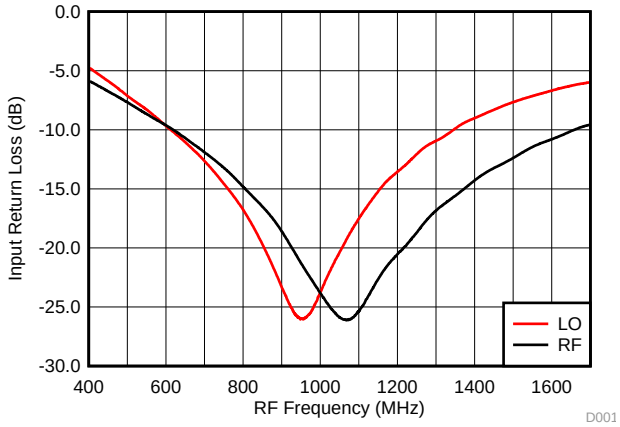


Figure 20. RF/LO Input Return Loss

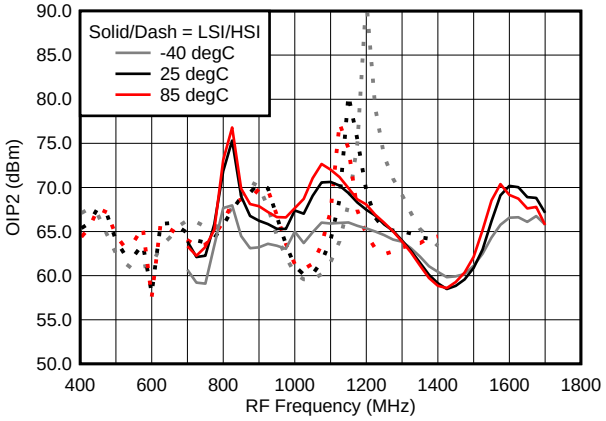


Figure 21. OIP2 vs Frequency over Temperature (HSI/LSI)

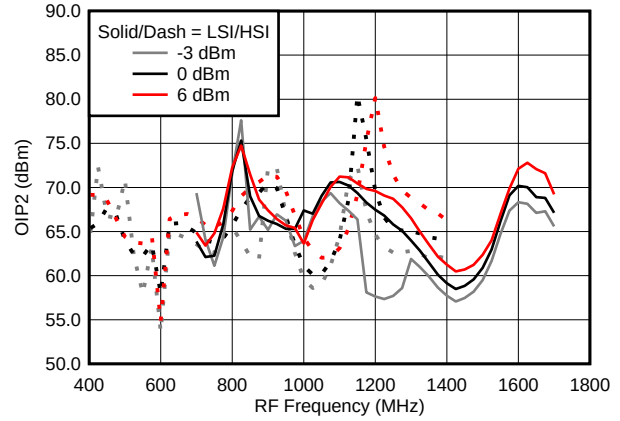


Figure 22. OIP2 vs Frequency over LO Drive (H/LSI)

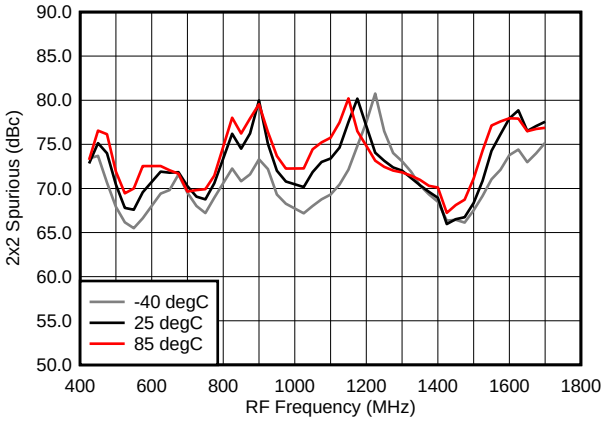


Figure 23. 2 x 2 Spurious over Temperature (H/LSI)

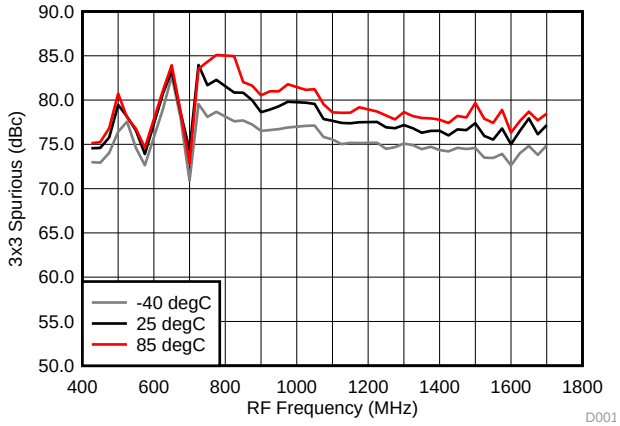


Figure 24. 3 x 3 Spurious over Temperature (H/LSI)

7.10 Typical Characteristics (TRF37B32)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 1950 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

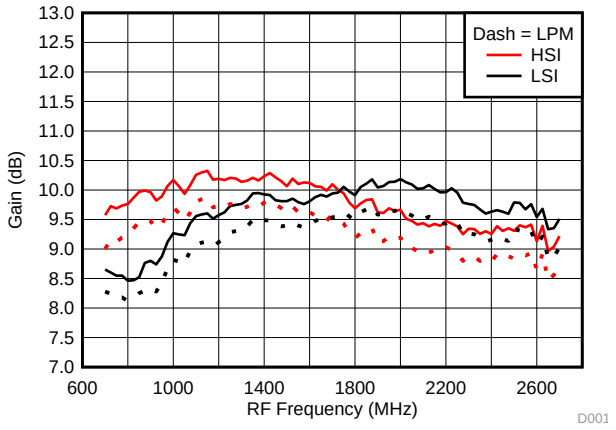


Figure 25. Gain vs Frequency over H/LSI, LPM

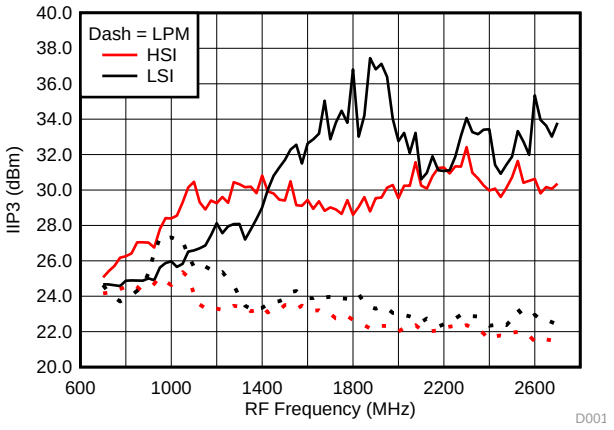


Figure 26. IIP3 vs Frequency over H/LSI, LPM

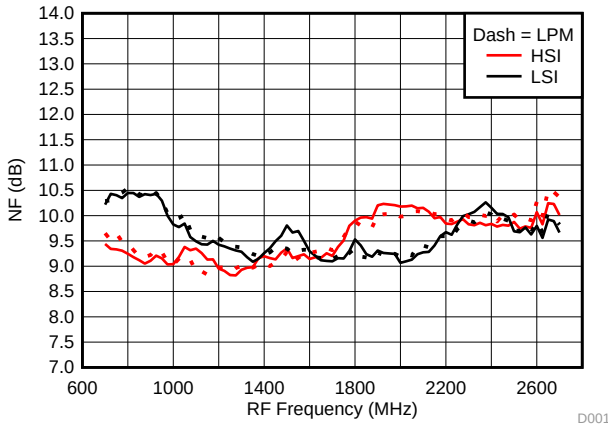


Figure 27. NF vs Frequency over H/LSI, LPM

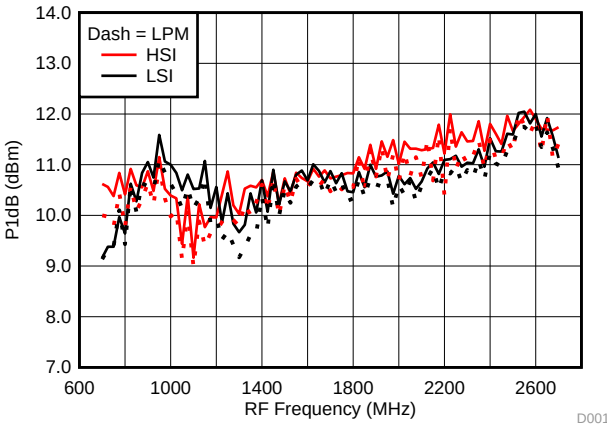


Figure 28. Input P1dB vs Frequency over H/LSI, LPM

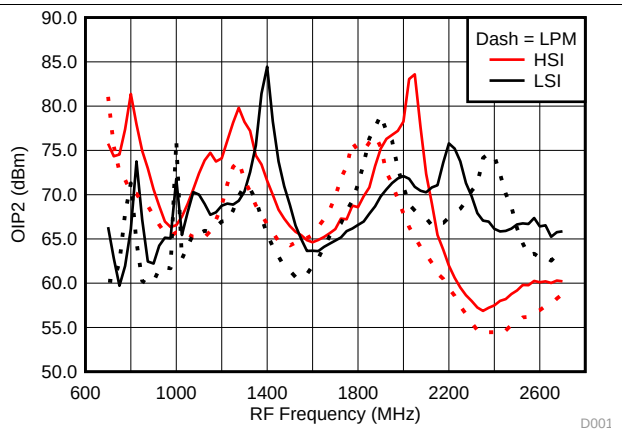


Figure 29. OIP2 vs Frequency over H/LSI, LPM

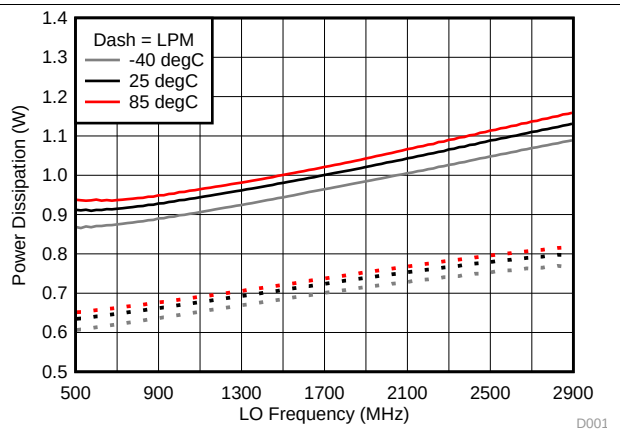


Figure 30. Power Dissipation vs Temperature, LPM

Typical Characteristics (TRF37B32) (continued)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 1950 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

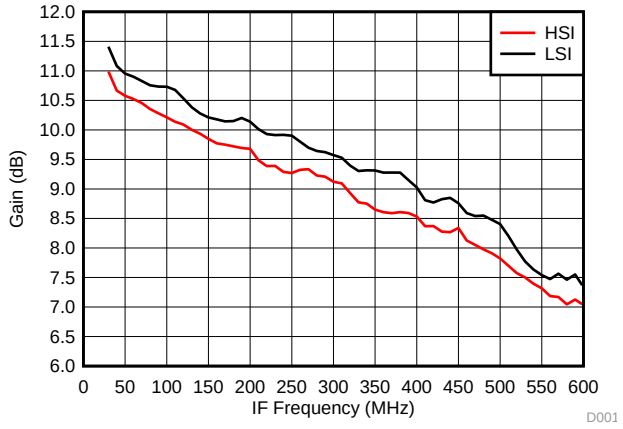


Figure 31. Gain vs IF Frequency over H/LSI

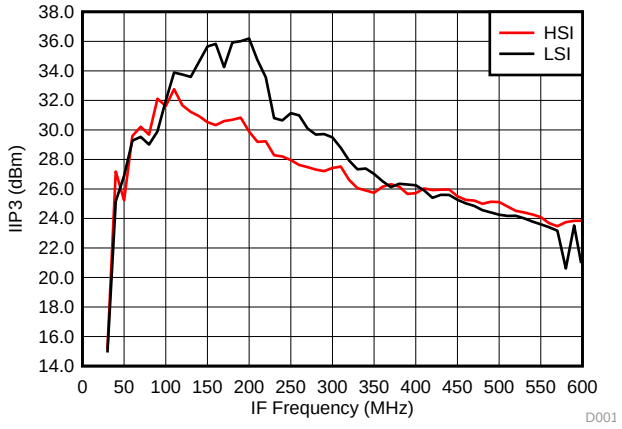


Figure 32. IIP3 vs IF Frequency over H/LSI

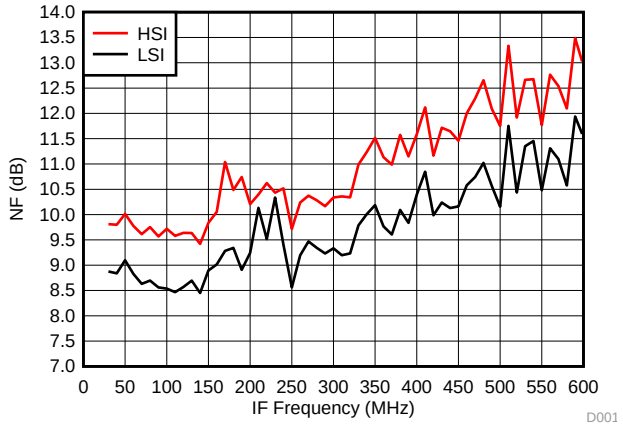


Figure 33. NF vs IF Frequency over H/LSI

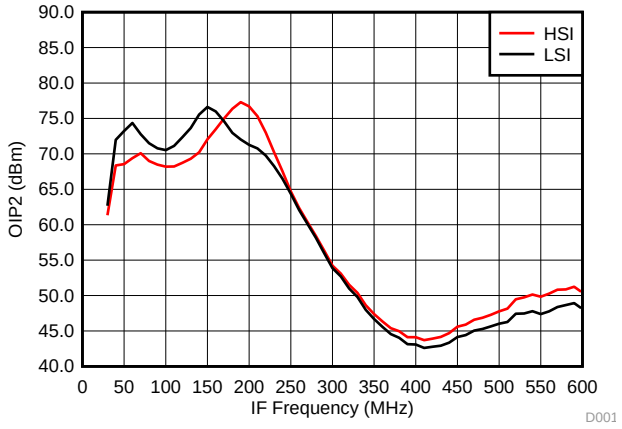


Figure 34. OIP2 vs IF Frequency over H/LSI

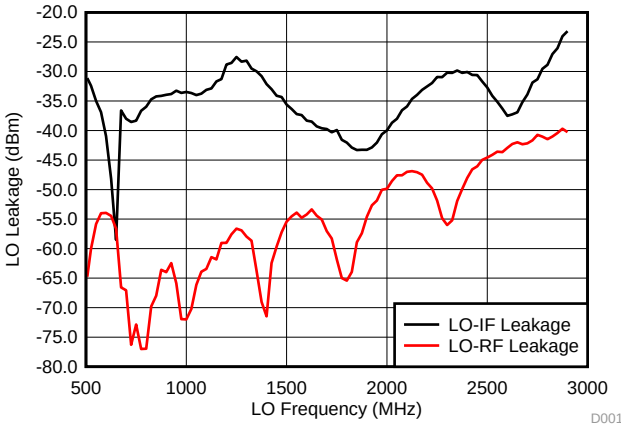


Figure 35. LO-IF/RF Leakage vs Frequency

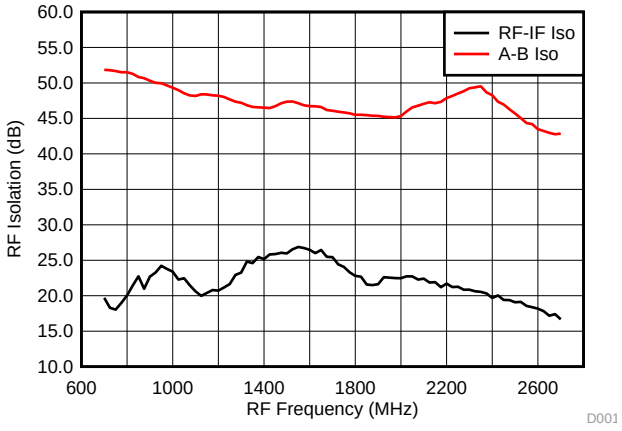


Figure 36. A-B Channel and RF-IF Isolation

Typical Characteristics (TRF37B32) (continued)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 1950 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

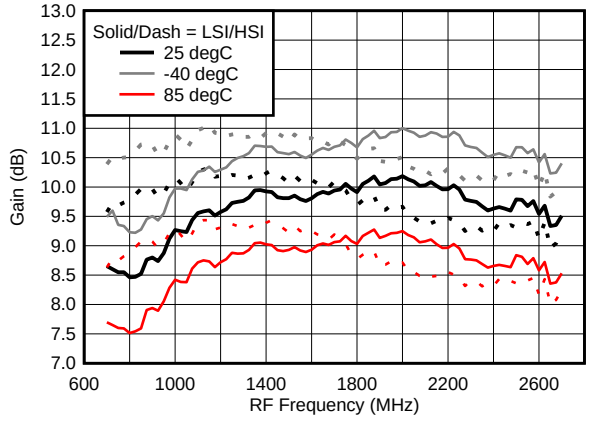


Figure 37. Gain vs Frequency over Temperature (HSI/LSI)

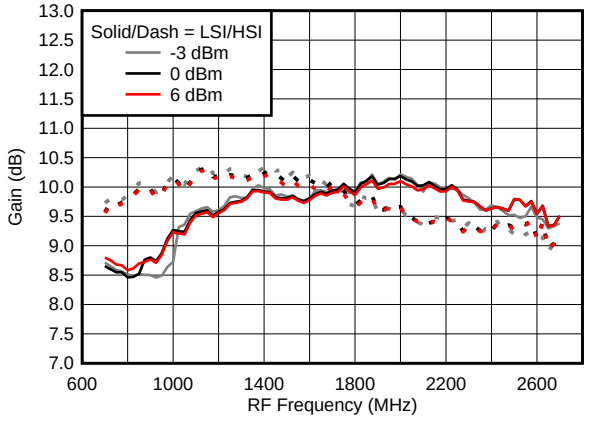


Figure 38. Gain vs Frequency over LO Drive (H/LSI)

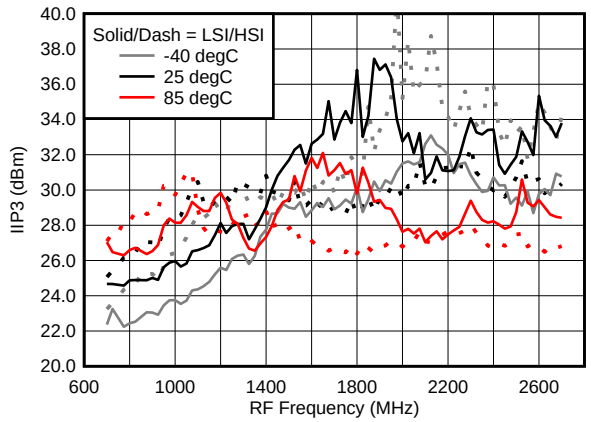


Figure 39. IIP3 vs Frequency over Temperature (HSI/LSI)

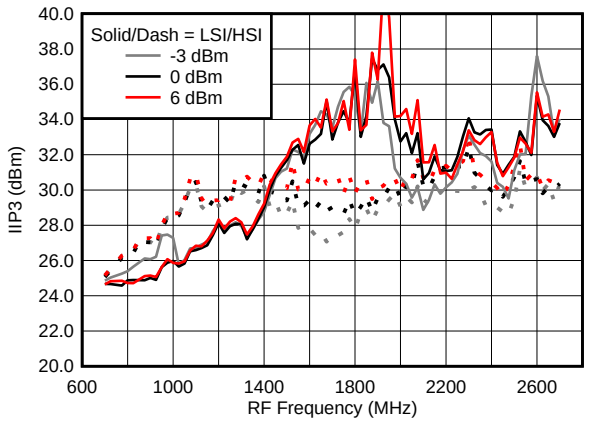


Figure 40. IIP3 vs Frequency over LO Drive (H/LSI)

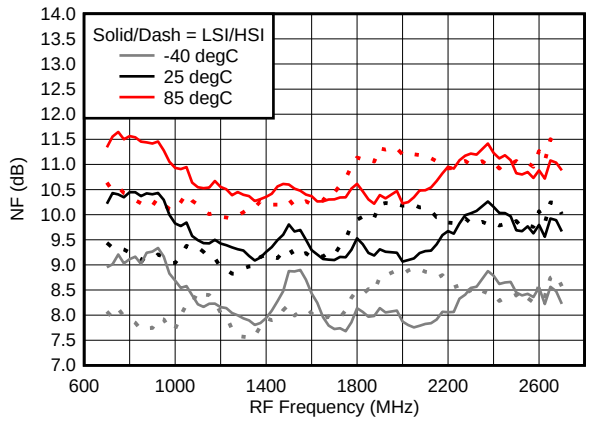


Figure 41. NF vs Frequency over Temperature (HSI/LSI)

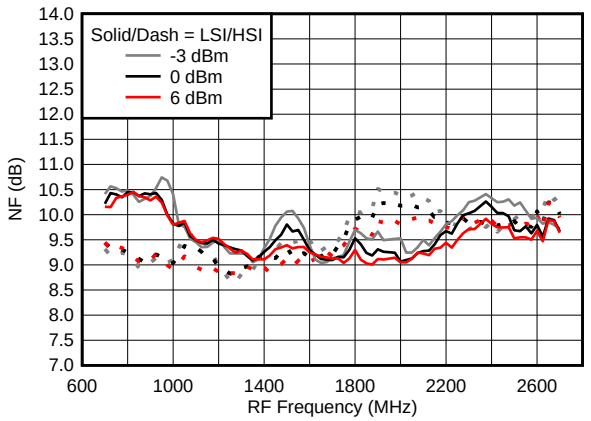


Figure 42. NF vs Frequency over LO Drive (H/LSI)

Typical Characteristics (TRF37B32) (continued)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 1950 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

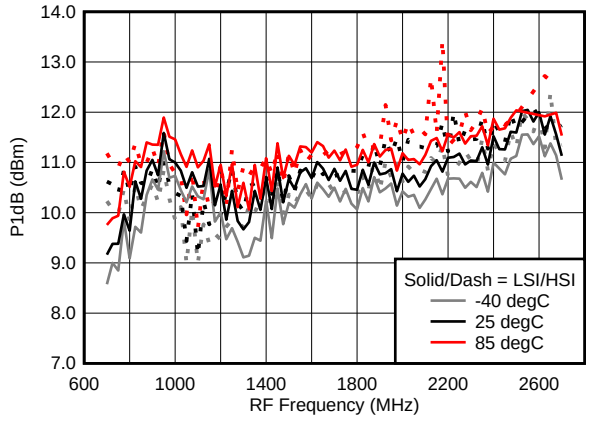


Figure 43. Input P1dB vs Frequency over Temperature (HSI/LSI)

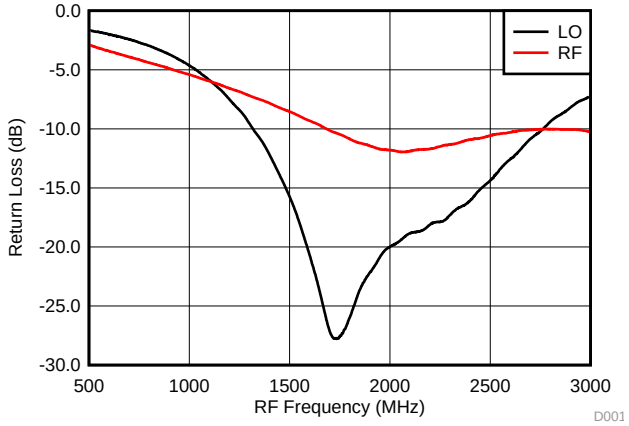


Figure 44. RF/LO Input Return Loss

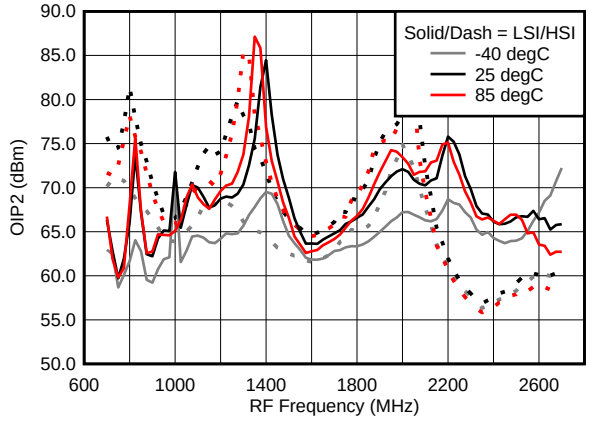


Figure 45. OIP2 vs Frequency over Temperature (HSI/LSI)

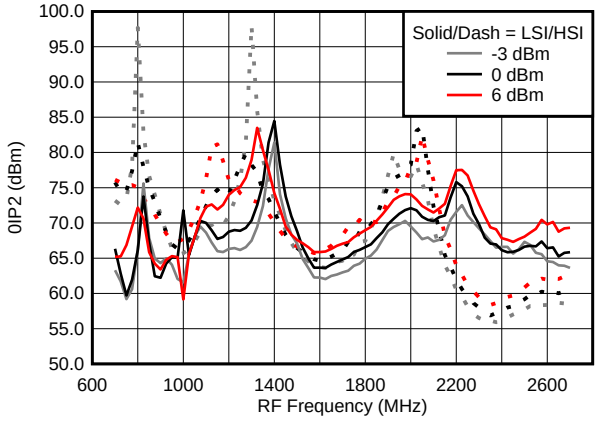


Figure 46. OIP2 vs Frequency over LO Drive (H/LSI)

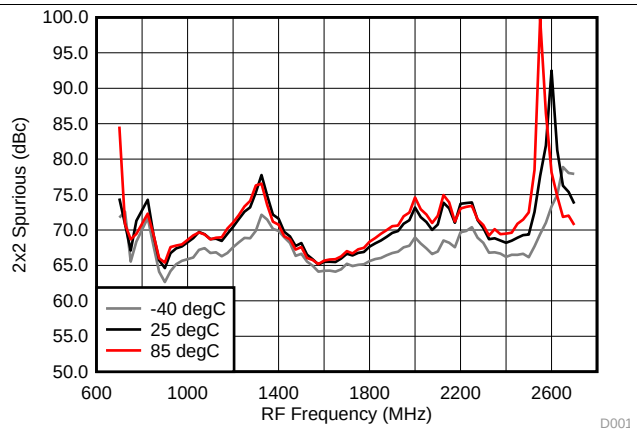


Figure 47. 2 x 2 Spurious over Temperature (H/LSI)

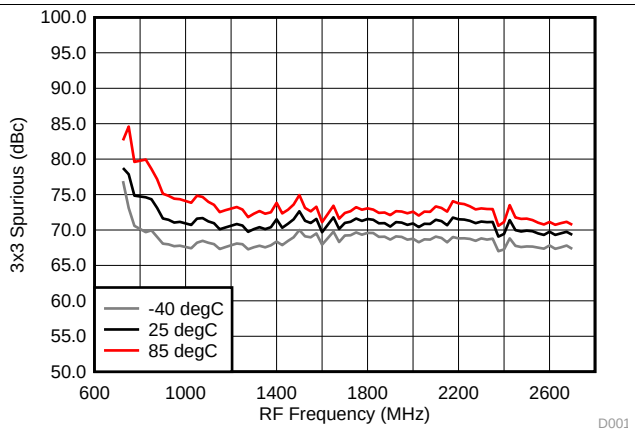


Figure 48. 3 x 3 Spurious over Temperature (H/LSI)

7.11 Typical Characteristics (TRF37C32)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 2500 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

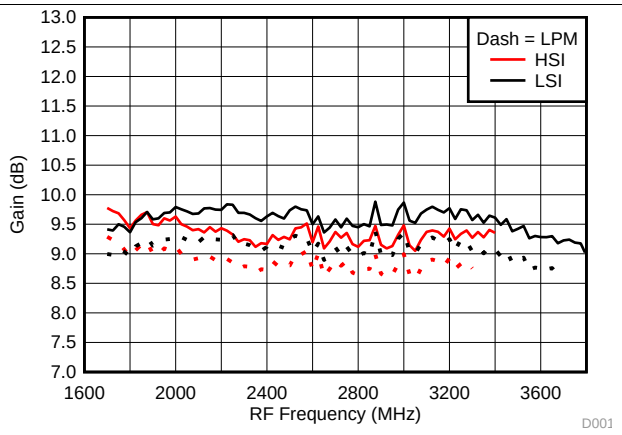


Figure 49. Gain vs Frequency over H/LSI, LPM

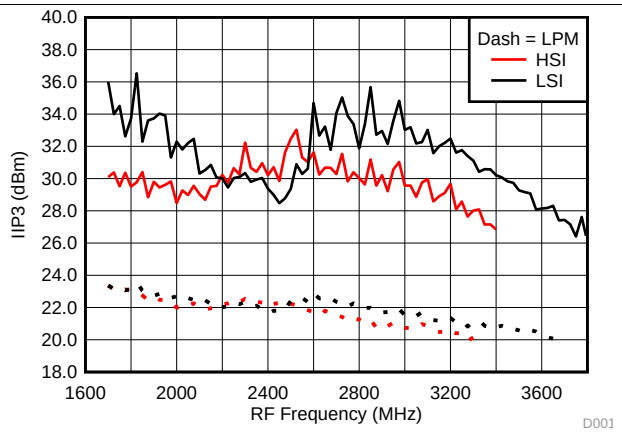


Figure 50. IIP3 vs Frequency over H/LSI, LPM

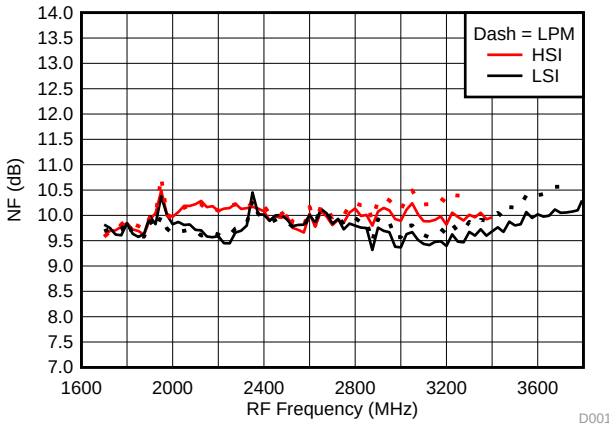


Figure 51. NF vs Frequency over H/LSI, LPM

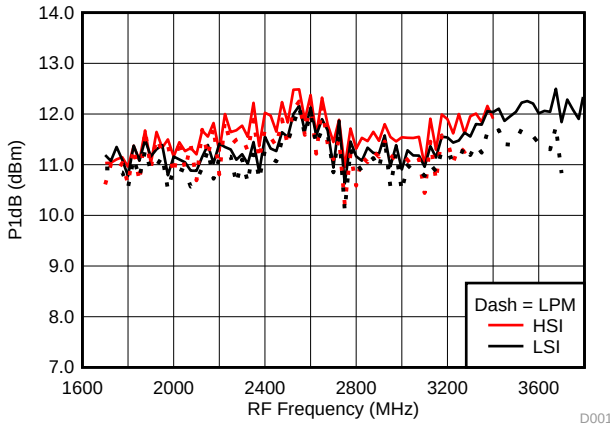


Figure 52. Input P1dB vs Frequency over H/LSI, LPM

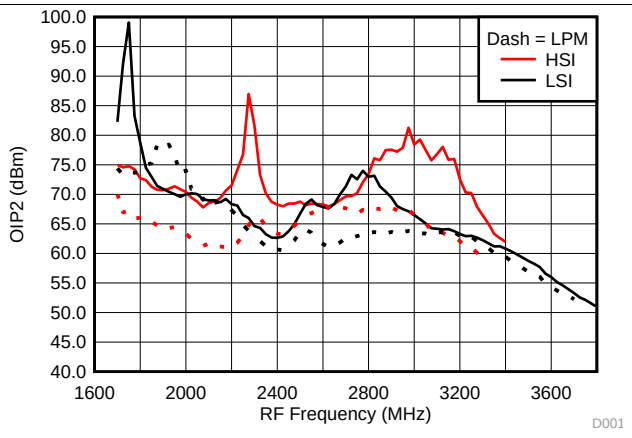


Figure 53. OIP2 vs Frequency over H/LSI, LPM

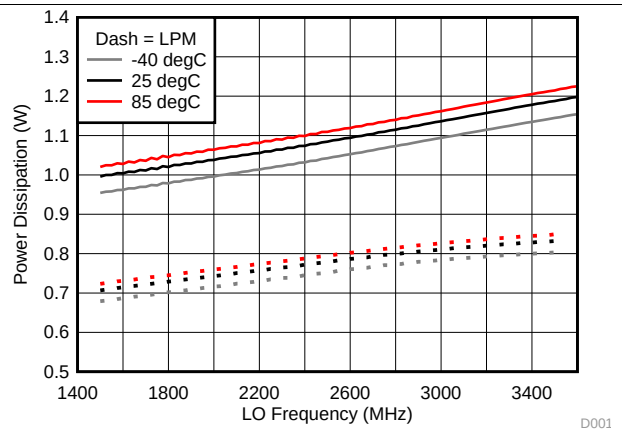


Figure 54. Power Dissipation vs Temperature, LPM

Typical Characteristics (TRF37C32) (continued)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 2500 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

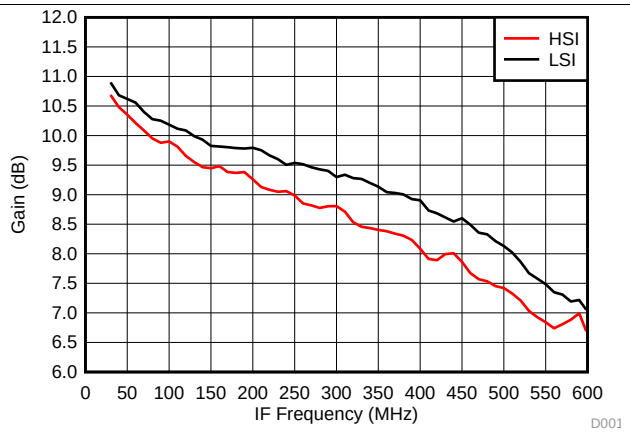


Figure 55. Gain vs IF Frequency over H/LSI

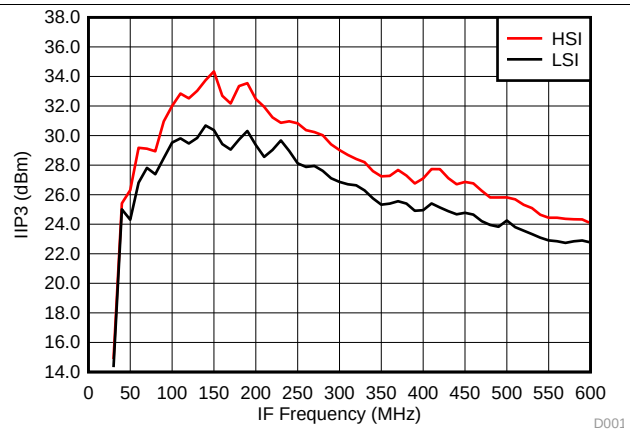


Figure 56. IIP3 vs IF Frequency over H/LSI

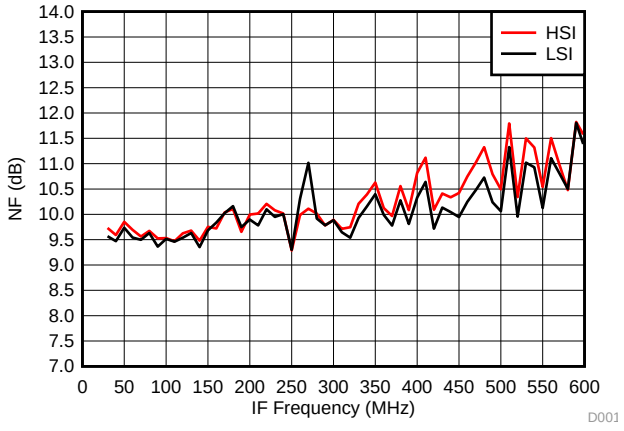


Figure 57. NF vs IF Frequency over H/LSI

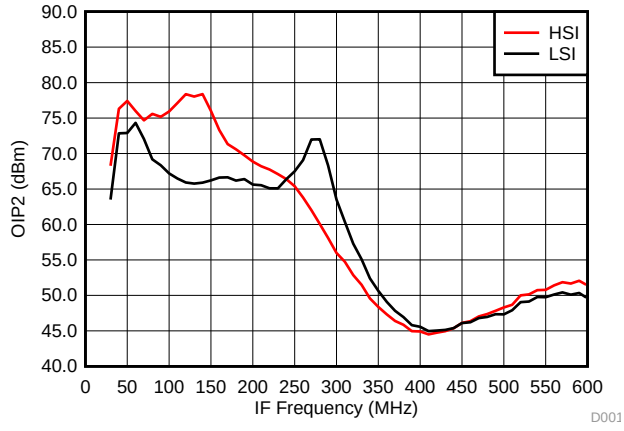


Figure 58. OIP2 vs IF Frequency over H/LSI

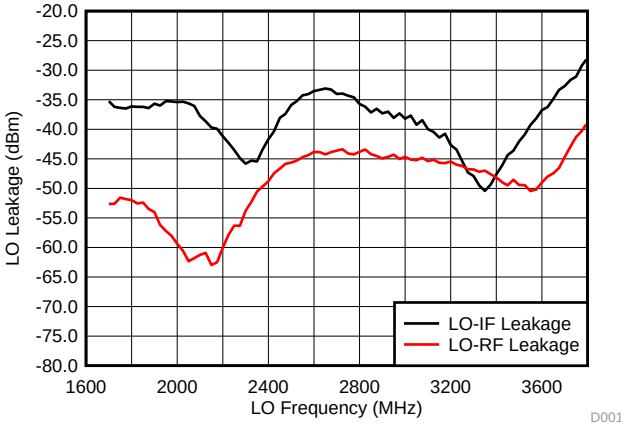


Figure 59. LO-IF/RF Leakage vs Frequency

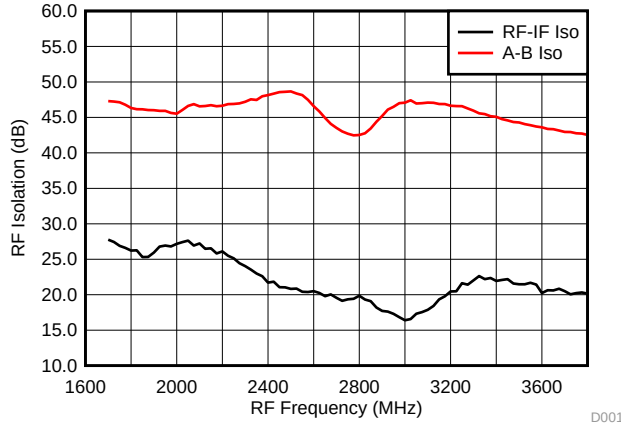


Figure 60. A-B Channel and RF-IF Isolation

Typical Characteristics (TRF37C32) (continued)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 2500 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

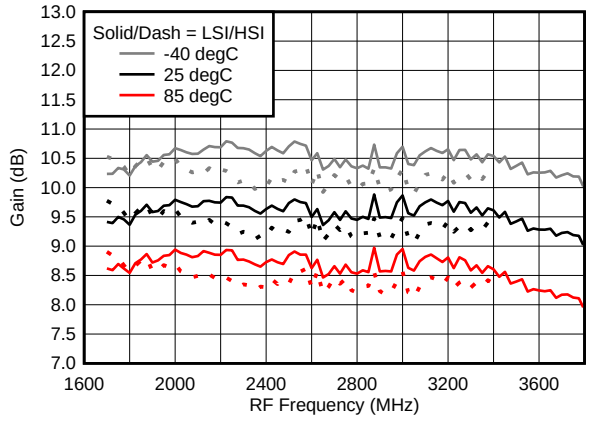


Figure 61. Gain vs Frequency over Temperature (HSI/LSI)

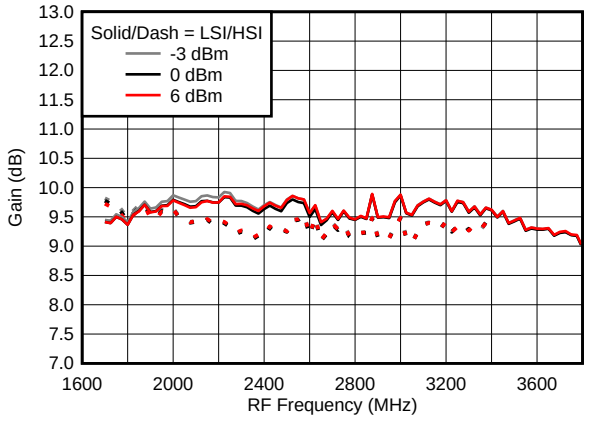


Figure 62. Gain vs Frequency over LO Drive (H/LSI)

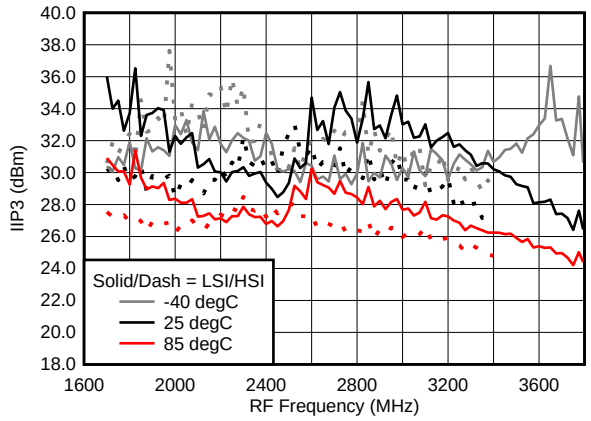


Figure 63. IIP3 vs Frequency over Temperature (HSI/LSI)

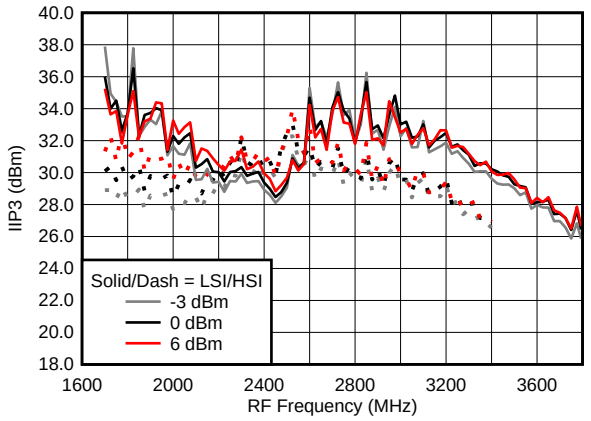


Figure 64. IIP3 vs Frequency over LO Drive (H/LSI)

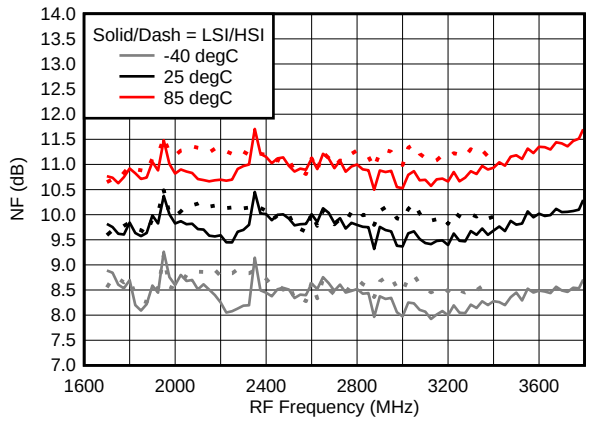


Figure 65. NF vs Frequency over Temperature (HSI/LSI)

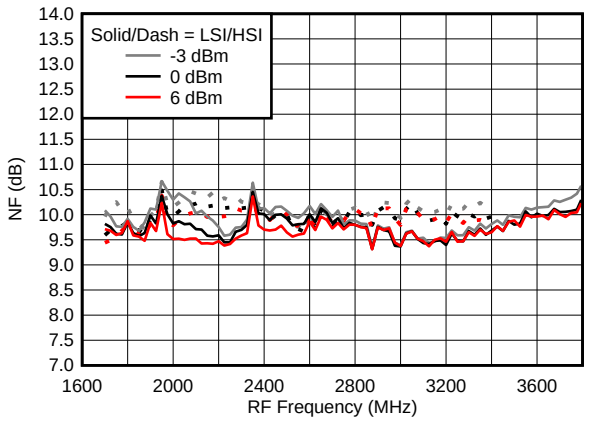


Figure 66. NF vs Frequency over LO Drive (H/LSI)

Typical Characteristics (TRF37C32) (continued)

T_A = 25°C, V_{CC} = 3.3 V; P_{RF} = –10 dBm; F_{RF} = 2500 MHz; P_{LO} = 0 dBm; F_{IF} = 200 MHz; Low Side Injection, LPM = 0 (unless otherwise noted)

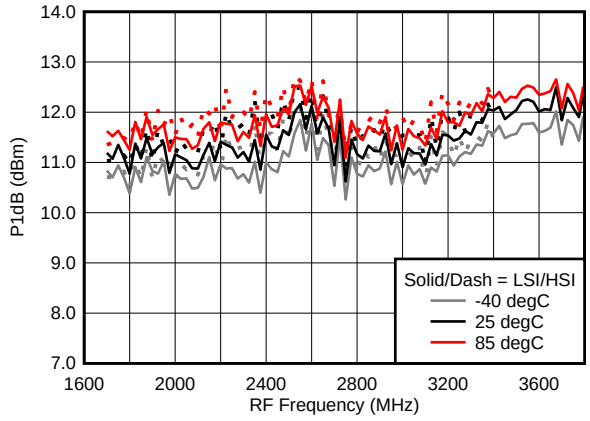


Figure 67. Input P1dB vs Frequency over Temperature (HSI/LSI)

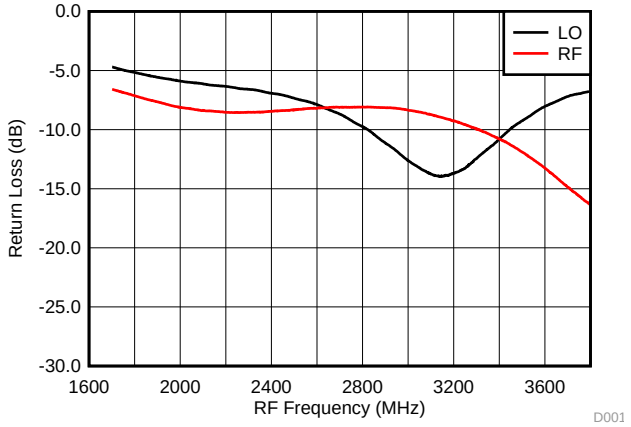


Figure 68. RF/LO Input Return Loss

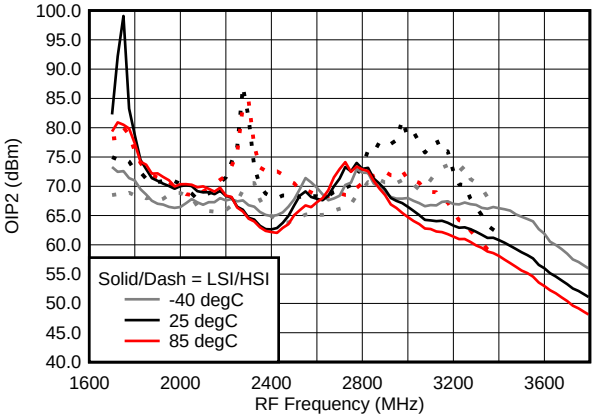


Figure 69. OIP2 vs Frequency over Temperature (HSI/LSI)

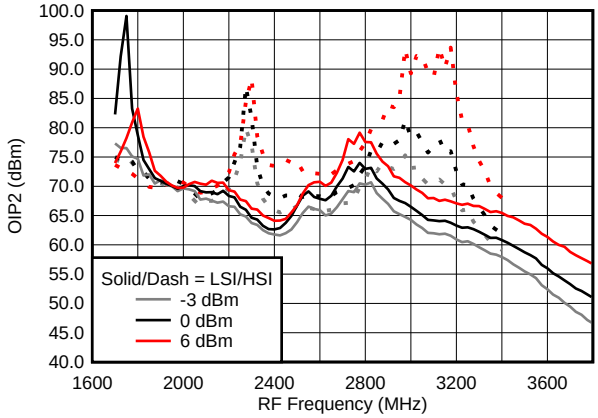


Figure 70. OIP2 vs Frequency over LO Drive (H/LSI)

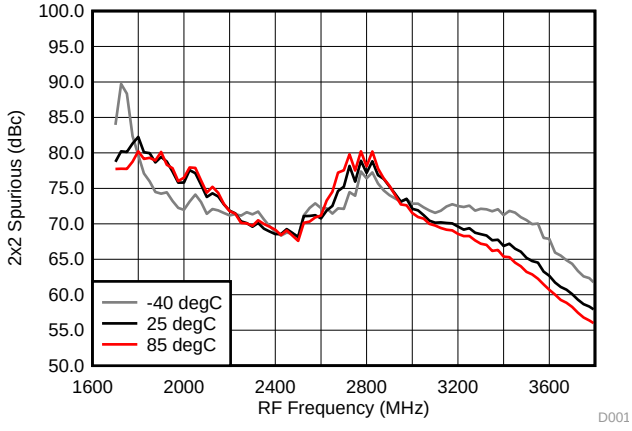


Figure 71. 2 x 2 Spurious over Temperature (H/LSI)

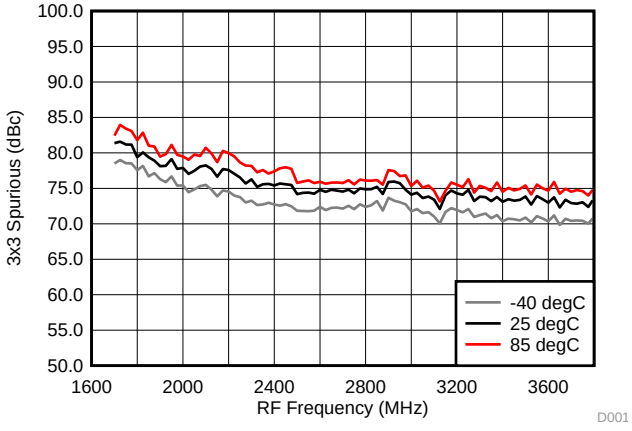


Figure 72. 3 x 3 Spurious over Temperature (H/LSI)

8 Detailed Description

8.1 Overview

The TRF37x32 family is a dual-channel, down convert receive mixer. It provides high-linearity over wide RF and IF bandwidths while also consuming low power. The device comes in three varieties, A, B, and C, to cover an extremely wide frequency band and can operate with either low side injection (LSI) or high side injection (HSI). The IF output is optimized for 200 MHz but operates from 30 MHz to 600 MHz with appropriate external components.

The device consists of a passive mixer core buffered by an LO amplifier and a high-linearity IF amplifier. There is an on-chip LDO to regulate VCC to the voltages needed for the small-geometry SiGe BiCMOS components. The single-ended RF and LO inputs each have a wideband internal balun. The balun's center tap is internally grounded.

Each channel offers an external power down terminal control which disables the IF circuitry. The device has a low power mode controlled through an external terminal control. Low power mode reduces bias current in the LO circuitry. Both power down and low power mode controls are internally biased to a normal operating state. The IFA/B_BT terminals are self-biased and require no external components.

The TRF37x32 uses a single 3.3 V power supply and draws exceptionally low current for its performance node.

8.2 Functional Block Diagram

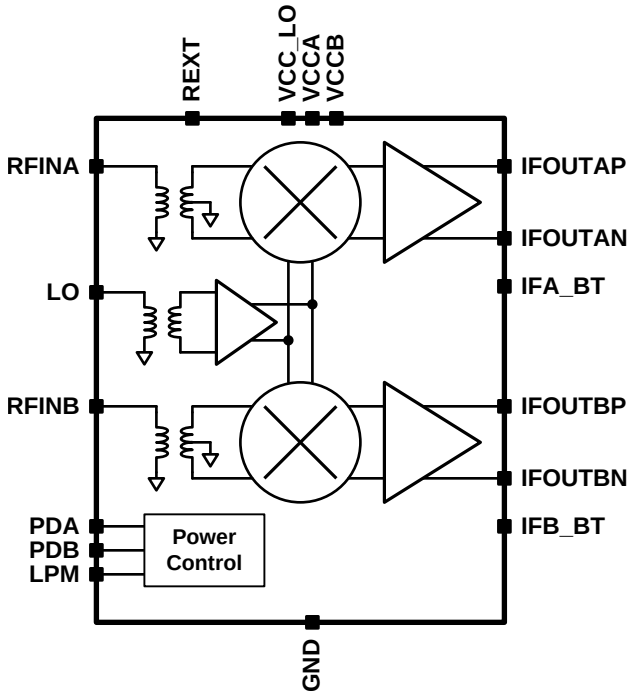


Figure 73. Block Diagram

8.3 Feature Description

8.3.1 Low Power Mode

Low power mode is enabled by setting the active-high LPM terminal to a logic high. The device contains an internal pull-down to engage normal operation when the terminal is left unconnected or floating.

Low power mode reduces the bias current in the LO amplifier portion of the device and affects both channels. Total current consumption is reduced 30% while lowering analog performance metrics.

8.3.2 Power Down

Each channel is powered down individually through the active-high PDA and PDB terminals. A logic high sets the respective channel in power down. The device contains an internal pull-down to engage normal operation when the terminal is left unconnected or floating.

Power down is implemented by removing bias in the IF amplifier. Operation of the opposite channel is not affected when either channel is turned off. Turn-on and turn-off time is fast enough to serve in most TDD applications.

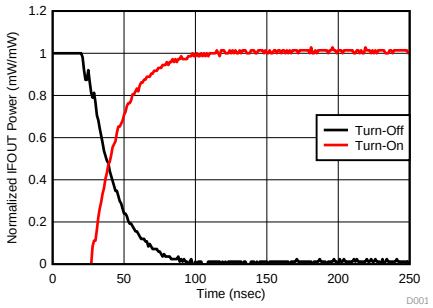


Figure 74. Device power down turn-on and turn-off time

8.3.3 Single Ended RF Input

Each RF input is single-ended with a wideband internal balun to convert the input to a differential signal, as shown in Figure 73. The center tap of the balun is internally grounded and is not available external to the device. The RF input should be ac coupled to driving circuitry according to the chart in Table 1.

Table 1. RF Input AC coupling capacitor

Device	Blocking Cap Value
TRF37A32	20 pF
TRF37B32	10 pF
TRF37C32	10 pF

8.3.4 Single Ended LO Input

The LO input is single ended with an internal balun to convert the input to a differential signal. The LO drive path includes a high frequency dual-mode oscillation inhibitor circuitry to ensure stable operation. For best operation it is recommended to keep the LO drive level at 0 dBm or higher to ensure inhibitor circuit does not falsely engage. At lower LO drive level, keep the LO power engaged to the device at power-up. At lower drive level the inhibitor may engage within certain frequency bands when the LO power transitions.

At the extreme RF frequencies the LO input bandwidth will force operation to either high side injection (HSI) or low side injection (LSI). Table 2 provides the operating range of the LO for each device.

Table 2. LO Input Frequency Operating Range

Device	Operating Range
TRF37A32	600 - 1400 MHz
TRF37B32	500 - 2900 MHz

Table 2. LO Input Frequency Operating Range (continued)

Device		Operating Range
TRF37C32	Low Power mode (LPM) disabled	1500 - 3600 MHz
	Low Power mode (LPM) enabled	1500 - 3500 MHz

8.3.5 IF Amplifier

The output of the device is driven by a high-linearity IF amplifier. The output nodes must be pulled up to VCC with high-Q inductors. It is designed to provide 200 Ω differential / 100 Ω single-ended output impedance. Layout should include symmetry for the differential output signal paths.

The IF output circuitry is optimized for performance at 200 MHz but operates over 30 MHz – 600 MHz.

8.4 Device Functional Modes

8.4.1 Low Power Mode

Low power mode is activated through the low power terminal, as described in the features description. It is designed for extremely low power consumption.

8.4.2 Single Channel and Shutdown Modes

The device may be operated as a single channel device by disabling one channel or in complete shutdown by disabling both channels.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The devices are high-linearity, wideband receive mixers. They are typically implemented to convert frequencies from the range 400 MHz to 3800 MHz into the range 30 MHz to 600 MHz.

9.2 Typical Application

The TRF37x32 device is typically placed in a system as illustrated in Figure 75.

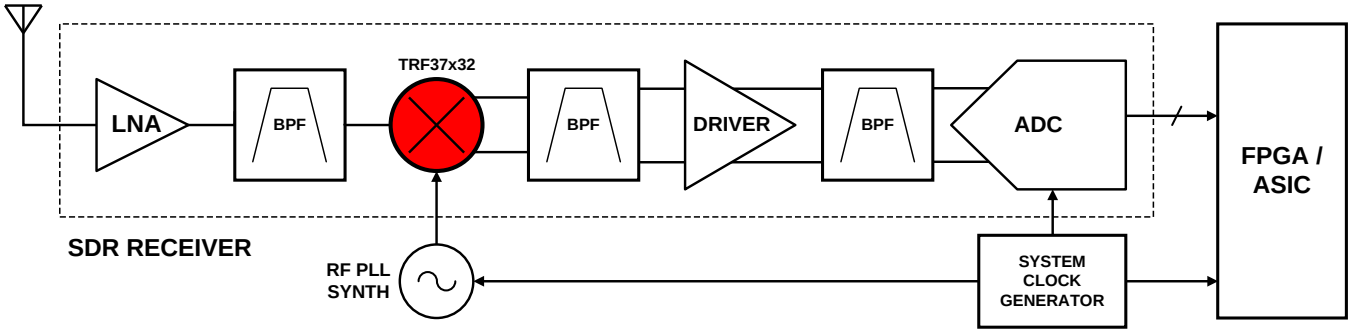


Figure 75. Typical System Implementation of TRF37x32

A typical schematic for the TRF37x32 is shown in Figure 76.

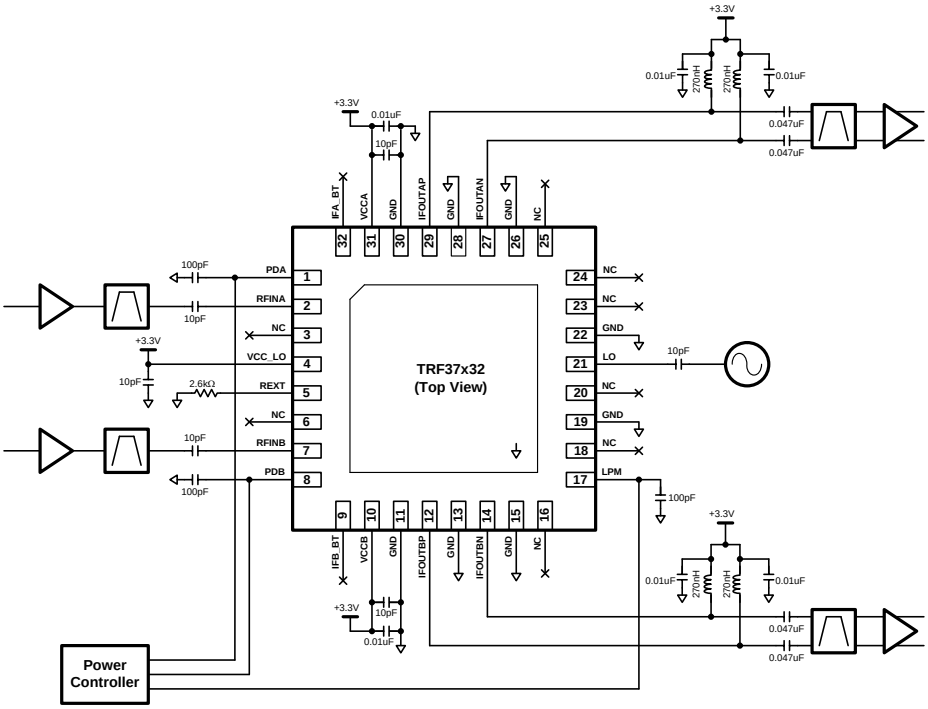


Figure 76. Typical Application Schematic for TRF37x32

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 3.

Table 3. Design Parameters

MIXER PARAMETER	EXAMPLE APPLICATION REQUIREMENTS(1)	TRF37B32 PERFORMANCE (TYPICAL)
RF Frequency Range	2300 - 2400 MHz	700 - 2700 MHz
IF Frequency Range	318.64 - 418.64 MHz	30 - 600 MHz
Gain	9 - 10 dB	9.7 dB at F_{RF} = 2300 MHz
NF	< 12 dB	10 dB at F_{RF} = 2300 MHz
IIP3	> 28 dBm	30 dBm at F_{RF} = 2300 MHz
IP1dB	> 8 dBm	11 dBm at F_{RF} = 2300 MHz

(1) The example application requirements are derived from a hypothetical application and do not reflect the performance of the TRF37x32.

9.2.2 Detailed Design Procedure

9.2.2.1 Power Level

Input power should back off from the TRF37x32 compression point for linear operation, ideally by 10dB or more. Choose LNA gain and gain scheduling in order to set the appropriate power level at the RF input to the TRF37x32.

Given the expected input power level, use the expected gain through the mixer and other elements, such as SAW filter and matching networks, to calculate the voltage expected at the ADC. Adjust gain and loss elements to maximize the utilization of ADC dynamic range.

9.2.2.2 Matching

Although the TRF37x32 was designed to interface with 50 Ω RF and LO and 200 Ω differential signal lines, some elements in the signal chain may not present a wideband real impedance. Matching components are optional but may be used at these ports to improve impedance alignment, thereby increasing power delivered to the RF node and decreasing reflected and radiated power. Good matching maximizes isolation and linearity performance.

9.2.2.3 RF Input Component Selection

The blocking capacitor value on the RF input should be selected according to Table 1.

9.2.2.4 IF Output Component Selection

Use high Q inductors for pull-up biasing on the IF output. 270 nH 0805-size wirewound indictors provides excellent linearity and gain. Larger inductor values may compress the IF bandwidth, while smaller package sizes tend to introduce lower inductor Q ratings.

Connect the supply nodes of both inductors for a given channel symmetrically to the VCC net with close proximity to ensure balanced connection to the supply.

9.2.2.5 Frequency Planning

The LO and RF inputs are both designed for wideband behavior, and either high-side or low-side injection may be used interchangeably across most of the RF band. At the extreme RF frequencies the LO input bandwidth will force operation to either high side injection (HSI) or low side injection (LSI). Table 2 provides the operating range of the LO for each device. Where possible it is recommended to utilize low side injection to keep the power dissipation to a minimum.

9.2.2.6 Control Terminal Transients

Decoupling capacitors reduce terminal noise but also slow transient response. Adjust external capacitors in order to meet specified power-on and power-off response times. Apply transmission line matching techniques to achieve the fastest response times.

9.2.3 Application Curves

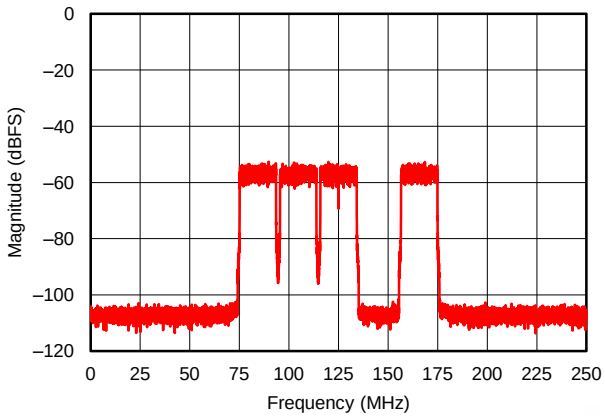


Figure 77. 4-Carrier Receiver Application

10 Power Supply Recommendations

The nominal voltage supply is 3.3 V; however, the TRF37x32 offers very consistent performance across the entire recommended voltage range. Signal isolation depends partly on power supply isolation. All supplies may be generated from a common source but should be isolated through decoupling capacitors placed close to the device. The typical application schematic in Figure 76 is an excellent example. Select capacitors with self-resonant frequency near the application frequency or noise frequency. When multiple capacitors are used in parallel to create a broadband decoupling network, place the capacitor with the higher self-resonant frequency closer to the device.

10.1 Power Up Sequence

No power up sequence is required.

11 Layout

11.1 Layout Guidelines

Good layout practice helps to enable excellent linearity and isolation performance. An example of good layout is shown in Figure 78. In the example, only the top signal layer and its adjacent ground reference plane are shown. Some recommended layout principles include the following:

- Excellent electrical connection from the PowerPAD™ to the board ground is essential. Use the recommended footprint, solder the pad to the board, and do not include solder mask under the pad
- Connect pad ground to device terminal ground on the top board layer.
- Verify that the return current path follows the primary current path by including topside terminal to pour ground connection and vias close to any reference layer transition.
- Do not route signal lines over breaks in the reference plane.
- Maintain symmetry as much as possible between lines in a differential pair. Match electrical lengths.
- Avoid routing clocks and digital control lines near signal lines.
- Do not route signal lines over noisy power planes. Ground is the best reference, although clean power planes can serve where necessary.
- Place supply decoupling close to the device.
- Keep channels physically separated to improve isolation.

11.2 Layout Example

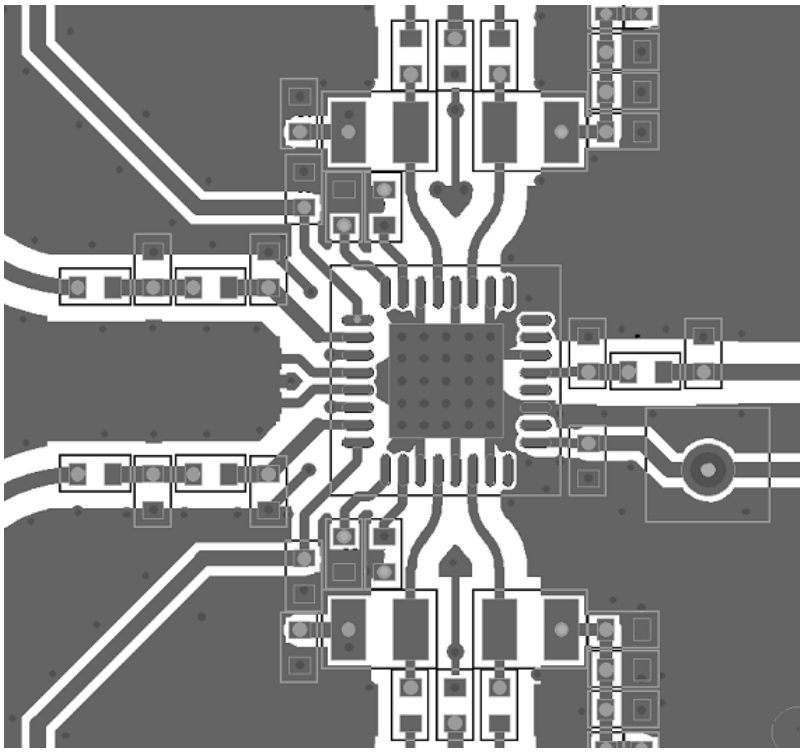


Figure 78.

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TRF37A32	Click here	Click here	Click here	Click here	Click here
TRF37B32	Click here	Click here	Click here	Click here	Click here
TRF37C32	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF37A32IRTVR	ACTIVE	WQFN	RTV	32	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TR37A32 IRTV	Samples
TRF37A32IRTVT	ACTIVE	WQFN	RTV	32	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TR37A32 IRTV	Samples
TRF37B32IRTVR	ACTIVE	WQFN	RTV	32	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TR37B32 IRTV	Samples
TRF37B32IRTVT	ACTIVE	WQFN	RTV	32	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TR37B32 IRTV	Samples
TRF37C32IRTVR	ACTIVE	WQFN	RTV	32	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TR37C32 IRTV	Samples
TRF37C32IRTVT	ACTIVE	WQFN	RTV	32	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TR37C32 IRTV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

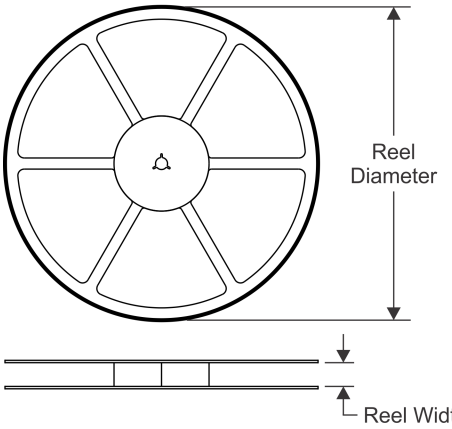
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

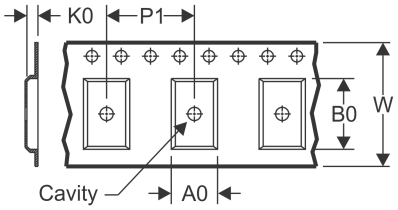
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

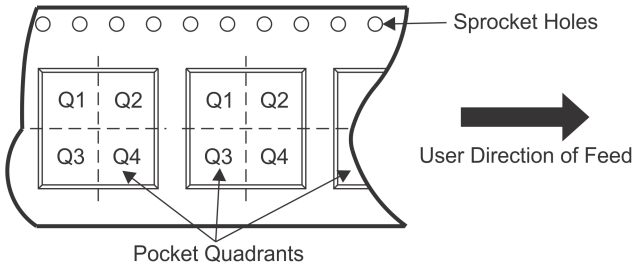


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

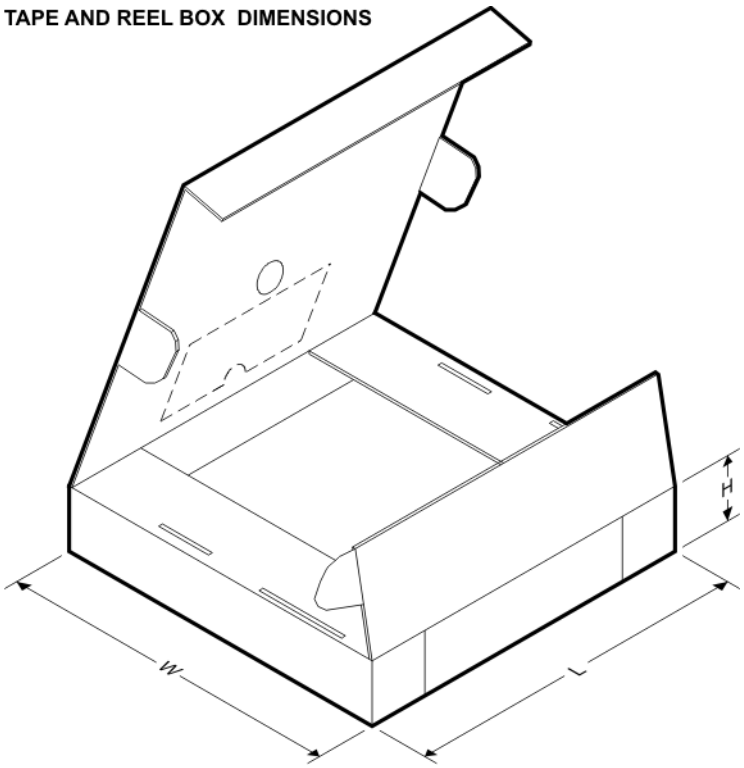
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF37A32IRTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF37B32IRTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF37C32IRTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

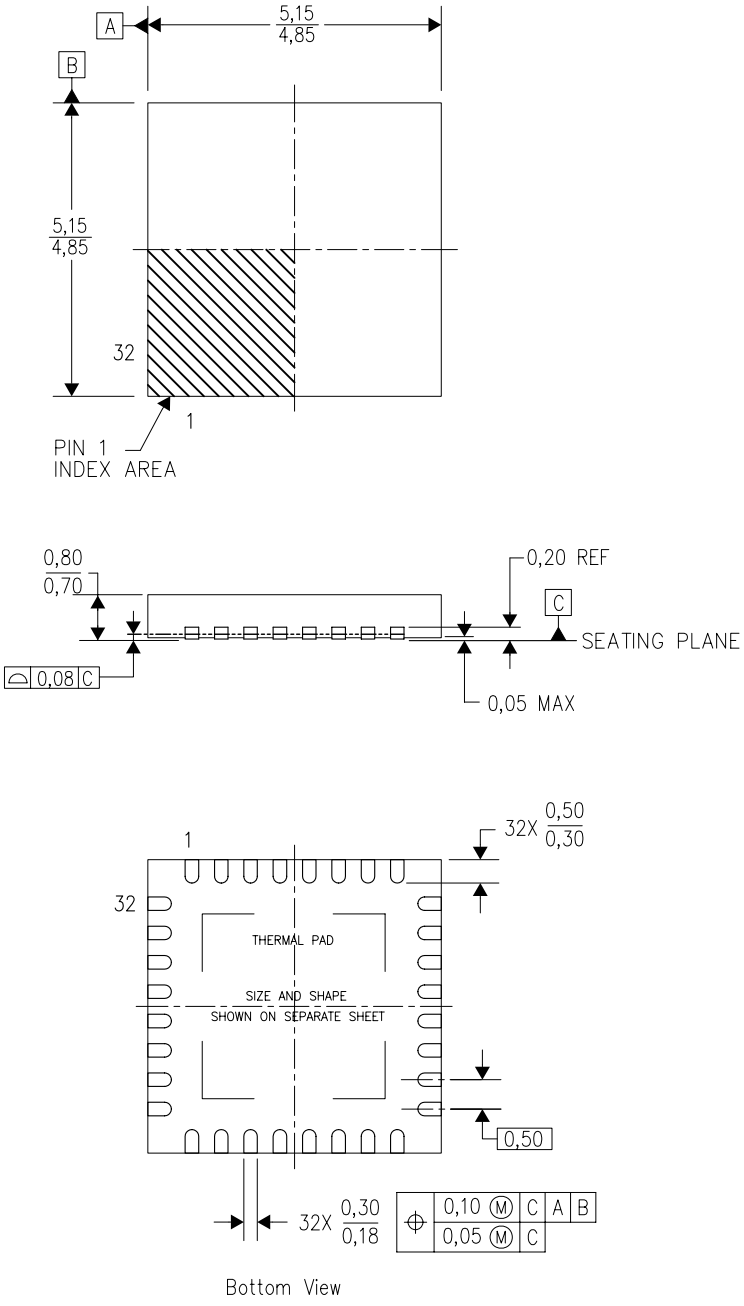
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF37A32IRTVR	WQFN	RTV	32	3000	350.0	350.0	43.0
TRF37B32IRTVR	WQFN	RTV	32	3000	350.0	350.0	43.0
TRF37C32IRTVR	WQFN	RTV	32	3000	350.0	350.0	43.0

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4206245/C 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

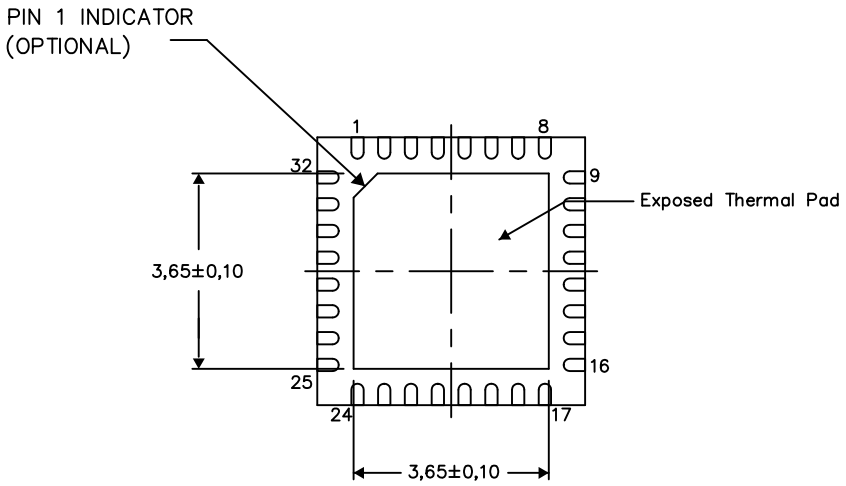
RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206250–7/Q 05/15

NOTE: All linear dimensions are in millimeters

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