SN74LVC1G57 Configurable Multiple-Function Gate

1 Features

- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
  - Supports Down Translation to V_{CC}
- Max t_{pd} of 6.3 ns at 3.3 V
- Schmitt-Triggered Inputs
- Low Power Consumption, 10-µA Maximum I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Available in the Texas Instruments NanoFree™ Package

2 Applications

- Active Noise Cancellation (ANC)
- Barcode Scanners
- Blood Pressure Monitors
- CPAP Machines
- Cable Solutions
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- HVAC: Heating, Ventilating, and Air Conditioning
- TVs: High-Definition (HDTV), LCD, and Digital
- Video Communications Systems

3 Description

The SN74LVC1G57 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

This configurable multiple-function gate is designed for 1.65-V to 5.5-V V_{CC} operation.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

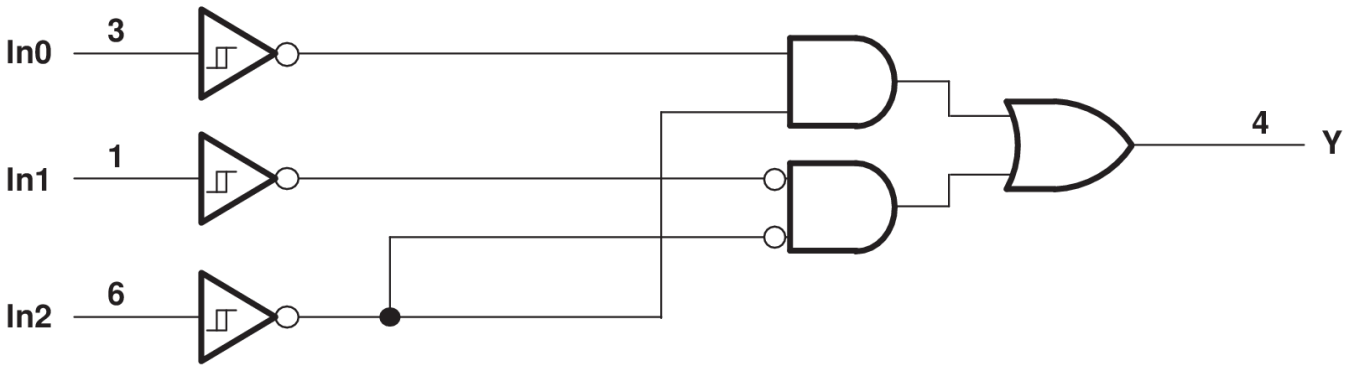
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
SN74LVC1G57DBV	SOT-23 (6)	2.90 mm × 1.60 mm
SN74LVC1G57DCK	SC70 (6)	2.00 mm × 1.25 mm
SN74LVC1G57DRL	SOT (6)	1.60 mm × 1.20 mm
SN74LVC1G57DRY	SON (6)	1.45 mm × 1.00 mm
SN74LVC1G57DSF	SON (6)	1.00 mm × 1.00 mm
SN74LVC1G57YZP	DSBGA (6)	1.41 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (December 2013) to Revision P — **Page**

- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed Package thermal impedance, $R_{\theta JA}$, values From: 165°C/W To: 223°C/W (DBV), From: 259°C/W To: 271.7°C/W (DCK), From: 142°C/W To: 252.5°C/W (DRL), and From: 123°C/W To: 124°C/W (YZP) ... 5

Changes from Revision N (April 2013) to Revision O — **Page**

- Changed I_{off} in *Features* ... 1
- Changed Operating temperature range ... 4

Changes from Revision M (October 2011) to Revision N — **Page**

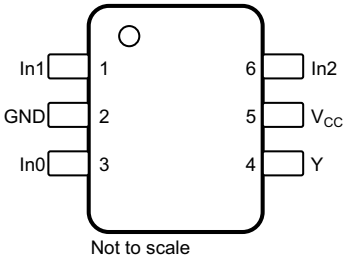
- Removed Ordering Information table; package updates now included in Package Ordering Addendum ... 1

Changes from Revision L (January 2007) to Revision M — **Page**

- Added additional package options to the Ordering Information table ... 1
- Added DRY and DSF packages to data sheet ... 1

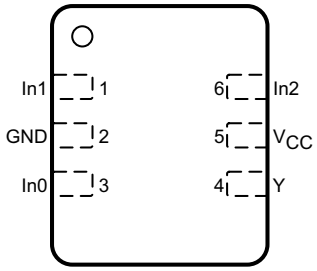
5 Pin Configuration and Functions

DBV, DCK, or DRL Package
6-Pin SOT-23, SC70, or SOT
Top View



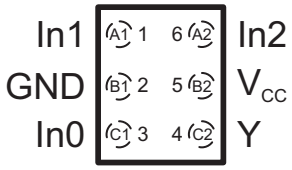
Not to scale

DRY or DSF Package
6-Pin SON
Top View



Not to scale

YZP Package
6-Pin DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	In1	I	Logic input 1
2	GND	—	Ground
3	In0	I	Logic input 0
4	Y	O	Logic output
5	V_{CC}	—	Power
6	In2	I	Logic input 2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	6.5	V
Input voltage, V_I(2)		–0.5	6.5	V
Voltage range (applied to any output), V_O	High-impedance or power-off state(2)	–0.5	6.5	V
	High or low state(2)(3)	–0.5	V_{CC} + 0.5	
Input clamp current, I_{IK} (V_I < 0)			–50	mA
Output clamp current, I_{OK} (V_O < 0)			–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
T_A	Operating free-air temperature	BGA package	–40	85	°C
		All other packages	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation, see *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC1G57						UNIT
		DBV (SOT)	DCK (SOT)	DRL (SOT)	YZP (DSGBA)	DSF (SON)	DRY (SON)	
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	223	271.7	252.5	124	360.1	332.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	174.4	129.8	111.6	1.4	158.8	198.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71	73.1	118.5	29.7	213.5	189	°C/W
ψ_{JT}	Junction-to-top characterization parameter	57.1	8.3	11.8	0.5	20.4	44.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.3	72.4	118.8	30.1	213.2	189.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_{CC} = 1.65 V		0.79		1.16	V
		V_{CC} = 2.3 V		1.11		1.56	
		V_{CC} = 3 V		1.5		1.87	
		V_{CC} = 4.5 V		2.16		2.74	
		V_{CC} = 5.5 V		2.61		3.33	
V_{T-}	Negative-going input threshold voltage	V_{CC} = 1.65 V		0.35		0.62	V
		V_{CC} = 2.3 V		0.58		0.87	
		V_{CC} = 3 V		0.84		1.19	
		V_{CC} = 4.5 V		1.41		1.9	
		V_{CC} = 5.5 V		1.87		2.29	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 1.65 V		0.3		0.62	V
		V_{CC} = 2.3 V		0.4		0.8	
		V_{CC} = 3 V		0.53		0.87	
		V_{CC} = 4.5 V		0.71		1.04	
		V_{CC} = 5.5 V		0.71		1.11	
V_{OH}		V_{CC} = 1.65 V to 5.5 V, I_{OH} = –100 µA		V_{CC} – 0.1			V
		V_{CC} = 1.65 V, I_{OH} = –4 mA		1.2			
		V_{CC} = 2.3 V, I_{OH} = –8 mA		1.9			
		V_{CC} = 3 V, I_{OH} = –16 mA		2.4			
		V_{CC} = 3 V, I_{OH} = –24 mA		2.3			
		V_{CC} = 4.5 V, I_{OH} = –32 mA		3.8			
V_{OL}		V_{CC} = 1.65 V to 5.5 V, I_{OL} = 100 µA				0.1	V
		V_{CC} = 1.65 V, I_{OL} = 4 mA				0.45	
		V_{CC} = 2.3 V, I_{OL} = 8 mA				0.3	
		V_{CC} = 3 V, I_{OL} = 16 mA	T_A = –40°C to 85°C			0.4	
			T_A = –40°C to 125°C			0.45	
		V_{CC} = 3 V, I_{OL} = 24 mA				0.55	
		V_{CC} = 4.5 V, I_{OL} = 32 mA	T_A = –40°C to 85°C			0.55	
			T_A = –40°C to 125°C			0.58	
I_I		V_{CC} = 0 V to 5.5 V, V_I = 5.5 V or GND				±1	µA
I_{off}		V_{CC} = 0 V, V_I or V_O = 5.5 V				±10	µA
I_{CC}		V_{CC} = 1.65 V to 5.5 V, V_I = 5.5 V or GND, I_O = 0				10	µA
ΔI_{CC}		V_{CC} = 3 V to 5.5 V, one input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND				500	µA
C_i		V_{CC} = 3.3 V, V_I = V_{CC} or GND			3.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz, T_A = 25°C	V_{CC} = 1.8 V		20		pF
			V_{CC} = 2.5 V		20		
			V_{CC} = 3.3 V		21		
			V_{CC} = 5 V		22		

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted; see Figure 3)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	Any input to Y (output)	T_A = –40°C to 85°C	V_{CC} = 1.8 V ± 0.15 V	3.2		14.4	ns
			V_{CC} = 2.5 V ± 0.2 V	2		8.3	
			V_{CC} = 3.3 V ± 0.3 V	1.5		6.3	
			V_{CC} = 5 V ± 0.5 V	1.1		5.1	
		T_A = –40°C to 125°C	V_{CC} = 1.8 V ± 0.15 V	3.2		16.4	
			V_{CC} = 2.5 V ± 0.2 V	2		9.3	
			V_{CC} = 3.3 V ± 0.3 V	1.5		7.3	
			V_{CC} = 5 V ± 0.5 V	1.1		6.1	

6.7 Typical Characteristics

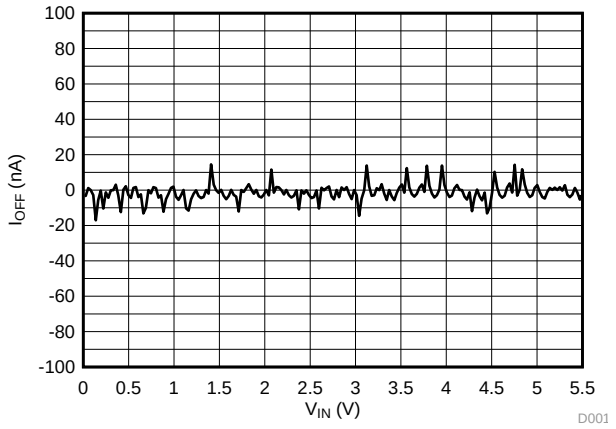


Figure 1. Partial-Power-Down Mode I_{OFF} Across V_{IN}

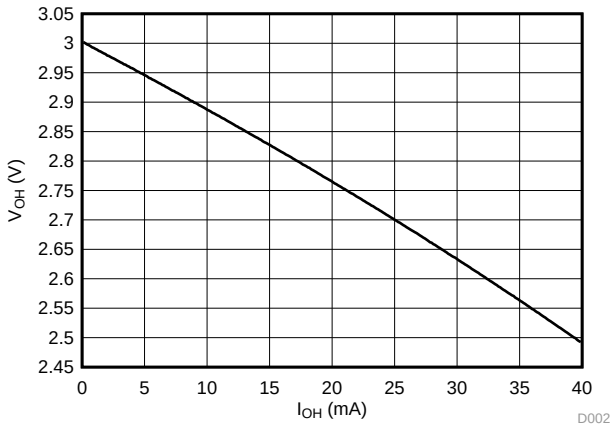
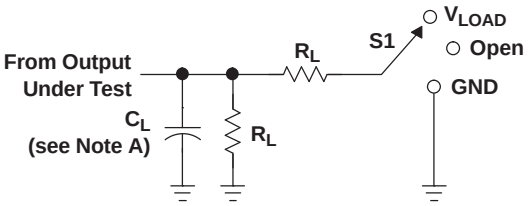


Figure 2. Output Voltage (V_{OH}) vs Current (I_{OH})

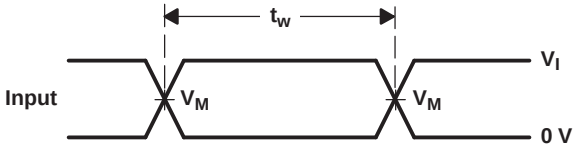
7 Parameter Measurement Information



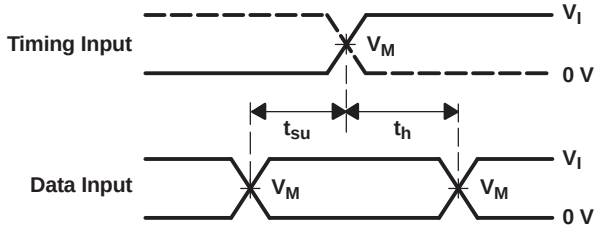
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

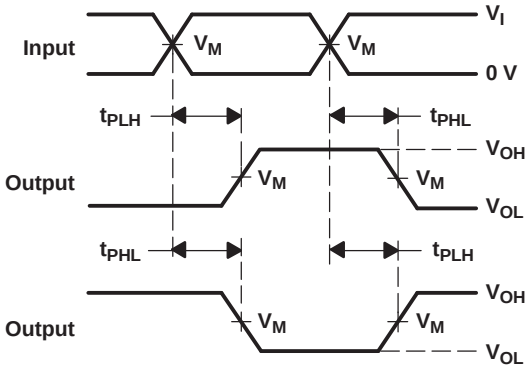
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



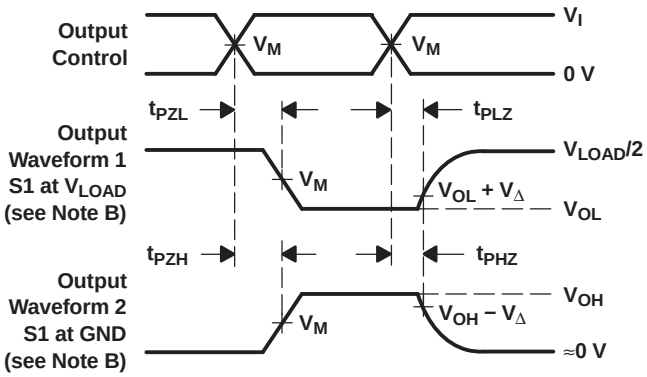
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

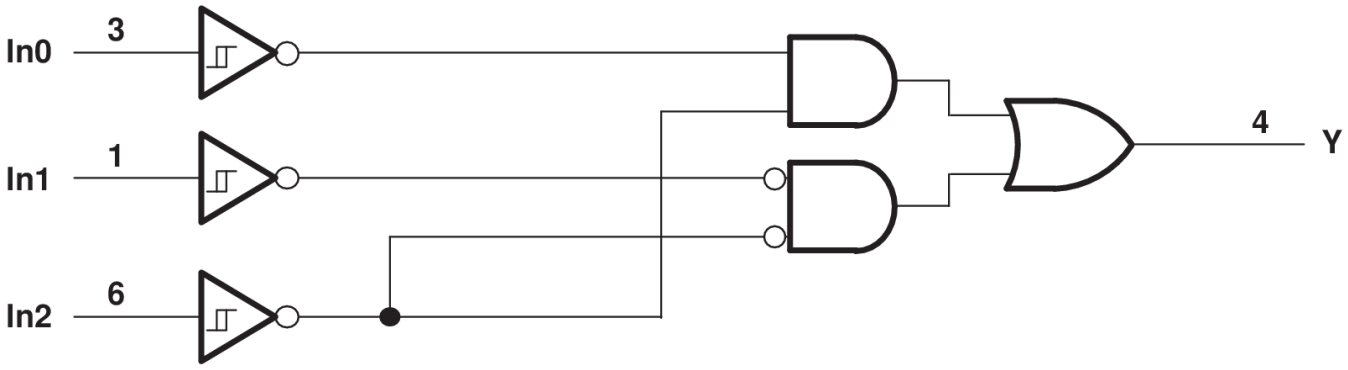
8.1 Overview

The SN74LVC1G57 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

This configurable multiple-function gate is designed for 1.65-V to 5.5-V V_{CC} operation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Schmitt-Trigger Inputs

Schmitt-trigger inputs are designed to provide a minimum separation between positive and negative switching thresholds. This allows for noisy or slow inputs that would cause problems such as oscillation or excessive current draw with normal CMOS inputs

8.3.2 Inputs Accept Voltages to 5.5 V

The SN74LVC1G57 is a configurable multiple-function gate is designed for 1.65-V to 5.5-V V_{CC} operation. Inputs are over-voltage tolerant up to 5.5 V. This feature allows the use of this device as a translator in a mixed 1.8-V, 3.3-V, and 5-V system environment.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1G57 and Table 2 lists the logic configuration images.

Table 1. Function Table

INPUTS			OUTPUT
In2	In1	In0	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

Table 2. Logic Configurations

LOGIC FUNCTION	FIGURE NO.
2-Input AND	Figure 4
2-Input AND with both inputs inverted	Figure 7
2-Input NAND with inverted input	Figure 5 and Figure 6
2-Input OR with inverted input	Figure 5 and Figure 6
2-Input NOR	Figure 7
2-Input NOR with both inputs inverted	Figure 4
2-Input XNOR	Figure 8

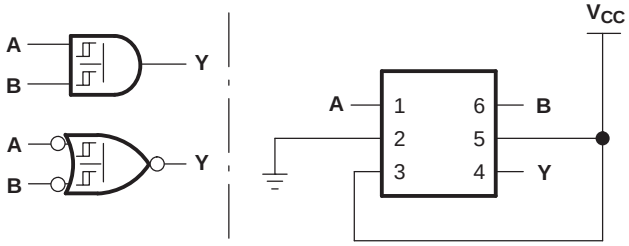


Figure 4. 2-Input AND Gate

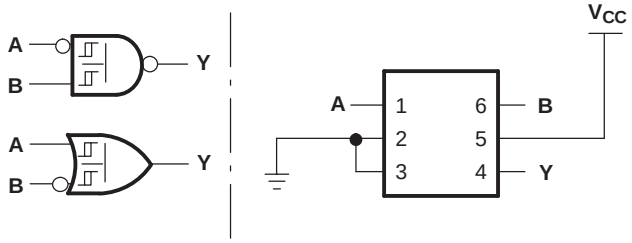


Figure 5. 2-Input NAND Gate With Inverted A Input

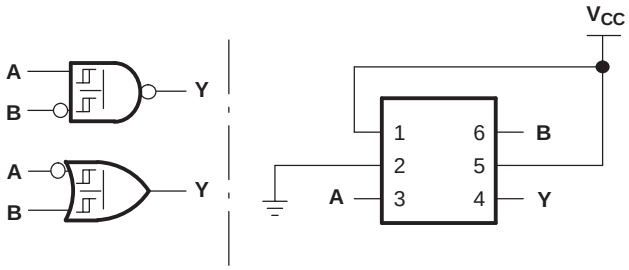


Figure 6. 2-Input NAND Gate With Inverted B Input

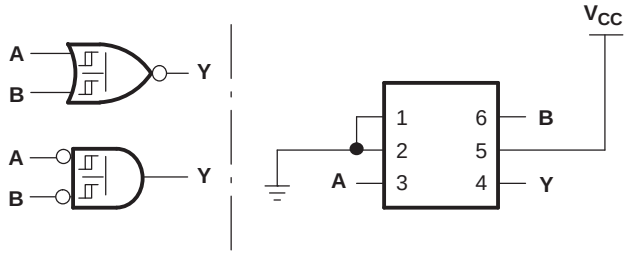


Figure 7. 2-Input NOR Gate

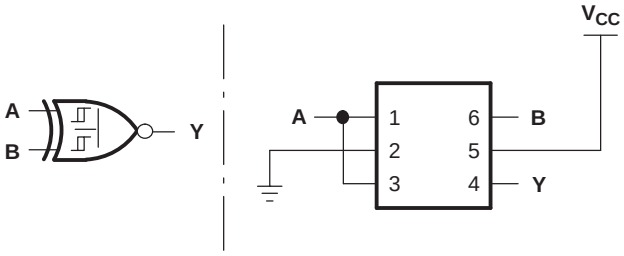


Figure 8. 2-Input XNOR Gate

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G57 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

9.2 Typical Application

This application shows the SN74LVC1G57 configured as an OR gate with an inverted input. This particular configuration is helpful for dual sensor or switch applications where one of the inputs is normally closed or a logic high *1*. Normally this application would require two external gates, but because the SN74LVC1G57 can be configured to meet this function the application can be implemented with a single chip solution.

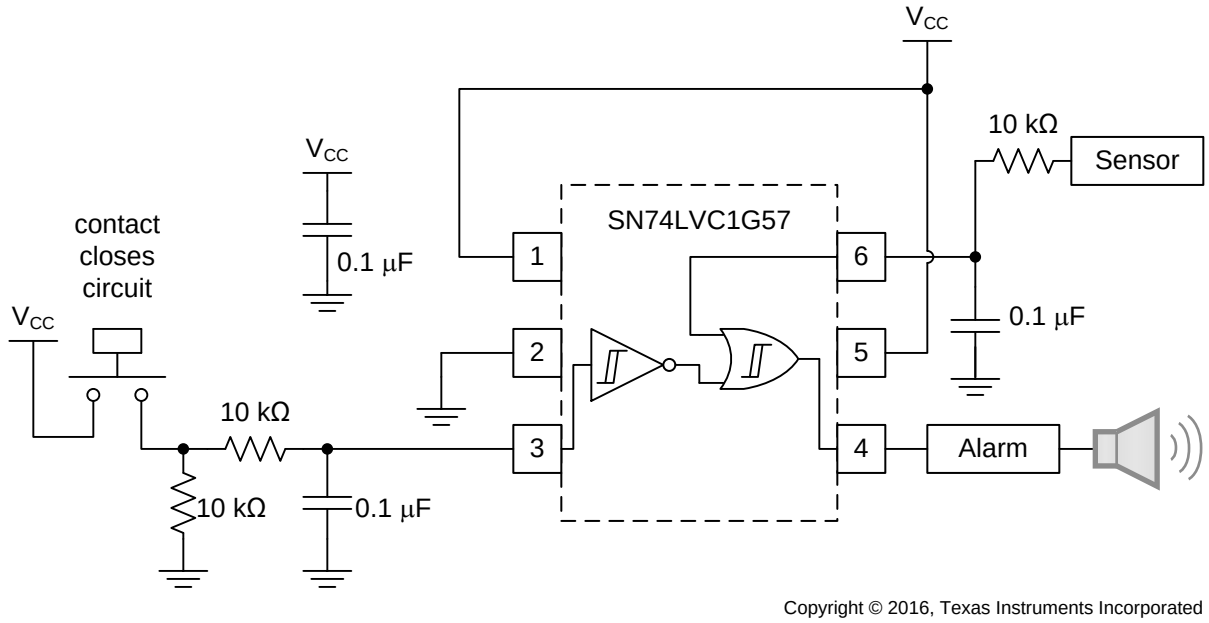


Figure 9. Dual-Sensor Alarm Trigger

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Application Truth Table

Because we are working with two independent alarm triggers, we need to ensure that the alarm signal is only sent whenever either condition is met. Therefore our resulting truth table will look very much like a logic OR function. However, since we are also assuming one of the conditions to always be true, i.e. a door that should remain closed, we make use of the inverted input in Table 3.

Table 3. Dual-Sensor Truth Table

INPUTS		OUTPUT
TRIGGER OR SWITCH	SENSOR	ALARM
L	X	H
H	L	L
X	H	H

9.2.1.2 Schmitt-Trigger Inputs

On a normal (non-Schmitt-Trigger) input the part will switch at the same point on the rising edge and falling edge. With a slow rising edge the part will switch at the threshold. When the switch occurs it will require current from V_{CC}. When current is forced from V_{CC}, the V_{CC} level can drop causing the threshold to shift. When the threshold shifts it will cross the input again causing the part to switch again. This can go on and on causing oscillation which can cause excessive current. The same thing can happen if there is noise on the input. The noise can cross the threshold multiple times and cause oscillation or multiple clocking. The solution to these problems is to use a Schmitt-Trigger type device to translate the slow or noisy edges into something faster that will meet the input rise and fall specs of the following device. A true Schmitt-Trigger input will not have rise and fall time limitations.

9.2.2 Detailed Design Procedure

1. Recommended Input conditions:
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended output conditions:
   - Load currents should not exceed 20 mA on the output and 50 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves

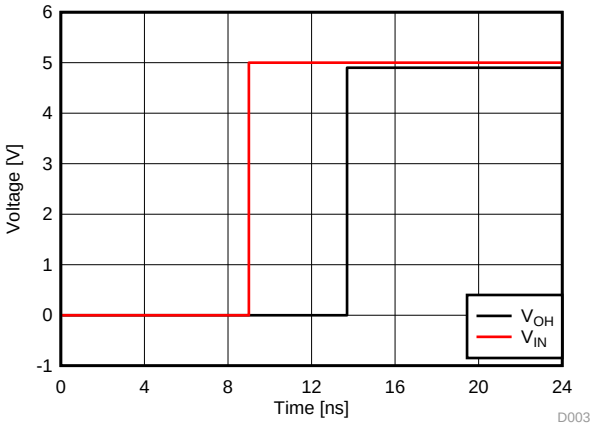


Figure 10. Simulated Output V_{OH} at 5 V and 25°C

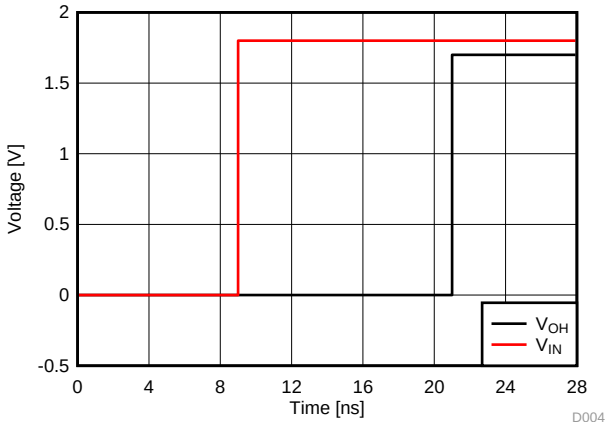


Figure 11. Simulated Output V_{OH} at 1.8 V and 25°C

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 12 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

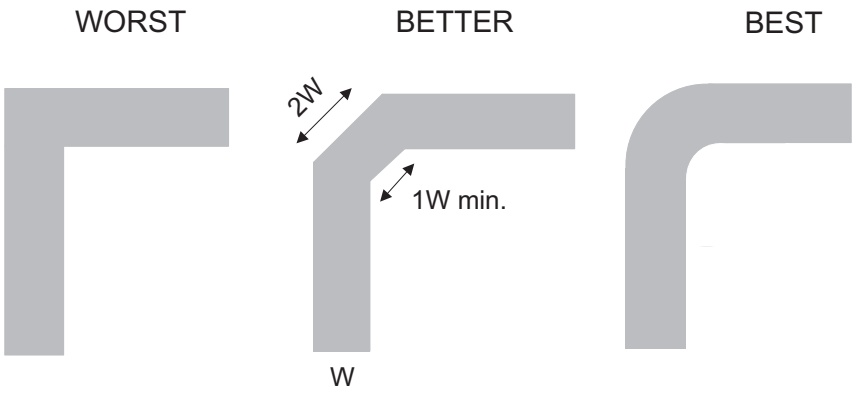


Figure 12. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G57DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CA7O, CA7R)	Samples
SN74LVC1G57DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CL5, CLF, CLJ, CLK, CLR)	Samples
SN74LVC1G57DCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CLF	Samples
SN74LVC1G57DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(1K2, CL7, CLR)	Samples
SN74LVC1G57DRY2	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL	Samples
SN74LVC1G57DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL	Samples
SN74LVC1G57DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL	Samples
SN74LVC1G57YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CLN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

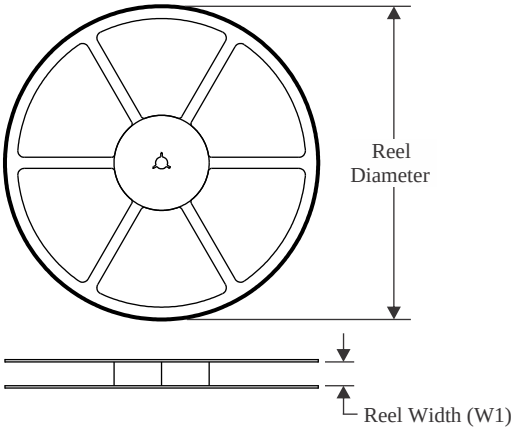
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

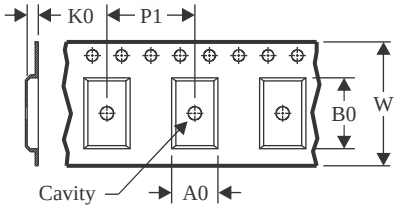
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

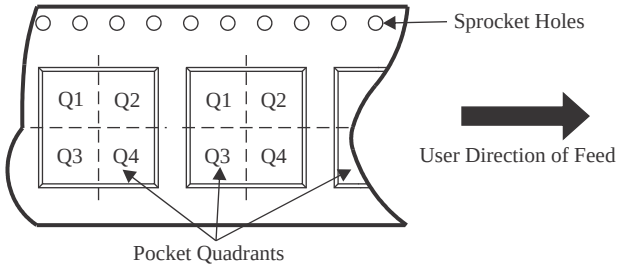


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

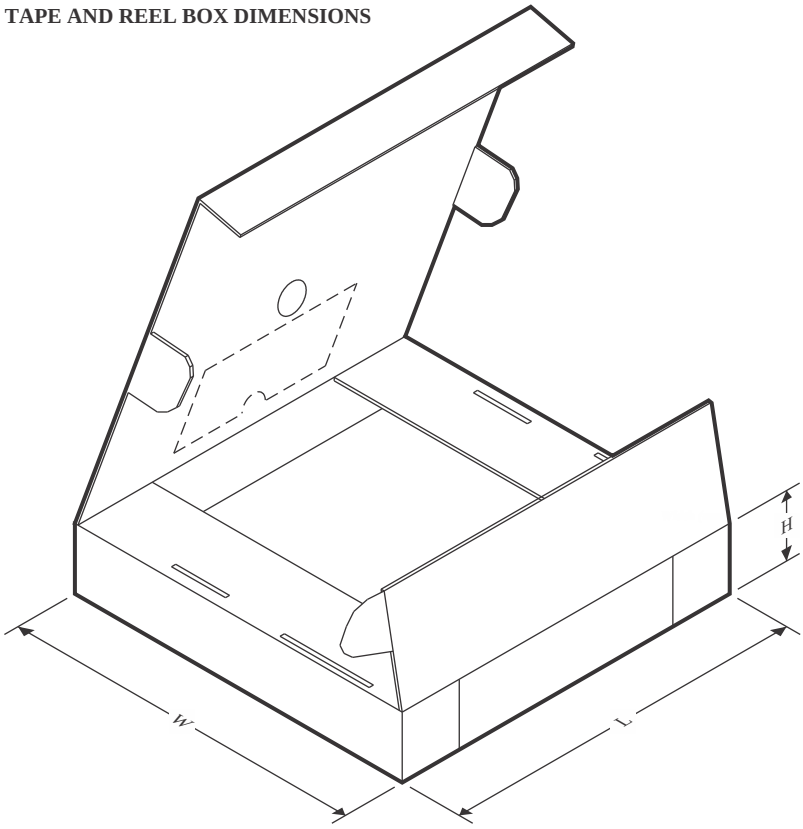
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G57DCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G57DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G57DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G57DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G57DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G57DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G57YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

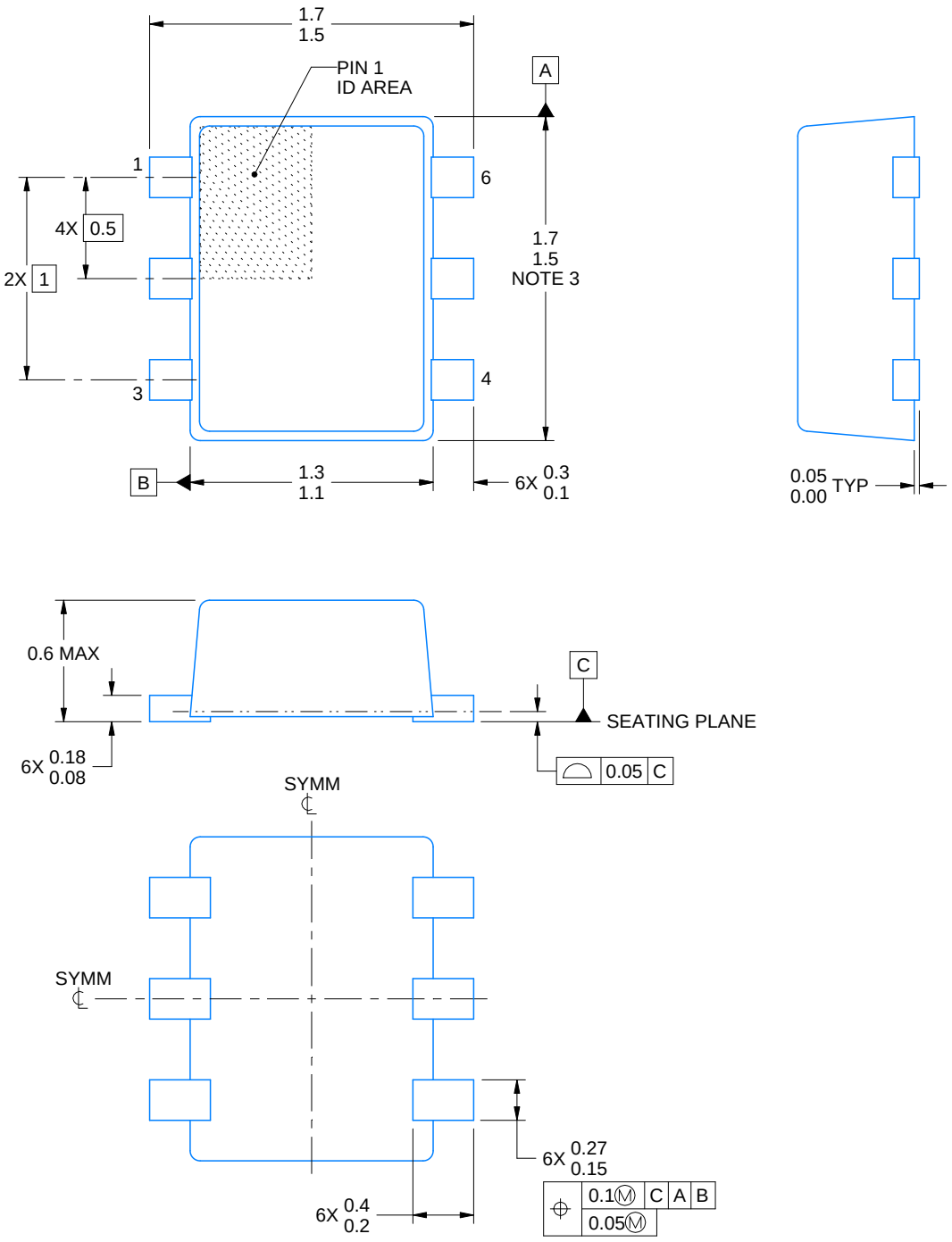
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G57DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G57DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
SN74LVC1G57DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G57DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G57DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G57DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G57YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DRL0006A

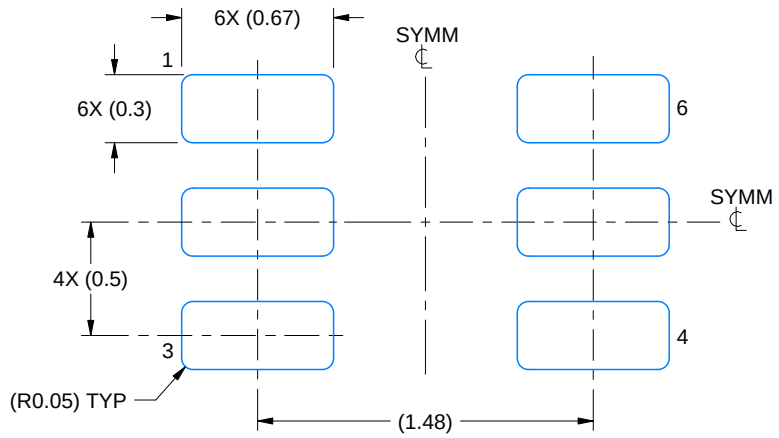
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

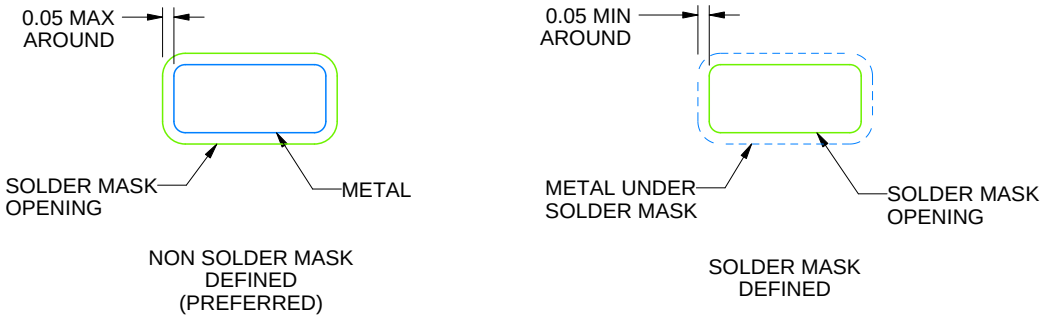


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

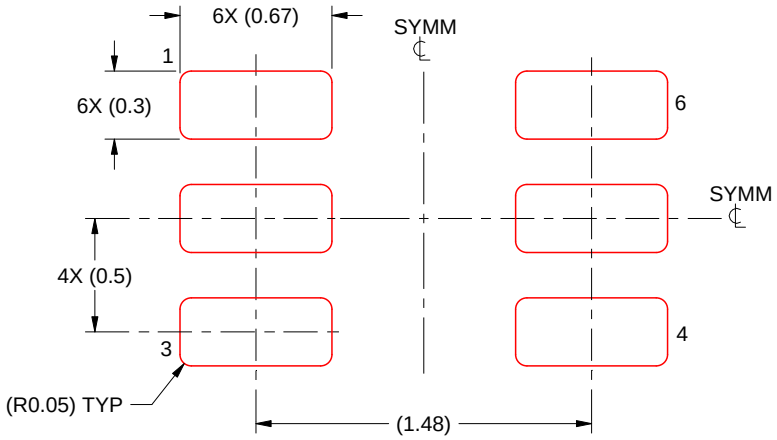
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

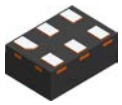
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

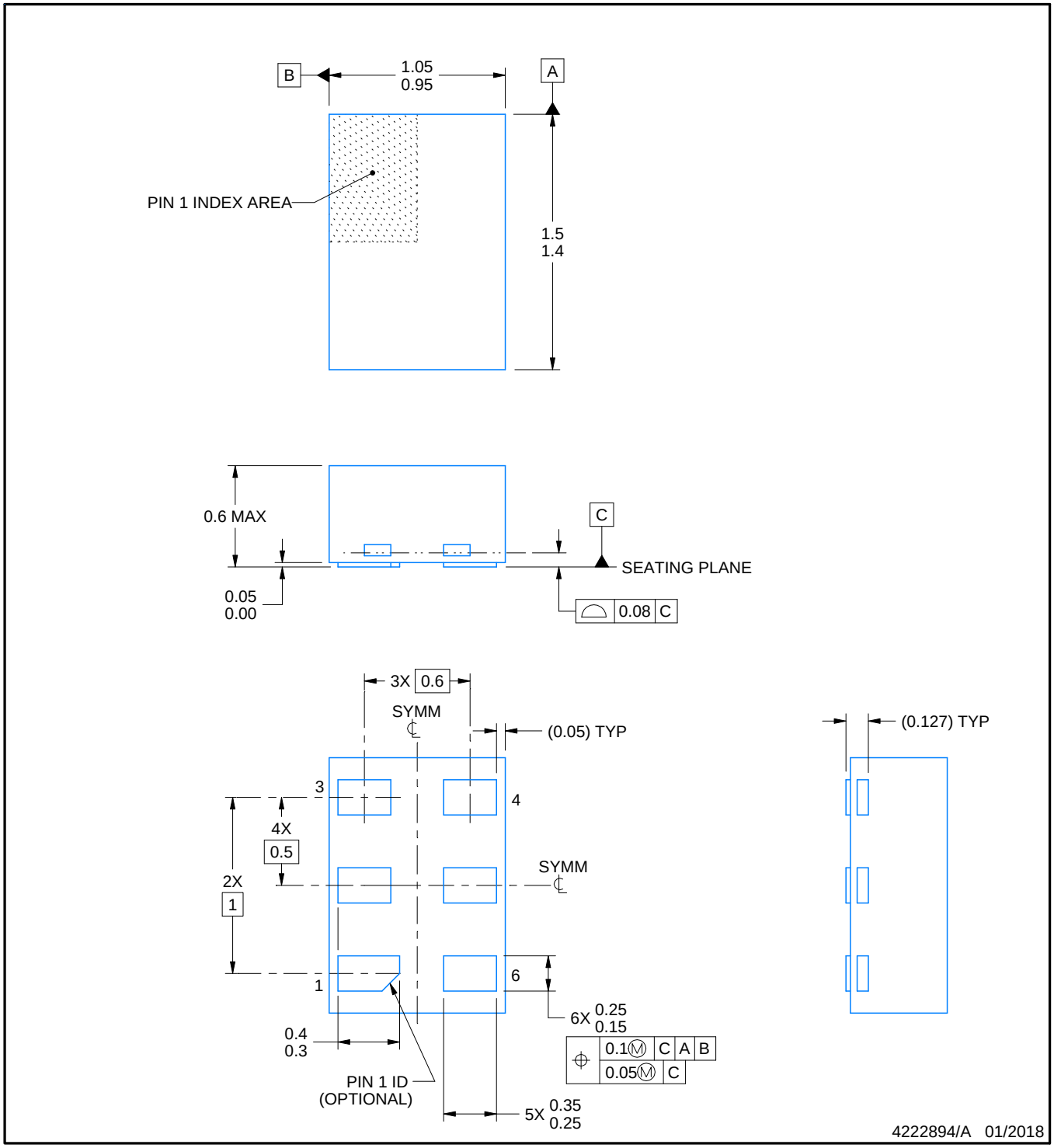
DRY0006A



PACKAGE OUTLINE

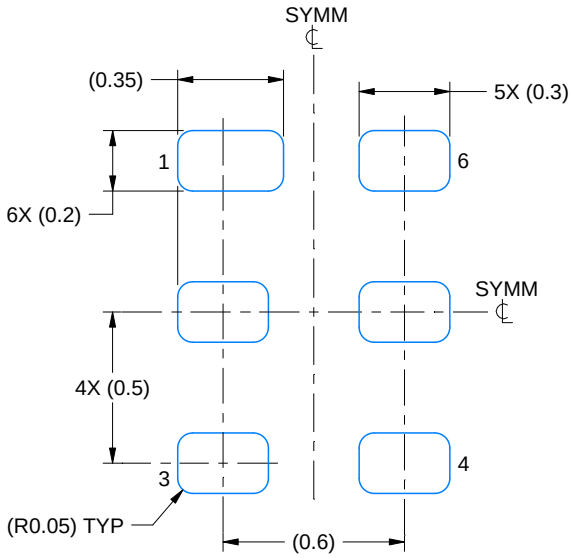
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

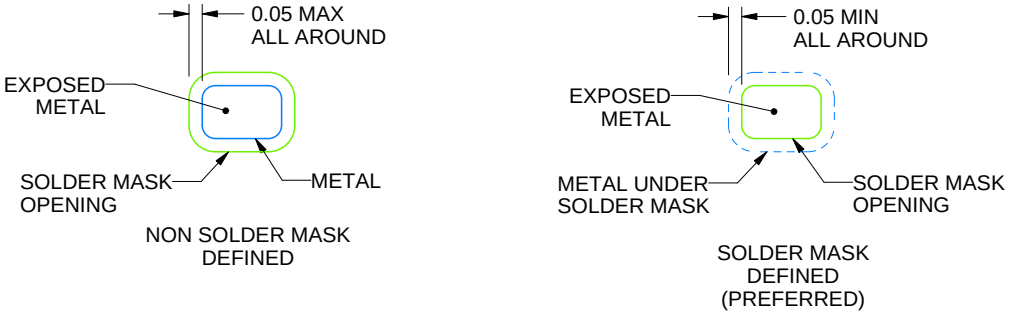


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

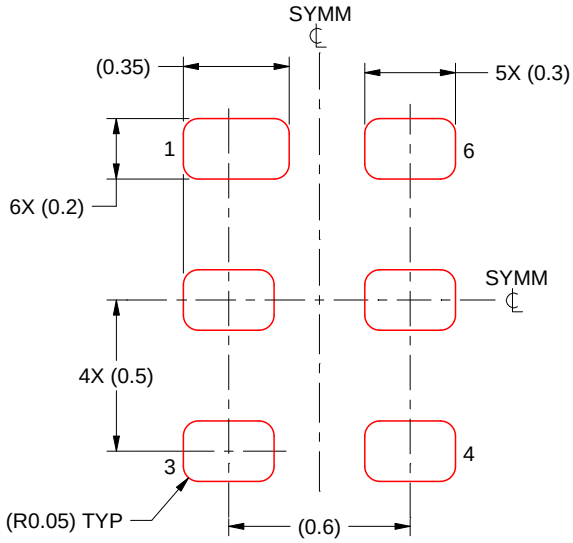
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

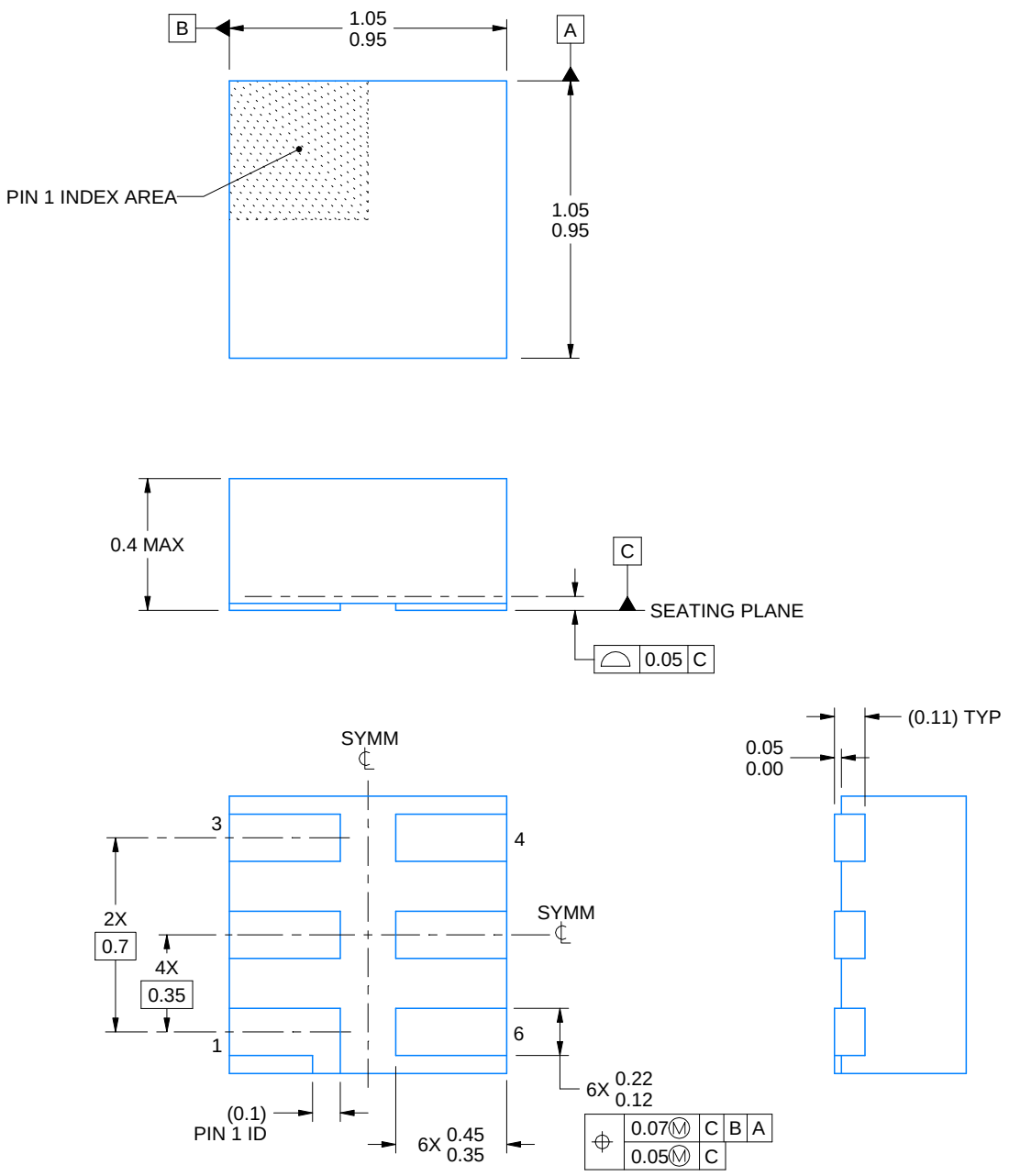
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

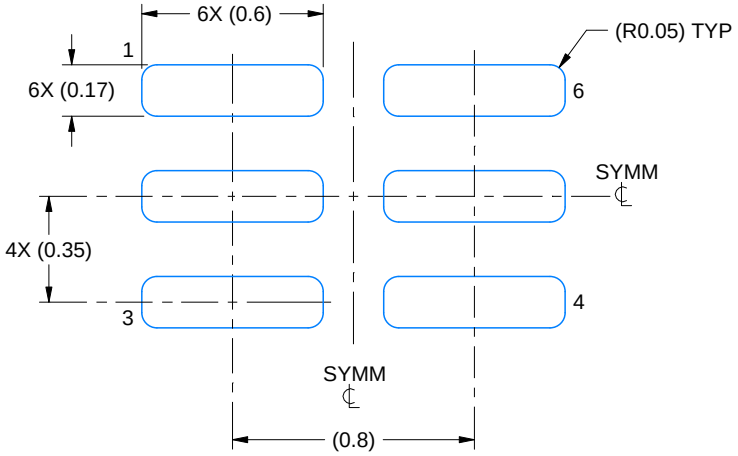
PLASTIC SMALL OUTLINE - NO LEAD



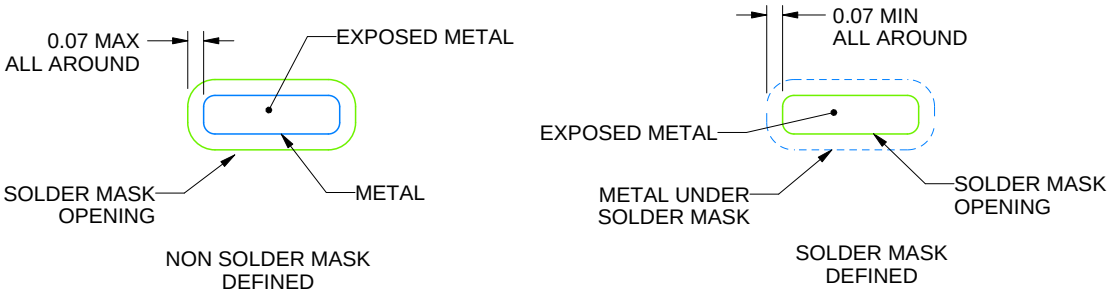
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

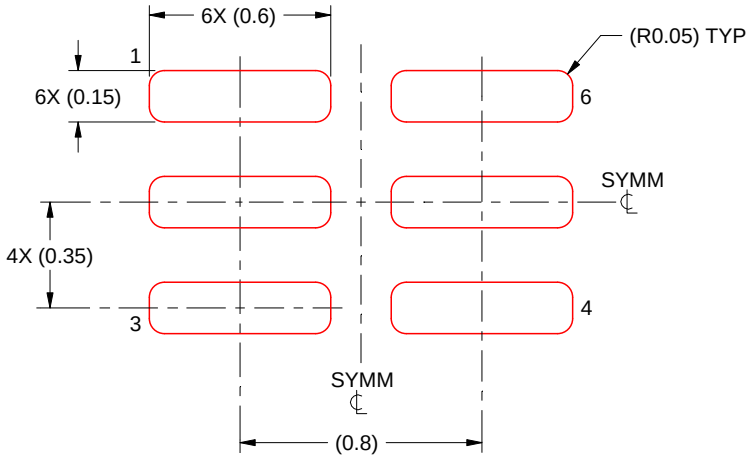
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

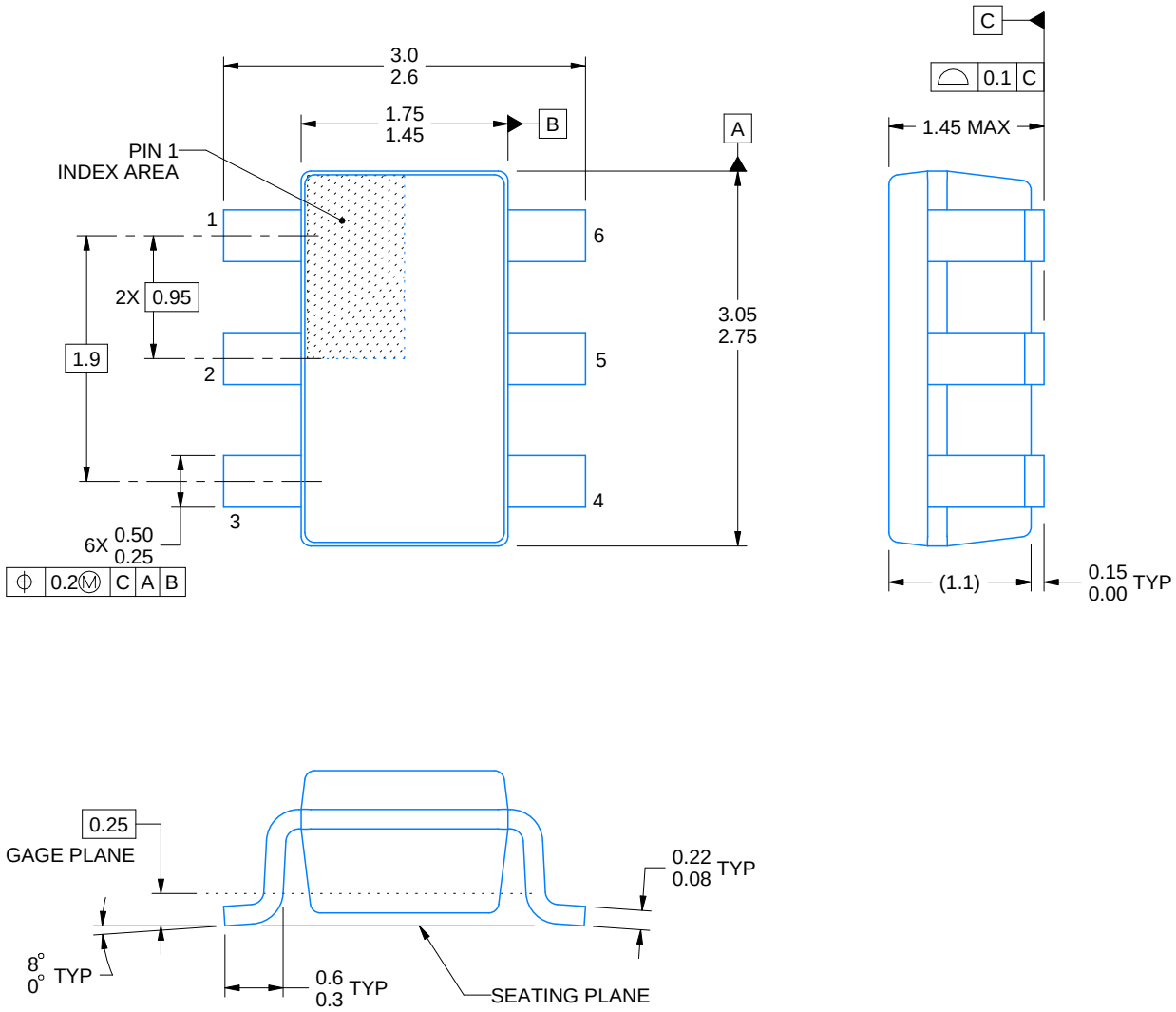
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

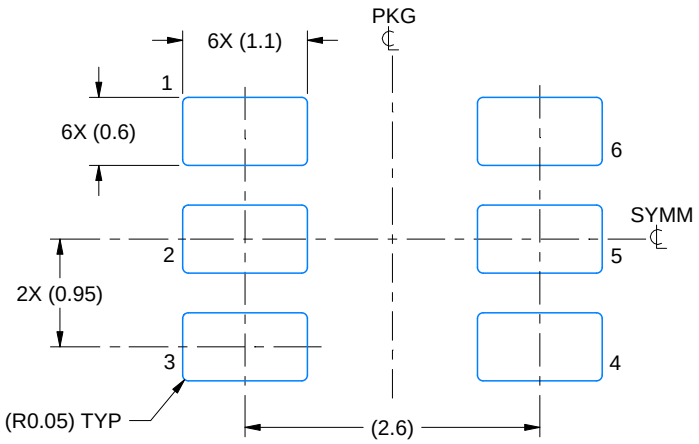
SMALL OUTLINE TRANSISTOR



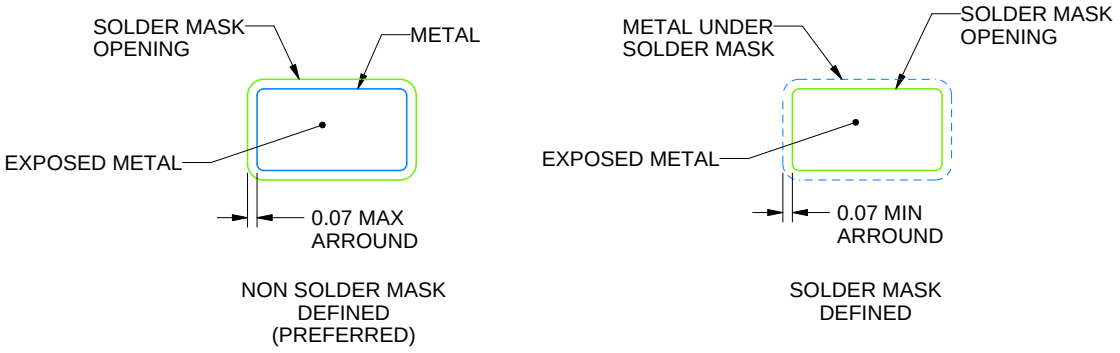
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

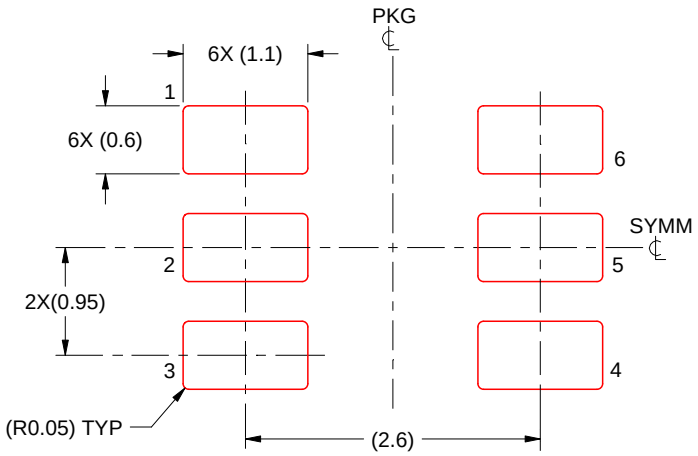


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

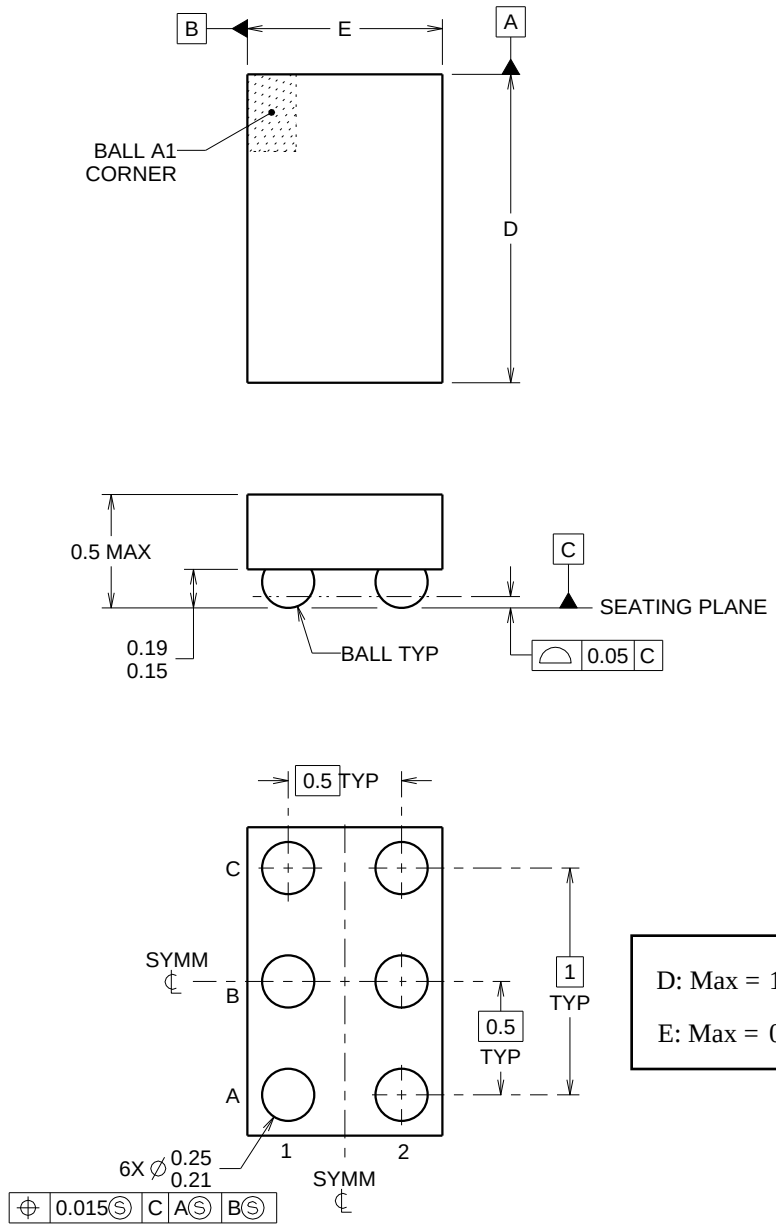
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.358 mm

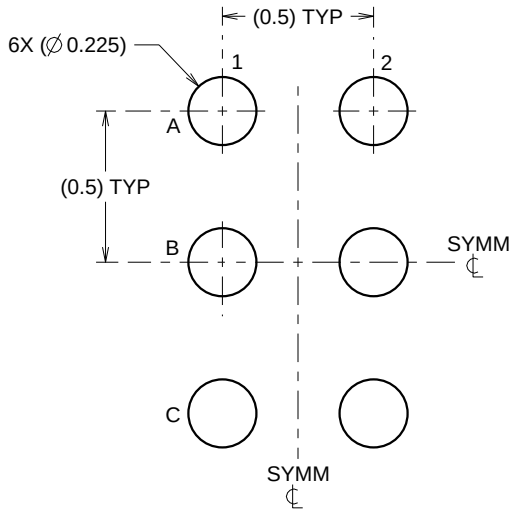
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

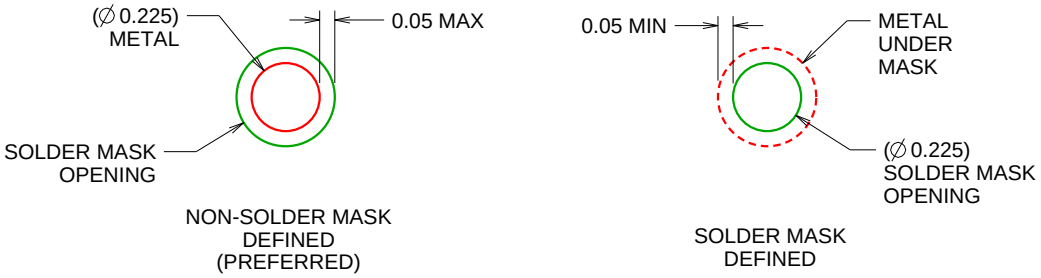
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

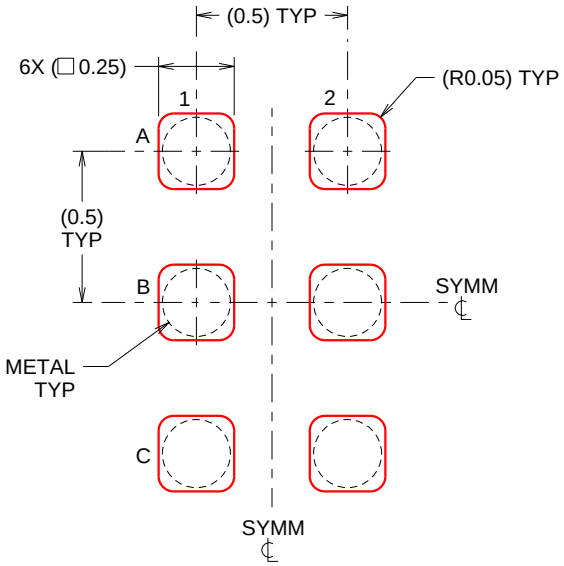


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



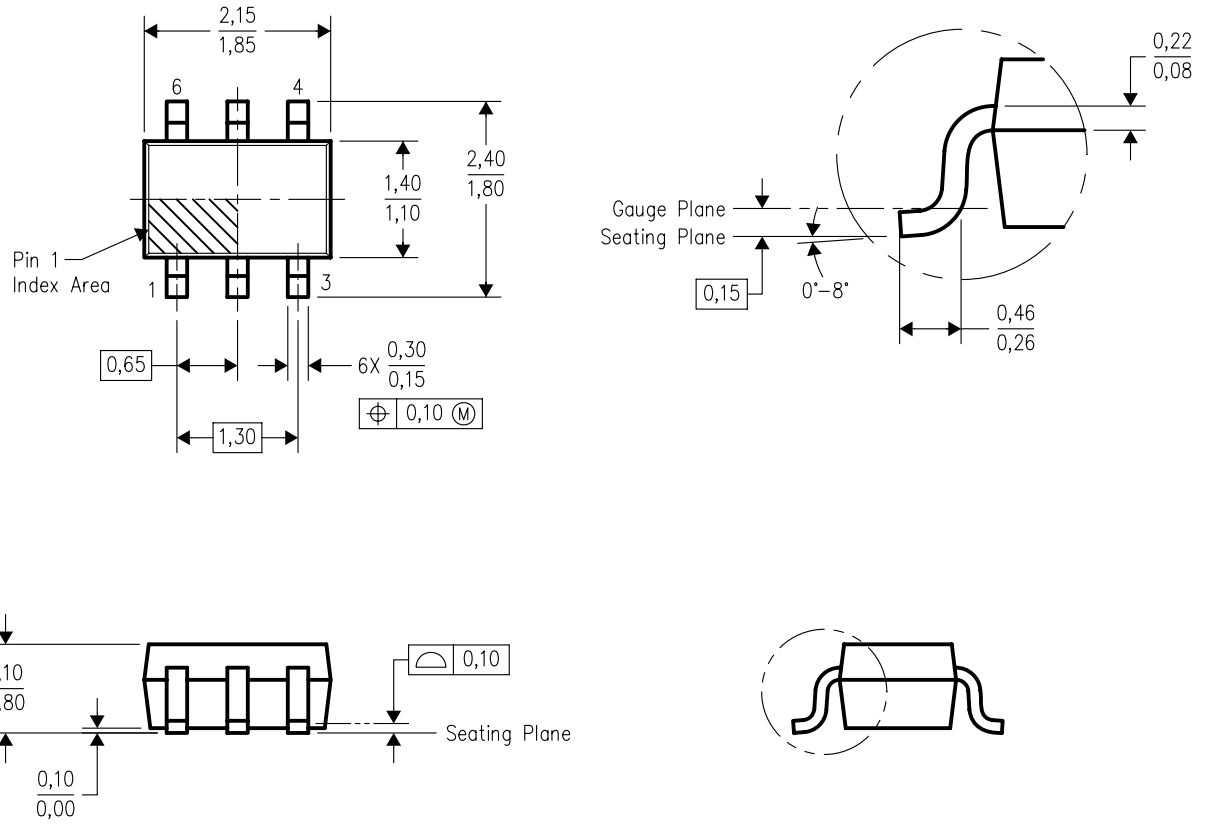
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

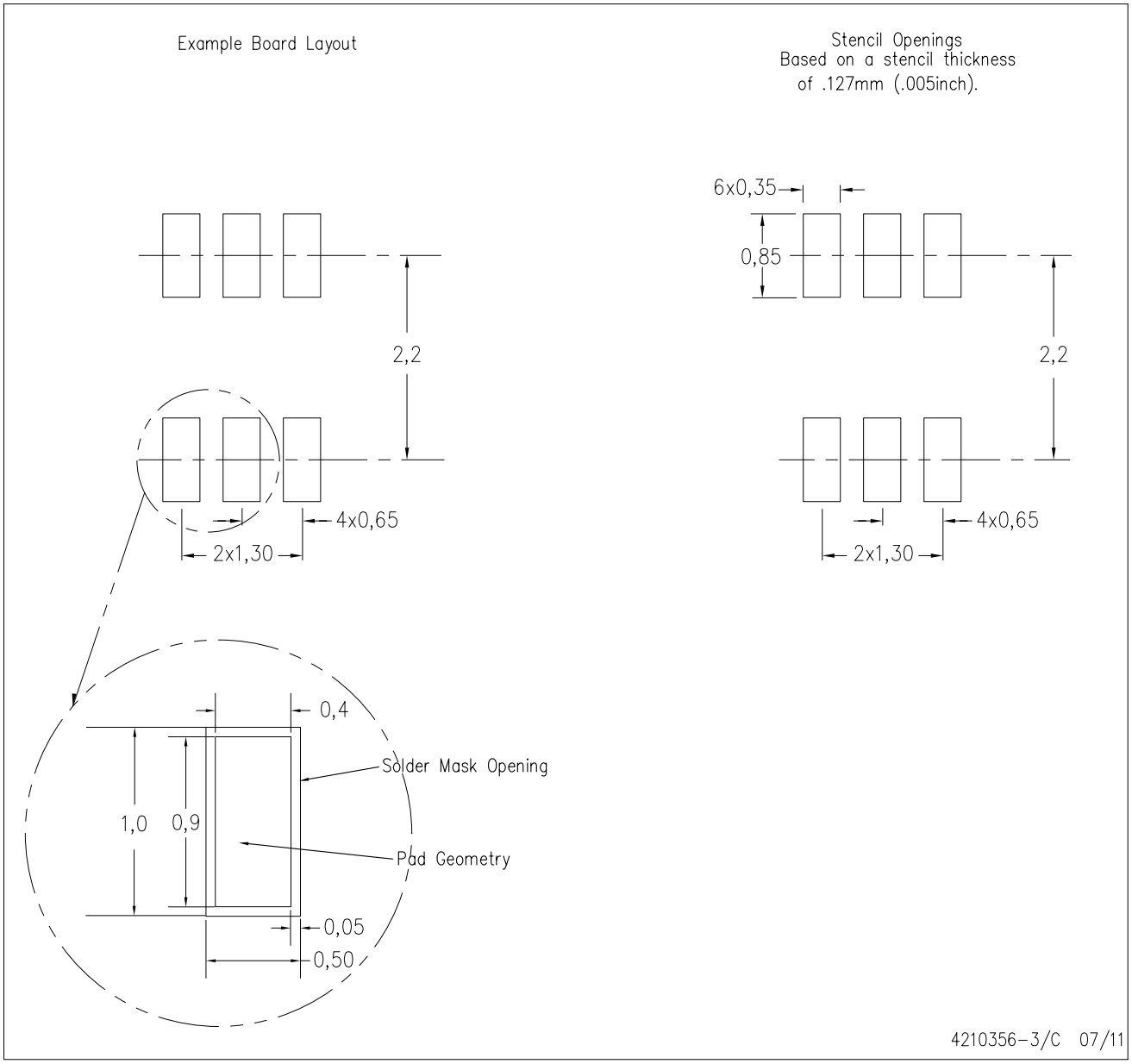
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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